Sizhen(Simon) Wang

Department of Electrical and Computer Engineering
North Carolina State University, Raleigh, NC 27695
(919)995-0818 swang31@ncsu.edu

Applied Position: Device and Process Integration Engineering

Education (*Might be graduated in Dec. 2016*):

- Ph.D, Since *Jan. 2013*, Major in Electrical Engineering, Minor in Materials Science,
  North Carolina State University, Raleigh, NC
  Dissertation: design, fabrication and characterization of high performance GaN power devices with Magnesium ion implanted p-type GaN layer.
  Related Course: Wide Bandgap Power Semiconductor Devices (A^-), Power Electronics (A)
  Semiconductor Devices and Materials Characterization (A^+),
  Principles of Microwave Engineering (A^-), RF Design for Wireless Communication
  Material Science and Process of Semiconductor Devices (A^-),
  VLSI Fabrication Technology (A), Thin Film Process (A), Defects in Solids.
- M.S. in Condensed Matter Physics, *June 2005*, Nanjing University, Nanjing, P. R. China
- B.S. in Physics, *June 2002*, Nanchang University, Nanchang, P. R. China

Experiences in industry:

- Senior device and process integration engineer, Micron Singapore Technology Center,
  Nov. 2011 – Nov. 2012, developed front end process modules and devices for 37nm node DRAM.
- Senior device and process integration engineer, Globalfoundries, Singapore,
  Sept. 2007 – Aug. 2011, as a team leader to develop and ramp up 0.35μm high voltage, and non-volatile memory process.
- Senior Process Integration Engineer, Hejian Technology(Suzhou) Co. Ltd.,
  Jun. 2005- Aug.2007, developed gate stack and trench isolation module for 0.18/0.13μm high voltage process.

Skills and strengths:

- Ten years of working experience in VLSI process integration, Si and wide band-gap power devices.
- Communication well with technical and business staff, and act as a liaison for those groups,
- Strengths in device physics, especially on power semiconductor device physics,
- Strengths in power device design, TCAD simulation with Synopsys Sentaurus,
- Highly skilled in device layout design with Cadence IC design platform,
- Highly competitive in device characterization, design of experiment and problem solving.

Research activities (*Since 2013*):

- Design, fabricate, and characterize GaN JBS power diode with implanted p-GaN to enhance reverse breakdown, reduce reverse leakage (on-going).
- High current, high voltage lateral GaN MIS-HEMT layout design, fabrication and characterization.
- Developed innovative Mg ion implantation and activation annealing process on GaN-on-Si to achieve GaN P-N junction diode rectifier behavior.
- High temperature electrical characterization of commercial GaN power transistors (on-going). .
- As author or co-author, published four papers in IEEE sponsored conferences.