

A multi-loop controller for LCL-filtered grid-connected converters integrated with a hybrid harmonic compensation and a novel virtual impedance

Yonghwan Cho, Maziar Mobarrez, Subhashish Bhattacharya
Department of Electrical and Computer Engineering
North Carolina State University
Raleigh, North Carolina, USA

Abstract—The LCL-filtered converter is widely adapted to interface renewable energy sources and energy storage devices to the grid. While the LCL filter is capable of eliminating current harmonics caused by the high-frequency PWM of the converter, low-order current harmonics are reduced selectively by the stationary-frame resonant harmonic compensators (HCs). There are two types of the harmonic compensator, namely, harmonic current compensator (HCC) and harmonic voltage compensator (HVC). HCCs are in general embedded in parallel with conventional grid current controllers by which the active and reactive power are regulated. If autonomous islanding operation is required, the active and reactive power are controlled by a V - f droop method and a filter capacitor voltage controller with which HCCs or HVCs are added in parallel. In this paper, a multi-loop controller is proposed as one possible alternative to the conventional grid current controller to improve the harmonic compensation performance by using both HCCs and HVCs, which is a hybrid harmonic compensation (HHC). In addition, a novel virtual impedance implementation technique which fits to the multi-loop frame is presented to maintain stability of the controller in case of large grid impedance.

Index Terms—LCL filter, multi-loop control, hybrid harmonic compensation, virtual impedance.

I. INTRODUCTION

With the increasing penetration of power-electronics-based power conversion such as uninterruptible power supplies (UPSs), distributed generation (DG) systems, etc., the LCL-filtered voltage-source converter (VSC) has drawn much attention due to its better attenuation of switching frequency current harmonics compared to L-filtered VSC [1]-[3]. However, the low-order current harmonics should be removed by using either HCCs or HVCs in order to prevent the grid from being polluted. It is typical to use HCCs when the LCL-filtered VSC controls the grid current to regulate both DC-link voltage and power factor [5], [6], [8]. When the autonomous islanding operation is required and the DC-link voltage is regulated by energy storage devices, the HVCs are used with the filter capacitor voltage controller [6] or the HCCs can be used as proposed in [11].

A major challenge of the harmonic compensation is to add enough number of HCs to meet total harmonic distortion (THD) standards and guarantee stability of the converter at the same time. The maximum frequency of the HC is limited since the phase margin of the harmonic compensation loop decreases as its harmonic frequency increases. Moreover, the stability is worse if the grid impedance is large due to long cable or transformer [4], [8]. To overcome the instability issue, phase compensation methods are presented in [7], [8]. In those methods, conventional resonant HC is modified to have trigonometric terms to compensate the phase of it. In this paper, a multi-loop controller is presented as a possible replacement for the conventional grid current controller to have enough phase margin at high harmonic frequencies without using trigonometric terms and to achieve sufficient harmonics attenuation by implementing both HCCs and HVCs, namely, a hybrid harmonic compensation (HHC). Conventional multi-loop controller has an inner-loop of filter capacitor current or converter-side inductor current to improve dynamic performance and achieve active damping [2], [3], [6]. However, the proposed multi-loop controller has an inner-loop of filter capacitor voltage to provide not only the HHC but also a straightforward criteria of setting the controller gain of the outer-loop. It should be noted that active damping is also feasible with the proposed multi-loop frame by using a feed forward method presented in [2].

To improve the stability of the multi-loop controller at its fundamental frequency, a novel virtual impedance method is also proposed in this paper which fits to the multi-loop structure. Although the virtual impedance method is needed mainly for stabilizing LC-filtered VSC [2], [9], [10], the LCL-filtered VSC also faces the instability especially when the grid-side inductance of the LCL filter is small compared to the grid inductance. To implement differentiation of the grid current without high-frequency noise amplification, a high-pass filter is used in [9] and a proportional gain is ignored in [2] which both degrade accuracy of the fundamental frequency controller. The new method implements only imaginary value of the differentiation term at fundamental frequency instead of

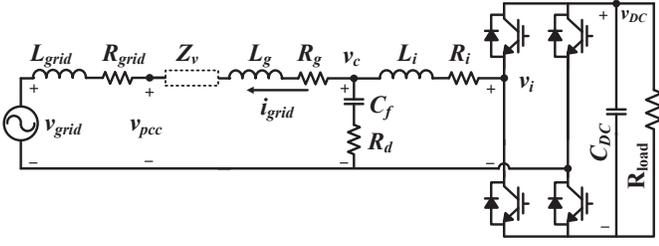


Fig. 1. Circuit diagram of the LCL-filtered grid-connected VSC.

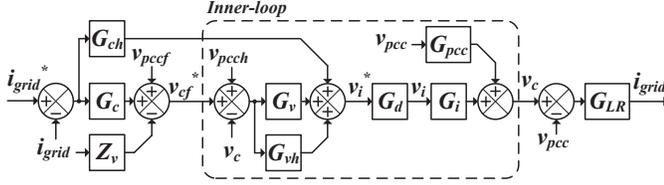


Fig. 2. Block diagram of the proposed multi-loop controller integrated with the HHC and the virtual impedance method.

the whole differentiation to avoid the noise amplification and the inaccuracy. It is based on the implementation method of imaginary value presented initially to extract positive sequence of the grid voltage [12] and the multi-loop structure proposed in this paper. Experiment results are presented to validate the proposed hybrid harmonic compensation scheme and virtual impedance method.

II. PROPOSED MULTI-LOOP CONTROLLER AND HYBRID HARMONIC COMPENSATION

Fig. 1 shows a single-phase LCL-filtered VSC connected to a point of common coupling (PCC). A damping resistor and the virtual impedance is connected in series with the filter capacitor and the grid-side inductor of the LCL filter, respectively. L_{grid} and R_{grid} represent the grid impedance.

The proposed multi-loop structure is shown in Fig. 2, where the HHC and the virtual impedance method are integrated. In the inner-loop, the fundamental and harmonic capacitor voltages are controlled by non-ideal P+Resonant (PR) controllers

$$G_v = K_{pv} + \frac{2K_{iv}\omega_{cv}s}{s^2 + 2\omega_{cv}s + \omega_f^2} \quad (1)$$

$$G_{vh} = \sum_h \frac{2K_{ivh}\omega_{cvh}s}{s^2 + 2\omega_{cvh}s + \omega_h^2} \quad (2)$$

where ω_f and ω_h are the system fundamental and harmonic angular frequency, ω_{cv} and ω_{cvh} are cutoff bandwidth at fundamental and each harmonic frequency, K_{iv} and K_{ivh} are the integral gain at fundamental and each harmonic frequency, and K_{pv} is the proportional gain at all frequencies. G_d denotes PWM delay which is approximately one and a half of the sampling period since the delay is not compensated. G_i and

G_{pcc} denote v_c/v_i and v_c/v_{pcc} , respectively. They can be mathematically expressed as follows:

$$G_i(s) = \frac{v_c}{v_i} = \frac{Y_i(s)}{E_i(s)} \quad (3)$$

$$Y_i(s) = L_g C_f R_d s^2 + (L_g + R_g R_d C_f) s + R_g \quad (4)$$

$$E_i(s) = L_g L_i C_f s^3 + C_f (L_g (R_i + R_d) + L_i (R_g + R_d)) s^2 + (L_i + L_g + C_f (R_i R_g + R_i R_d + R_g R_d)) s + R_g + R_i. \quad (5)$$

$$G_{pcc}(s) = \frac{v_c}{v_{pcc}} = \frac{Y_{pcc}(s)}{E_{pcc}(s)} \quad (6)$$

$$Y_{pcc}(s) = L_i C_f R_d s^2 + (L_i + R_i R_d C_f) s + R_i \quad (7)$$

$$E_{pcc}(s) = L_g L_i C_f s^3 + C_f (L_g (R_i + R_d) + L_i (R_g + R_d)) s^2 + (L_i + L_g + C_f (R_i R_g + R_i R_d + R_g R_d)) s + R_g + R_i. \quad (8)$$

The proportional and integral gain at fundamental frequency can be designed by analyzing the Bode diagram of the open-loop transfer function, $G_v G_d G_i$. It should have enough phase and gain margin for stability and large magnitude at fundamental frequency to both guarantee the accuracy of the controller and reject the disturbance term, $G_{pcc} v_{pcc}$.

In the outer-loop, the fundamental and harmonic grid currents are controlled by G_c and G_{ch} which have same form as (1) and (2). Since the inner-loop is controlling the capacitor voltage, the outer-loop plant, G_c , is simply grid admittance as described in (9). Therefore, the proportional and integral gain of the fundamental grid current controller can be set as (10) and (11), which is a widely used gain setting criteria for L-filtered VSCs or motor drive inverters [13]. In (10) and (11), ω_{cc} denotes the bandwidth of the current controller. It should be imposed five–ten times smaller than the bandwidth of the inner-loop in order to prevent undesired coupling effect.

$$G_c = \frac{1}{L_g s + R_g} \quad (9)$$

$$K_{pc} = L_g \omega_{cc} \quad (10)$$

$$K_{ic} = R_g \omega_{cc} \quad (11)$$

The HHC is implemented by using both HCCs and HVCs in the outer-loop and inner-loop, respectively. Unlike HCCs, HVCs need a voltage reference, v_{pcch} , which is a sum of harmonic frequency components of the PCC voltage. By synthesizing the harmonics of the PCC voltage at the filter

capacitor, the harmonic frequency component of the voltage difference across the grid-side inductor of the LCL filter is removed and thus, only fundamental current flows. It should be noted that no filter is needed to extract the PCC voltage harmonics. Since the fundamental frequency component of the PCC voltage, v_{pccf} , is also needed as a feed forward in the outer-loop to improve dynamic performance of the current controller, the PCC voltage measured by a voltage sensor can be used directly to replace the two adding terms, v_{pccf} and v_{pcch} .

The HVCs of the inner-loop are embedded mainly for attenuating high-frequency harmonic currents without any instability issue. The stability of the HCCs of a conventional single-loop controller shown in [1], [2] and that of the HVCs of the proposed multi-loop controller are compared in Fig. 3. The bode diagram of the open-loop transfer function of each case is depicted in Fig. 3(a) and Fig. 3(b), respectively. It is shown that the phase margin decreases as the harmonics frequency increases. In Fig. 3(a), the phase margin is almost zero at 11th harmonics and negative at 13th harmonics. It means that adding 11th or 13th HCCs in the single-loop controller causes instability issue and thus, harmonic currents at those frequencies cannot be suppressed. On the other hand, in Fig. 3(b), the phase margin is larger than 45 degree at both 11th and 13th harmonics. It can be seen that HVCs are better than HCCs in terms of the stability and can handle high-frequency harmonics. In the proposed HHC scheme, HVCs at all harmonic frequencies of interest are used and HCCs at whatever frequencies the system can maintain stability are also added to further attenuate the harmonic currents. It should be noted that the HHC can also be applied to the LCL-filtered VSC whose power is controlled by the V - f droop method and the filter capacitor voltage controller to achieve the autonomous islanding operation. In this application, the harmonic frequency component of the PCC voltage, v_{pcch} , should be extracted by a digital filter since the feed forward of the fundamental frequency component of the PCC voltage, v_{pccf} , becomes a considerable disturbance of the droop method.

III. VIRTUAL IMPEDANCE METHOD

The proposed virtual impedance implementation scheme is described in Fig. 4. It should be noted that the virtual impedance at only fundamental frequency is investigated in this paper. Instead of implementing the differentiation of the grid current to get the voltage drop across the virtual impedance, imaginary part of the voltage drop at fundamental frequency is calculated using the band-pass filter and the all-pass filter

$$H_{BPF} = \frac{2\zeta\omega_f s}{s^2 + 2\zeta\omega_f s + \omega_f^2} \quad (12)$$

$$H_{APF} = -\frac{s - \omega_f}{s + \omega_f} \quad (13)$$

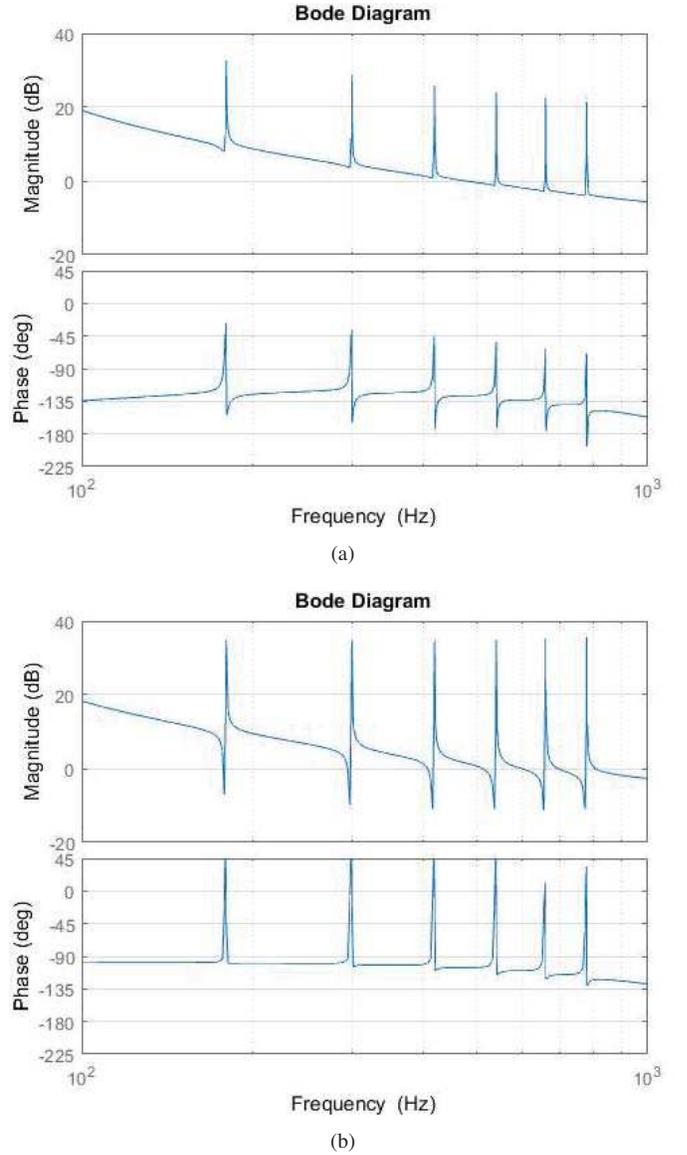


Fig. 3. (a) Bode diagram of the open-loop transfer function of the HCCs in the conventional single-loop controller. (b) Bode diagram of the open-loop transfer function of the HVCs in the proposed multi-loop controller.

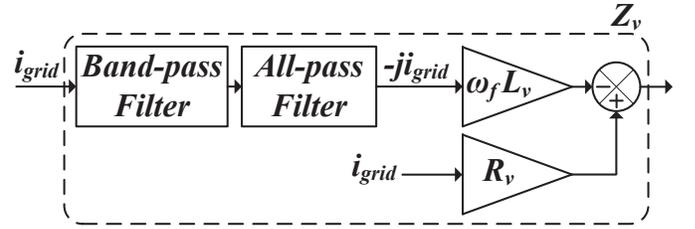


Fig. 4. Block diagram of the proposed virtual impedance method.

where ζ and ω_f denote damping ratio and fundamental angular frequency, respectively. When the grid current of fundamental frequency is filtered by the all-pass filter, it represents the pure imaginary value as shown in Fig. 4. Thus, the voltage drop

TABLE I: Parameters of the VSC (See Fig. 1)

Parameter	Value
Grid Voltage (rms)	120 V
Grid Frequency	60 Hz
Sampling Frequency	15 kHz
V_{DC}	200 V
L_g, R_g	1.0 mH, 0.2 Ω
L_i, R_i	1.0 mH, 0.2 Ω
C_f, R_d	10 μ H, 10 Ω
C_{DC}	2400 μ F
R_{load}	44.0 Ω
L_{grid}, R_{grid}	5.0 mH, 0.2 Ω
L_v, R_v	2.0 mH, 0.0 Ω

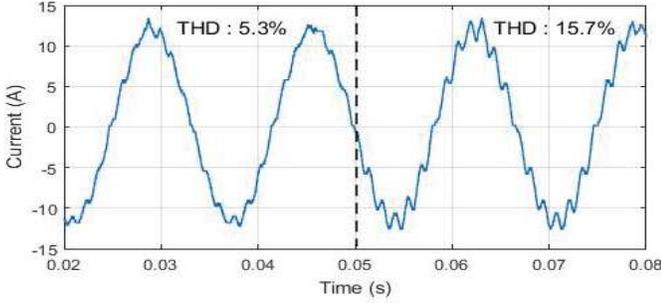


Fig. 5. Instability phenomenon of the 13th harmonic compensator of the conventional single-loop current controller.

across the virtual inductance is generated by multiplying the reactance of the virtual impedance to the output of the all-pass filter. The band-pass filter is used to get pure fundamental component of the grid current. The virtual resistance can also be implemented in the straightforward manner shown in Fig. 4. Finally, the voltage drop across the virtual impedance is subtracted from the output of the grid current controller to modify the reference of the capacitor voltage.

In addition to the feed forward of the voltage drop of the virtual impedance, the proportional and integral gains of the grid current controller and the capacitor voltage controller should be updated. The L_g and R_g of (4), (5), (8), (10), and (11) need to be replaced by $L_g + L_v$ and $R_g + R_v$. The gains of the current controller can be updated directly by the replacement. The capacitor voltage controller can be redesigned with the updated G_i and G_{pcc} .

IV. EXPERIMENTAL RESULTS

The performance of the HHC and the virtual impedance method are verified experimentally with a 1 kW single-phase VSC shown in Fig. 1. The controllers of the VSC is developed on TMS320F28335 DSP. The power spectrum analyzer, YOKOGAWA WT3000, is used to analyze the current harmonics. The detailed parameters of the VSC are listed in Table I. The L_{grid} and R_{grid} denote an inductor for changing the grid impedance. The grid inductor was not connected for the experiments of the harmonic compensation to show the attenuation performance with lower inductance. It is used for verifying the virtual impedance method.

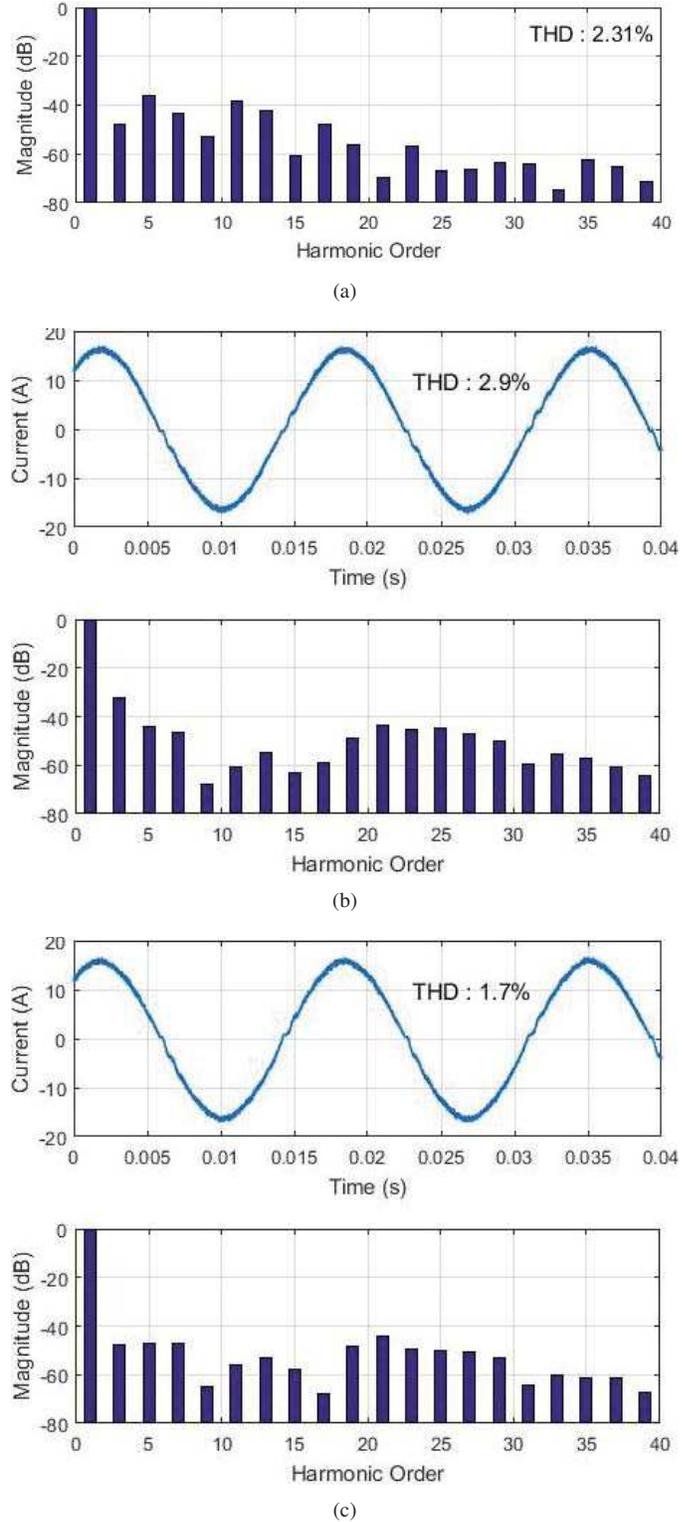


Fig. 6. (a) THD analysis of the PCC voltage. (b) Grid current waveform and THD analysis for the HVC in the multi-loop controller. (c) Grid current waveform and THD analysis for the HCC+HVC in the multi-loop controller.

In the following experiments, the magnitude of the grid current reference is generated by a DC-link voltage controller and the phase of it is synchronized to the PCC voltage for

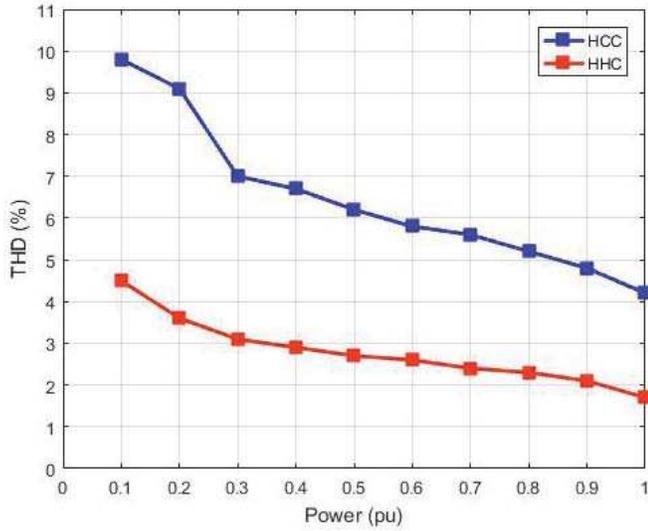


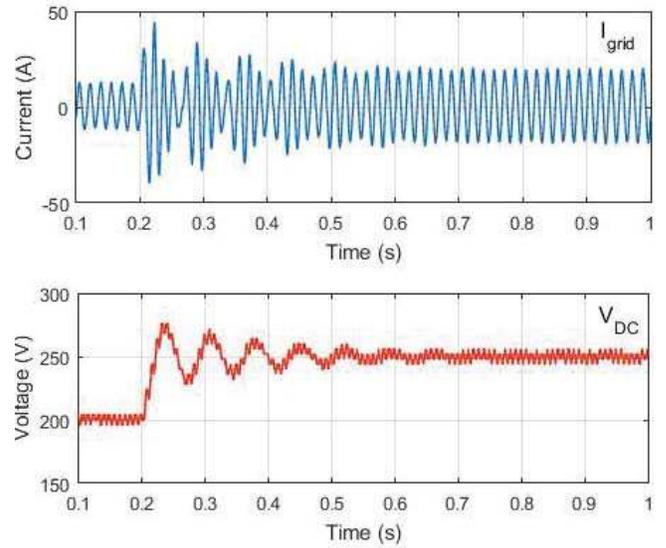
Fig. 7. THD of the HCC and the HHC according to different output power of the converter.

unity power factor operation.

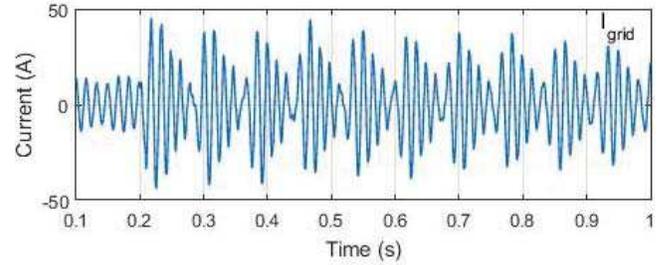
The instability phenomenon of the conventional HCCs of the single-loop controller is shown in Fig. 5. At 0.05 s, the 13th HCC is turned-on which results in undesired amplification of the 13th harmonics due to its not enough phase margin. This coincides with the analysis in Fig. 3(a).

On the contrary, the HVCs of the proposed multi-loop controller can be embedded up to 23rd harmonics. However, adding a HVC at a certain harmonic frequency affects also harmonics at nearby frequencies and can even amplify them. Moreover, admissible harmonic currents limited by IEEE Std 519-1992 decreases as harmonic frequency increases. Thus, to prevent the harmonic currents near 23rd frequency from being amplified, HVCs up to 17th harmonics are selected. In Fig. 6(b), the grid current is shown and its harmonics are analyzed when only HVCs are used in the multi-loop controller. Although the result is better than the case shown in Fig. 5, the 3rd and 5th harmonics are not attenuated enough. Therefore, the 3rd and 5th HCCs are added for further suppression, which is called the hybrid harmonic compensation (HHC) in this paper. In Fig. 6(c), it is shown that all harmonic components are attenuated more than 40 dB. Although not applied in this paper, note that the time delay compensation in [14] can increase the stability of the HCs and allow harmonics reduction at even higher frequencies. The improved resonant controllers in [8] can also be used selectively with the proposed HHC. It is shown in this paper that the proposed HHC has better stability and attenuation capability than using only HCCs or only HVCs. The multi-loop controller is also provided as a structure in which the HHC can be embedded.

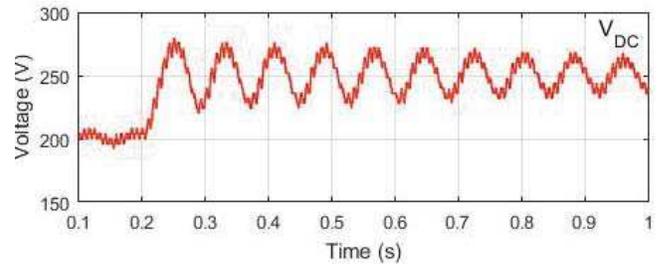
In Fig. 7, the THD of the HCC and the HHC is compared at different output power of the converter. The HCC is implemented with the conventional single-loop controller and



(a)



(b)



(c)

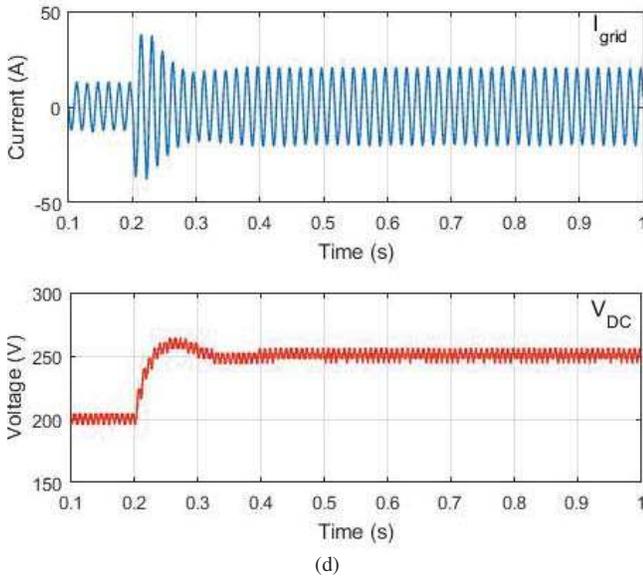


Fig. 8. The step responses of the DC-link voltage and the grid current. (a) Without Z_{grid} . (b) With Z_{grid} . (c) With Z_{grid} and only the feed forward of the virtual impedance method. (d) With Z_{grid} and the whole virtual impedance method.

the HHC with the proposed multi-loop controller. The integral gain of the HCs of the HCC and the HHC are not changed according to the operating points. Overall, the THD of the HCC is higher than that of the HHC since the HCs of the HCC are used only up to 11th harmonics while the HCs of the HHC are used up to 17th harmonics. It should be noted that the THD variation of the HHC according to the load is smaller than that of the HCC. The HHC is more robust to the variation of the operating point of the converter.

The proposed virtual impedance method for the stability of the fundamental grid current is verified by analyzing step responses of the DC-link voltage and the grid current as shown in Fig. 8. At 0.2s, the reference of the DC-link voltage is changed from 200 V to 250 V. In Fig. 8(a), the step responses are shown when the grid inductor, Z_{grid} , is not connected. There is oscillation that lasts for roughly 0.4 s. The oscillation is worse if the grid inductor is inserted in the circuit as shown in Fig. 8(b). The effectiveness of the virtual impedance method are shown in Fig. 8(c) and Fig. 8(d). The virtual resistance is set to zero to focus on the virtual inductance which is the main challenge as mentioned in the previous section. Firstly, to validate the feed forward of the voltage drop across the virtual inductance, the proportional gain of the grid current controller is not updated and results are shown in Fig. 8(c). It can be seen that the oscillation is reduced compared to the one in Fig. 8(b). Finally, in Fig. 8(d), results are depicted when the proportional gain is updated also. The oscillation is now almost removed and the DC-link voltage settles to 250 V in about 0.1 s.

V. CONCLUSION

A multi-loop controller for LCL-filtered grid-connected VSCs is proposed in this paper which is integrated with a hybrid harmonic compensation scheme and a novel virtual impedance method. The design criteria of the proportional and integral gains of the multi-loop controller is provided. The HVCs of the multi-loop controller are proved to have better stability than the HCCs of the conventional single-loop controller both by simulations and experiments. Moreover, it is verified that using both the HCCs and HVCs in the multi-loop controller maximizes the attenuation performance. The effectiveness of the virtual impedance method to the fundamental grid current controller is shown by analyzing step responses. The virtual impedance method will be investigated more to see if it is effective also at harmonic frequencies and will be discussed in the future work.

REFERENCES

- [1] M. S. Munir, J. He, and Y. Li, "Comparative Analysis of Closed-Loop Current Control of Grid Connected Converter with LCL Filter," in *Electric Machines & Drives Conference (IEMDC)*, 2011 IEEE International, 15-18 May 2011, pp. 1641-1646.
- [2] J. He and Y.W. Li, "Generalized closed-loop control schemes with embedded virtual impedances for voltage source converters with LC or LCL filters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1850-1861, Apr. 2012.
- [3] P. C. Loh and D. G. Holmes, "Analysis of multiloop control strategies for LC/CL/LCL-filtered voltage-source and current-source inverters," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 644-654, Mar./Apr. 2005.
- [4] M. Castilla, J. Miret, and J. Matas, "Control design guideline for single-phase grid-connected photovoltaic inverters with damped resonant harmonic compensators," *IEEE Trans. Ind. Electron.*, vol.56, no. 11, pp. 4492-4501, Nov. 2009.
- [5] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," in *Proc. Inst. Elect. Eng. - Elect. Power Appl.*, vol. 153, no. 5, pp. 750-762, Sep. 2006.
- [6] J. He, Y. Li, and M. S. Munir, "A flexible harmonic control approach through voltage-controlled DG-grid interfacing converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 444-455, Jan. 2012.
- [7] A. G. Yepes, F. Freijedo, O. Lopez, and J. Gandoy, "High-performance digital resonant controllers implemented with two integrators," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 563-576, Feb. 2011.
- [8] Q. Qian, J. Xu, S. Xie, and L. Ji, "Analysis and improvement of harmonic quasi resonant control for LCL-filtered grid-connected inverters in weak grid," in *Proc. IEEE Appl. Power Electron. Conf. and Expo.*, 20-24 March. 2016, pp. 3446-3452.
- [9] J. M. Guerrero, L. G. Vicuna, J. Matas, M. Castilla, and J. Miret, "A wireless controller to enhance dynamic performance of parallel inverters in distributed generation systems," *IEEE Trans. Power Electron.*, vol. 19, pp. 1205-1213, Sep. 2004.
- [10] Y. W. Li and C. N. Kao, "An accurate power control strategy for power-electronics-interfaced distributed generation units operating in a low-voltage multibus microgrid," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2977-2988, Dec. 2009.
- [11] J. He and Y. W. Li, "Hybrid voltage and current control approach for DG-grid interfacing converters with LCL filters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1797-1809, May 2013.
- [12] S.-J. Lee, J.-K. Kang, and S.-K. Sul, "A new phase detecting method for power conversion systems considering distorted conditions in power system," in *Conf. Rec. 34th IEEE IAS Annu. Meeting*, Oct. 3-7, 1999, pp. 2167-2172.
- [13] H. J. Lee, S. Jung, and S. K. Sul, "A current controller design for current source inverter-fed AC machine drive system," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp.1366-1381, Mar. 2013.
- [14] H. Deng, R. Oruganti, and D. Srinivasan, "PWM methods to handle time delay in digital control of a UPS inverter," *IEEE Power Electron. Lett.*, vol. 3, no. 1, pp. 1-6, Mar. 2005.