Y9.FS1.1: SiC Power Devices for SST Applications

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1. Project Goals

(a) Design and fabrication of 10kV SiC MPS rectifiers for solid-state transformer operation at high temperatures.

(b) Characterization of 10kV SiC MOSFET for SST operation at high temperatures.

2. Role in Support of Strategic Plan

This project develops SiC high voltage (10kV) devices devices for the solid-state transformer and fault-interruption device applications within the FREEDM green energy hub. Our Year 9 goal is aligned to the road map for developing devices that have better high temperature performance.

3. Fundamental Research, Technological Barriers and Methodologies

The major technological barrier is the limitation of the semiconductor fabrication equipment in NNF (NCSU) and SMiF (Duke), some process steps need to be outsourced.

4. Achievements

10kV SiC MPS Rectifiers:

In previous years, the center has proposed a novel SiC MPS (Merged-PiN-Schottky) Rectifier for the solid-state transformer application to improve the trade-off between on-state and turn-off switching losses [1]. This reduces energy loss and improves the efficiency of the SST. The MPS rectifiers were successfully fabricated in Year 6 [2] and demonstrated to have much superior trade-off curves compared to available PiN and JBS rectifiers in the industry. The devices were characterized at high temperatures (up to 200°C) in Year 7 and 8 [4].

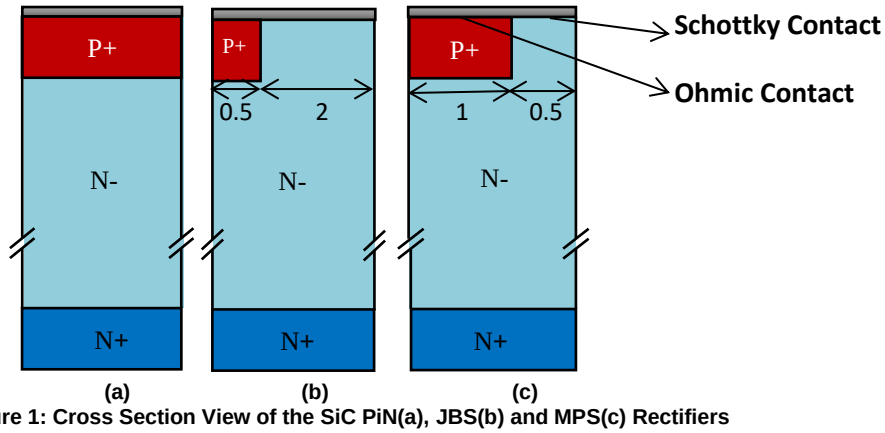

Figure 1: Cross Section View of the SiC PiN(a), JBS(b) and MPS(c) Rectifiers

Figure 1 shows the cross section view of the SiC PiN, JBS and MPS rectifiers. The structure of JBS and MPS rectifiers looks similar in that they both have P+ doped region to form potential barrier at reverse bias state, so that it can reduce electric field under the Schottky contact and to reduce leakage current. The difference between these two structures is that for JBS rectifier, the P+/N junction does not turn on at normal

operation state, so the Schottky contact region should be wide enough to lower on-state resistance. However, for MPS rectifier, the region under the Schottky contact should be very narrow so that the P+/N- junction can be turned on at normal operation state to reduce on-resistance.

One important process innovation achieved was to simultaneously make the Schottky contact to the N- SiC drift region and an Ohmic contact to the P+ regions. Fine features down to 1um were achieved, which is challenging for lithography at the university, as well as the lift-off process for metal deposition. This problem was finally solved by a new metal anneal process. It was found that when the Nickel was deposited and annealed at 850 ^{o}C, it has a high Schottky barrier height on N-type SiC and makes an Ohmic contact on P+ SiC at the same time. The Ohmic contact was also evaluated by TLM structures on wafer with P+ implanted surface, and the contact resistance is 1.4e4 Ωcm. The distribution of the Schottky barrier height extracted by the forward current voltage characteristics are shown in Figure 2a. Most of the test structures shows Schottky barrier height higher than 1.7 eV, and an excellent ideality factor of less than 1.1. A plot of ideality factors versus the barrier heights yields a straight line as shown in Figure 2b. An 'ideal' barrier height can be determined by extrapolating the line to n=1.0 according to [3]. It shows that the ideal barrier height is 1.8 eV. This high Schottky barrier height is beneficial for the operation of MPS rectifiers because the higher barrier will induce the injection of holes from the P+ region.

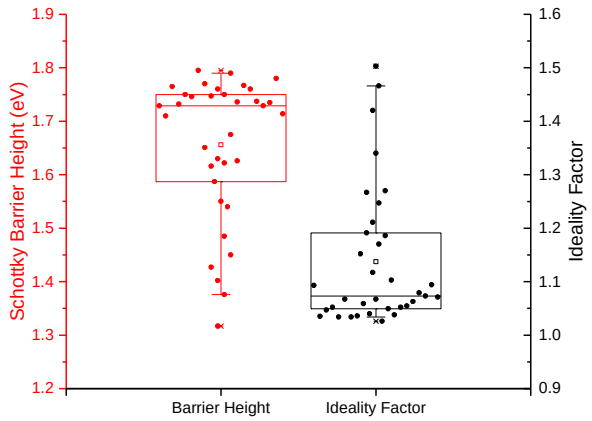

Fig. 2a: Distribution of extracted Schottky contact barrier height and ideality factor on wafer

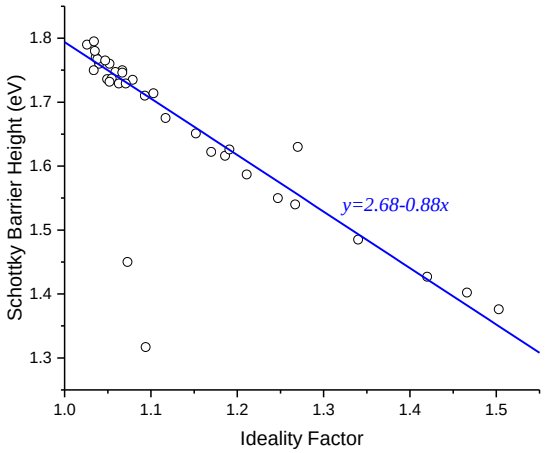

Fig. 2b: Relation between Schottky barrier height and ideality factor measured on wafer

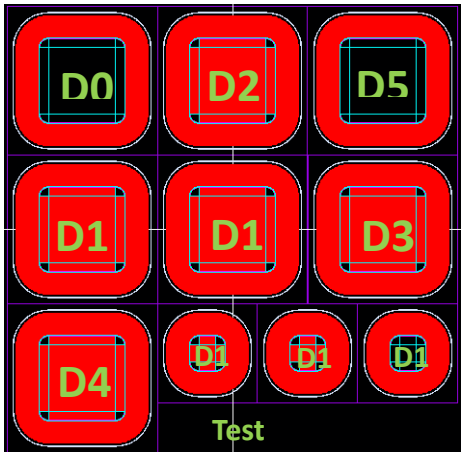

Fig. 3a: Mask layout for different device structures

Device Type	Ws(μm)	Wp(μm)
D0 (PiN)	0	-
D1 (MPS)	0.5	1.5
D2	1	1.5
D3	1.5	1.5
D4	2	1.5
D5 (SBD)	-	0

Fig. 3b: Schottky contact width (Ws) and Ohmic contact width (Wp) for various designs

For fabrication of 10-kV devices, a mask layout was designed as shown in Figure 3a. There are 7 big devices with active area of 6.68 mm^2 and 3 small devices with active area of 1.13 mm^2. The Schottky contact width were varied as shown in Figure 3b. The smallest half-cell width was 0.5 um for MPS structure.

The process flow defined bus us for the fabrication of the diodes is shown in Figure 4. SiC wafer was first etched to form the alignment mark, then the N+ channel stop ring was implanted, followed by the p+ ion implantation to form both the floating rings for edge termination and the p region in the active area. The oxide passivation was later formed by ALD oxide followed by RTA in 950 ^oC, and then PECVD oxide was deposited to increase the thickness. The backside Ohmic metal was formed by Nickel deposition and annealed at 950 ^oC for 2 mins. Nickel was then deposited at the front side contact metal to form both the Ohmic contact and Schottky contact as previously stated. Thick metal and polyimide was deposited to complete the device structure.

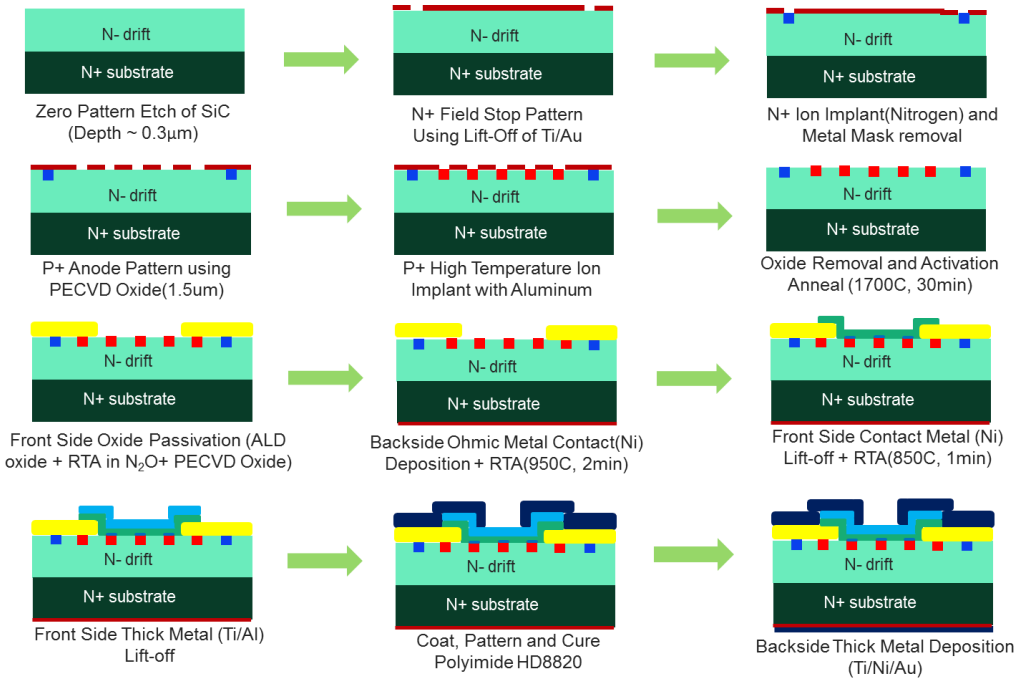

Fig. 4: Process flow of fabricating the 10kV MPS diode

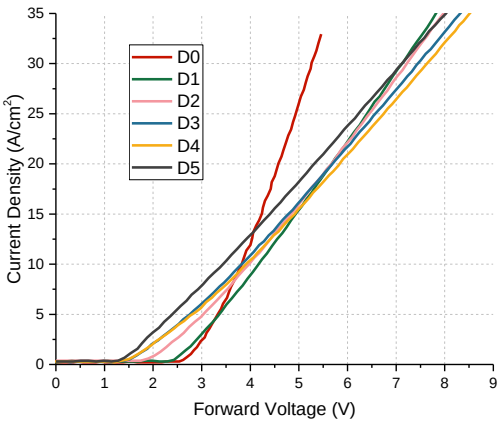

Fig. 5a: Forward IV of different types of diodes at room temperature.

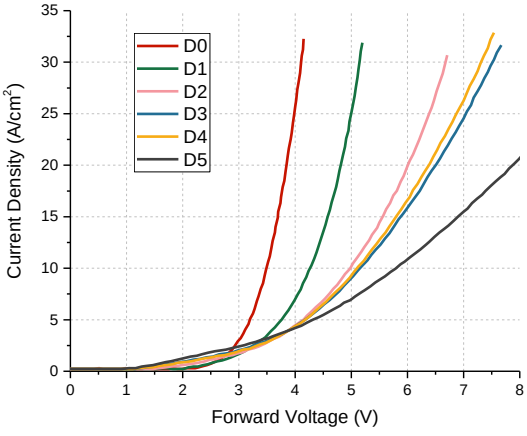

Fig. 5b: Forward IV of different types of diodes at 150 ^oC

The forward and reverse characteristics of the devices fabricated on the wafer are shown in Fig. 5 at room temperature and 150 ^{o}C. At room temperature, the knee voltage increases with narrower Schottky contact cell width (Ws) for the JBS rectifiers. When Ws = 0.5 µm, the knee voltage was close to that of the PiN diode (D0). Significant injection from the P-N junction was not observed at room temperature for all the MPS devices. However, injection from the P-N junction was clearly observed for MPS rectifiers when the temperature was increased to 150 ^{o}C (Fig. 5b). Fig. 6 shows the measured forward voltage drop at 20 A/cm^2 with increasing temperature. The forward voltage drop for D0 (JBS rectifier) increases with increasing temperature up to 150 ^{o}C. In contrast, the on-state voltage drop of the PiN and MPS rectifiers decreases with temperature as previously reported [4].

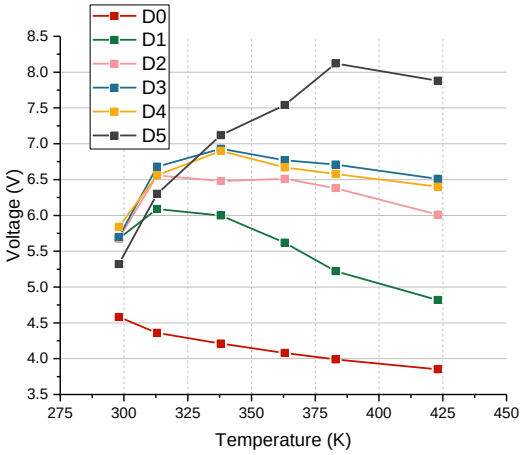

Fig. 6: Forward voltage of different types of diodes at 20A/cm^2 at different temperatures

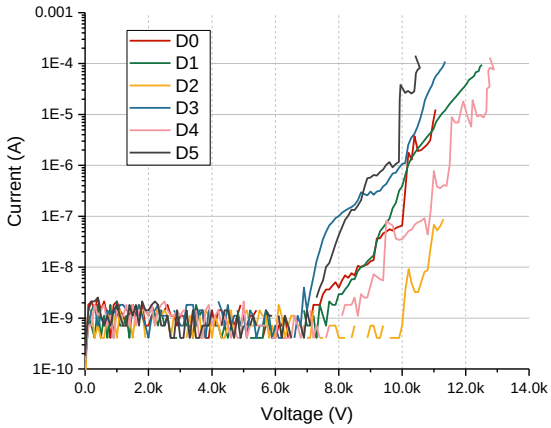

Fig. 7: Reverse IV of different types of diodes with active area 6.68mm^2 at room temperature

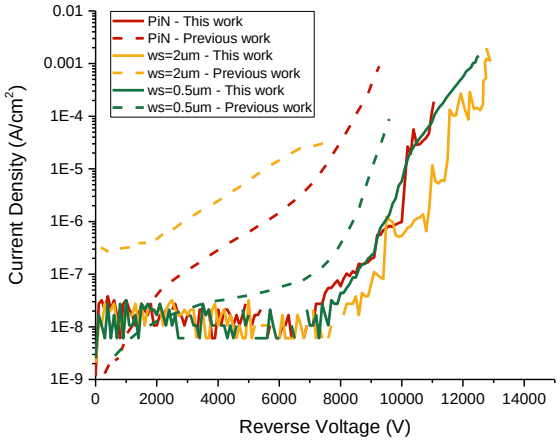

Fig. 8: Reverse IV for different types of devices compared to previous work in the center

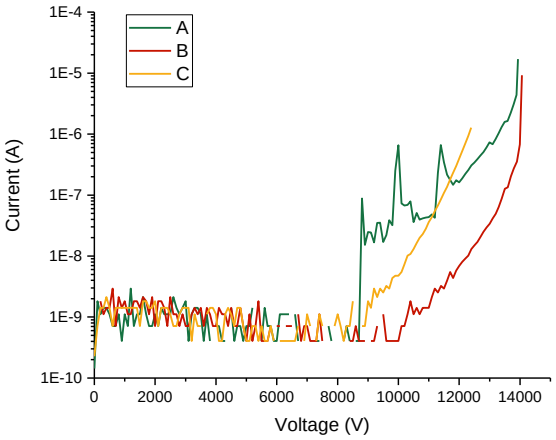

Fig. 9: Reverse IV of MPS with small active area (1.13 mm^2)

Figure 7 shows the reverse I-V for different types of devices with large area. A much lower leakage current and higher BV was achieved compared to previous results (Fig. 8) in Year 8. For the new devices, there was no significant leakage current difference for different structures, and even the SBD (D5) has a very low leakage current due to the high SBH and improved quality of the passivation oxide. In the previous Year-8 work, Schottky barrier height was 0.89 eV with ideality factor of 2.4. Our Year-9 work shows better quality for the Schottky contact. The reverse IV of small devices on wafer (Figure 9) shows higher breakdown

voltage probably due to less material defects, and the highest breakdown voltage goes above 14kV. We plan to package the devices for testing of the reverse recovery performance as a function of temperature.

10kV SiC Power MOSFETS:

Previously, 1.2kV SiC MOSFETs were characterized to high temperature in Year 8 [6]. In Year 9, the 10kV SiC MOSFET was characterized at high temperature up to 225 ^{o}C. Figure 10a shows the test circuit board for Ciss, Crss and Coss test, along with driver circuit for switching test and Qg test. The test set up with thermal plate to raise the operating temperature is shown in Figure 10b.

Fig. 10a: Test circuit board for the characterization of SiC MOSFET

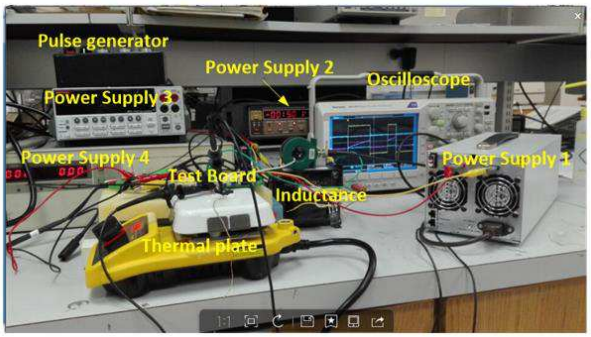

Fig. 10b: Test setup for the high temperature characterization of 10kV SiC MOSFET

Figure 11 shows the measured leakage current of the 10kV MOSFET at different temperature. The leakage current increases significantly when temperature increases above 150 ^{o}C. Figure 12 shows the output characteristics of the 10kV SiC MOSFET at selected temperatures. The On-Resistance increases with temperature due to reduction of the bulk and channel mobility with increasing temperature.

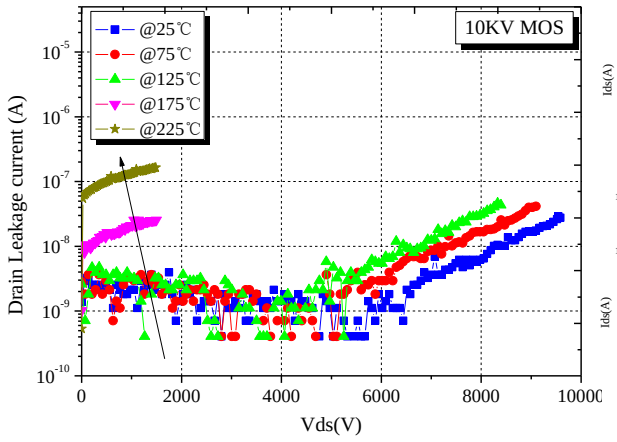

Fig. 11: Off-State drain leakage current of SiC MOSFET at different temperature

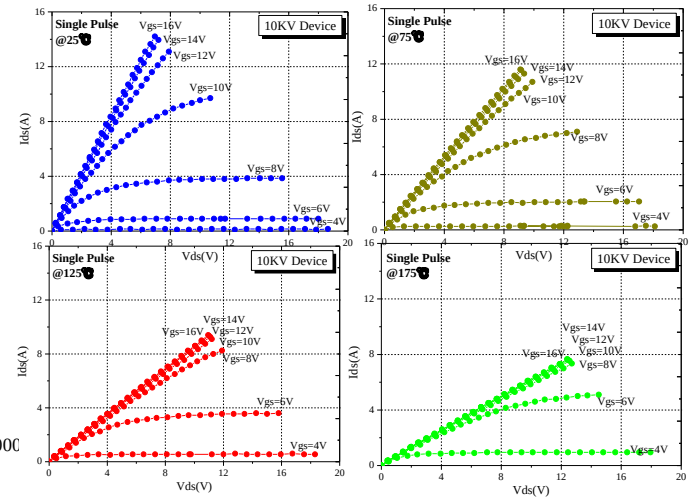

Fig. 12: Output characteristics of 10kV SiC MOSFET at different temperature

Figure 13 shows that the transfer characteristics at various temperatures. The threshold voltage decreases with increasing temperature as shown in Fig. 14 due to the increase of intrinsic carrier concentration. Fig.14 shows the on-resistance (Rdson) at different Vgs. It is worth to notice that when gate voltage is as small as 4V, the Rdson decreases with increasing temperature, because the channel mobility is increasing with increasing temperature due to traps at the SiO_2/SiC interface, and the channel resistance has a big impact on the total resistance when the gate bias is small.

Figure 15 shows the device capacitance Coss with Vds at different temperature, which shows that temperature does not influence the output capacitance as expected. The gate charge waveform also shows that temperature does not have a big impact on gate charge. The turn-on and off waveforms have a weak dependence on temperature based on Figure 17 and 18.

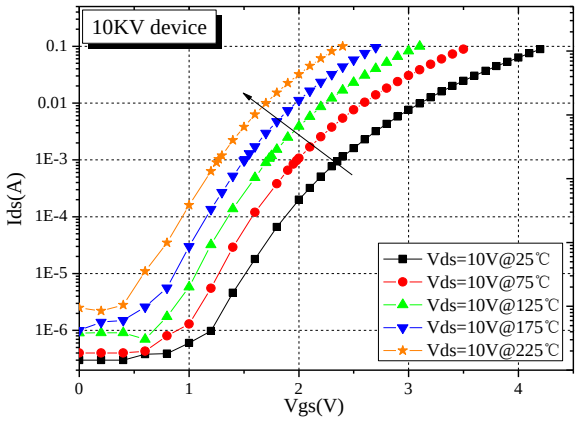

Fig. 13: transfer characteristic of SiC MOSFET at different temperature

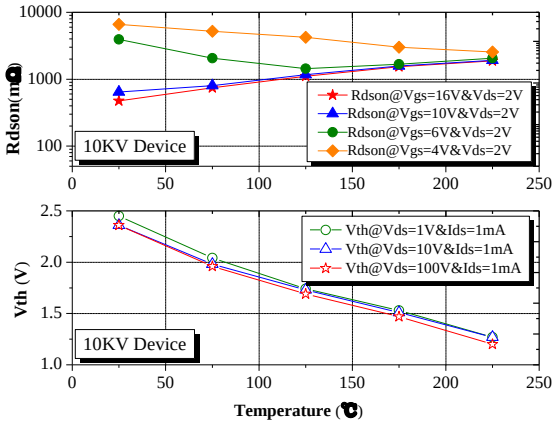

Fig. 14: Temperature dependence of Rds on at different gate bias and Vth at different Vds

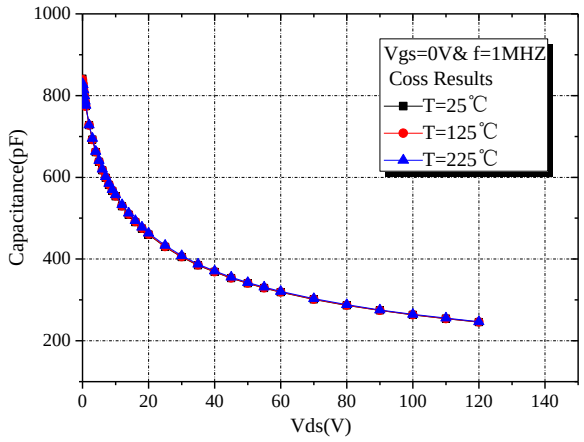

Fig. 15: Capacitance versus Vds at different temperature

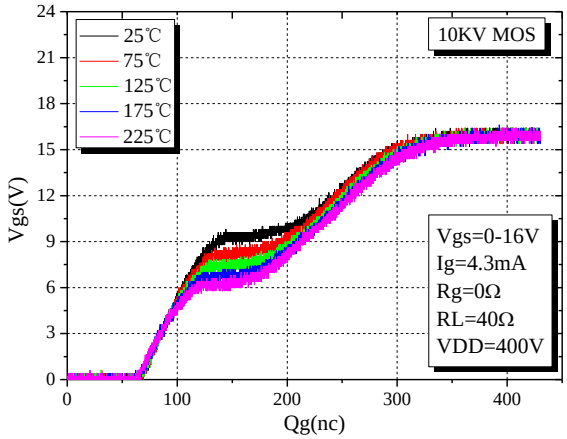

Fig. 16: Gate charge waveforms of SiC MOSFET at different temperature

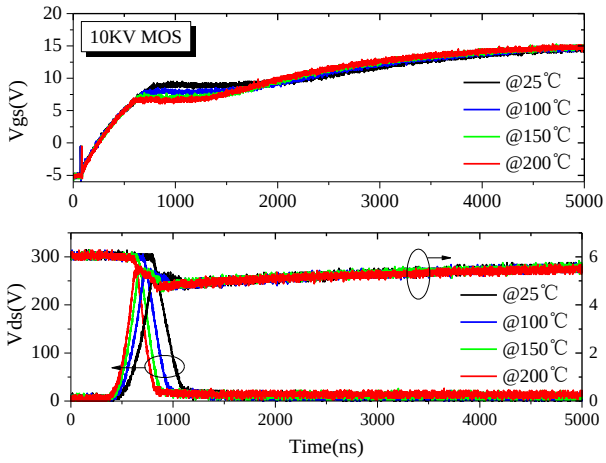

Fig. 17: Turn on waveform of Vgs, Vds, ids with time at different temperature

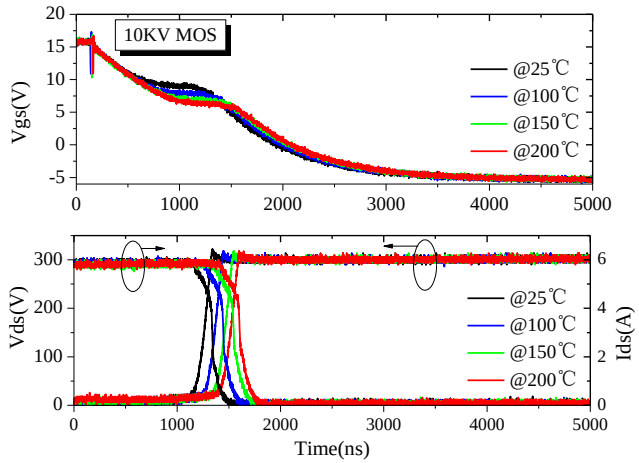

Fig. 18: Turn off waveform of Vgs, Vds, ids with time at different temperature

5. Other Relevant Work Being Conducted Within and Outside of the ERC

To the Center's knowledge, there was no other research activity is being directed towards making 10kV 4H-SiC MPS rectifiers until recently Dr. Kimoto's group demonstrated their SiC hybrid MPS diode [5]. The difference of their structure compared to ours is that they put PiN diode and JBS diode in one cell. The P region of the PiN diode is made by epitaxial growth, which will increase the lifetime for the PiN mode and have lower forward voltage. One disadvantage of their structure is that the current distribution will not be uniform, which may not have good thermal performance compared to our structure.

6. Milestones and Deliverables

In year 9, the 10kV SiC MPS rectifiers has been fabricated and shown better performance with smaller leakage current. The device will be packaged and tested for dynamic performance at high temperature up to 200 ^{o}C. Major milestone was met by achieving a large Schottky barrier height.

The 10kV SiC MOSFET has been characterized up to 225 ^{o}C. The output characteristics, transfer characteristics, capacitance test, Qg test and the switching characteristics have been tested at various temperature. Major milestone was met by complete characterization of the 10kV SiC power MOSFETs at high temperatures.

7. Plans for Next Five Years

Contingent on availability of funds, the PSD group will continue developing SiC high voltage devices, including rectifiers and transistors, for SST and FID application.

8. Member Company Benefits

This project will allow member companies to assess if high voltage SiC MPS rectifiers are attractive commercial products.

9. References

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[2] Edward Van Brunt, "Development of Optimal 4H-SiC Bipolar Power Diodes for High Voltage High-Frequency Applications" PhD Thesis, North Carolina State University, 2013

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[4] Yifan Jiang, Woongje Sung, Xiaoqing Song, Haotao Ke, Siyang Liu, B.Jayant Baliga, Alex Q.Huang and Edward Van Brunt, "10kV SiC MPS Diodes for High Temperature Applications", Proceedings of 28th ISPSD, Prague, Czech Republic, 2016

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