Y9.FS1.2.1: GaN Low Voltage Power Device Development

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1. Project Goals

The overall objective of the GaN power device project is to fabricate and demonstrate high performance rectifier and/or transistor for the solid state transformer (SST) and distributed storage devices (DESD) with 600V~1200V voltage blocking capability, and specific Ron of 1~2mΩ-cm^2. The specific goals for this year are:

- Design and fabricate 1200V GaN vertical power rectifier on free-standing GaN substrate. Evaluation of Lateral GaN HFET at high temperature

2. Role in Support of Strategic Plan

The proposed FREEDM 20KVA solid state transformer (SST) converts the high voltage (7kV) input to the low voltage (120V) output at a switching frequency of 10 KHz. The secondary side of the SST needs medium voltage (600V), high current (100A) power devices. In order to achieve extremely high SST efficiency (>97%), power losses should be minimized. For this purpose wide band gap GaN-based power devices will be implemented due to the superior physical properties of the GaN materials relative to Si. GaN is also superior to SiC based on many measured critical field in the range of 3 to 3.3 MV/cm, which is higher than the reported critical field for SiC. This project is important for the fundamental research in developing new devices/device structures based on new material, and also directly support the SST and DESD thrusts.

3. Fundamental Research, Technological Barriers and Methodologies

At the beginning of the center research program, due to the lack of GaN free-standing substrate/epi wafers, lateral GaN power devices have been the focus of the center and many other research groups worldwide. Nowadays many commercial lateral GaN HFETs are introduced. With high electron mobility (~2000cm^2/V-s) channel and high critical field, lateral GaN power transistor can deliver roughly two times current density[1] (2.4A/mm^2 vs 1.4A/mm^2) as that of latest Si vertical power device at 650V class. This transfer to half die size with same on-state current capability. And lateral GaN power transistor also demonstrate fast switch speed due to low inherent capacitance, this is favorable to design GaN based power converter to operate at MHz level switch frequency. However, due to the lateral device structure, lateral GaN will have limited opportunity to be competitive in higher voltages when compared with many exciting and future SiC vertical power devices. Therefore there is a strong need to develop vertical GaN power devices.

Recently high quality free-standing GaN substrate prepared by HVPE method are commercially available with a wafer size of 2 inch. This is similar to the situation of SiC about 10 years ago. The cost is reasonable for early stage R&D, to study GaN power device with vertical architecture, explore the challenge and opportunity for GaN community from scientific merit point of view. In year eight, we started the initiative to study 1200V class GaN power rectifier with vertical current conduction. The first major challenge is to form a vertical power device with good blocking capability. To address this issue, a variety of edge termination based on JTE and floating ring techniques will be designed to support high voltage blocking capability, and three type of rectifier (simple Schottky, junction barrier Schottky, and PIN diode) will be designed to trade-off forward R_{on} with reverse leakage current. Junction termination require the

[1] Yole Development, "SiC and GaN devices for the power electronic market" 2017 January, Webcast.

use of P type layer and currently there is very limited literature or successful results on how to form PN junction by implantation. Other groups have made vertical power devices based on MOCVD growth of the P layer. Therefore how to form the p layer by implantation represents a major challenge as well as opportunity for our research in Year 9.

4. Achievements

4.1 100V, 650V Class GaN Power Transistor Characterization at Elevated Temperature

100V and 650V GaN power transistors from GaN systems have been evaluated from room temperature to150°C. And Figure 1 lists temperature impact on major device parameters and switch performance. The on-state resistance increased substantially at high temperature ($R_{150°C}/R_{25°C}$=2.25 for 650V device, 1.73 for 100V device), this on-state resistance degradation is caused by the reduction of electron mobility at channel region due to polar optical phonon scattering effect, while the different temperature coefficient for two devices is due to the percentages of on-resistance distribution. While the temperature on threshold voltage on both devices are not so consistent. Fig. 1c) show gate charging data, the plateau gate voltage is 2.64V for 650V device, 1.20V for 100V device. As device junction temperature goes higher, gate voltage reach plateau voltage earlier and the plateau region become wider, so Qgs reduced and Qgd increased with higher temperature, also the total gate charges were higher with increasing test temperature. Fig. 1d) show timing and loss result based on double pulse switch tests on 650V devices, As temperature goes up, the rise time and turn-on delay show almost constant (23.67ns, 10.53ns), fall time reduced from 76ns to 65.2ns, and turn-off delay time reduced from 59.2ns to 41.6ns, this transfer to nearly constant turn-on loss (3.42µJ), turn-off loss decreased from 13.52µJ at room temperature to 10.68µJ at 150°C. Those results point out GaN lateral power transistor is favored for high temperature and high frequency operation. A paper has been presented at WiPDA 2016.

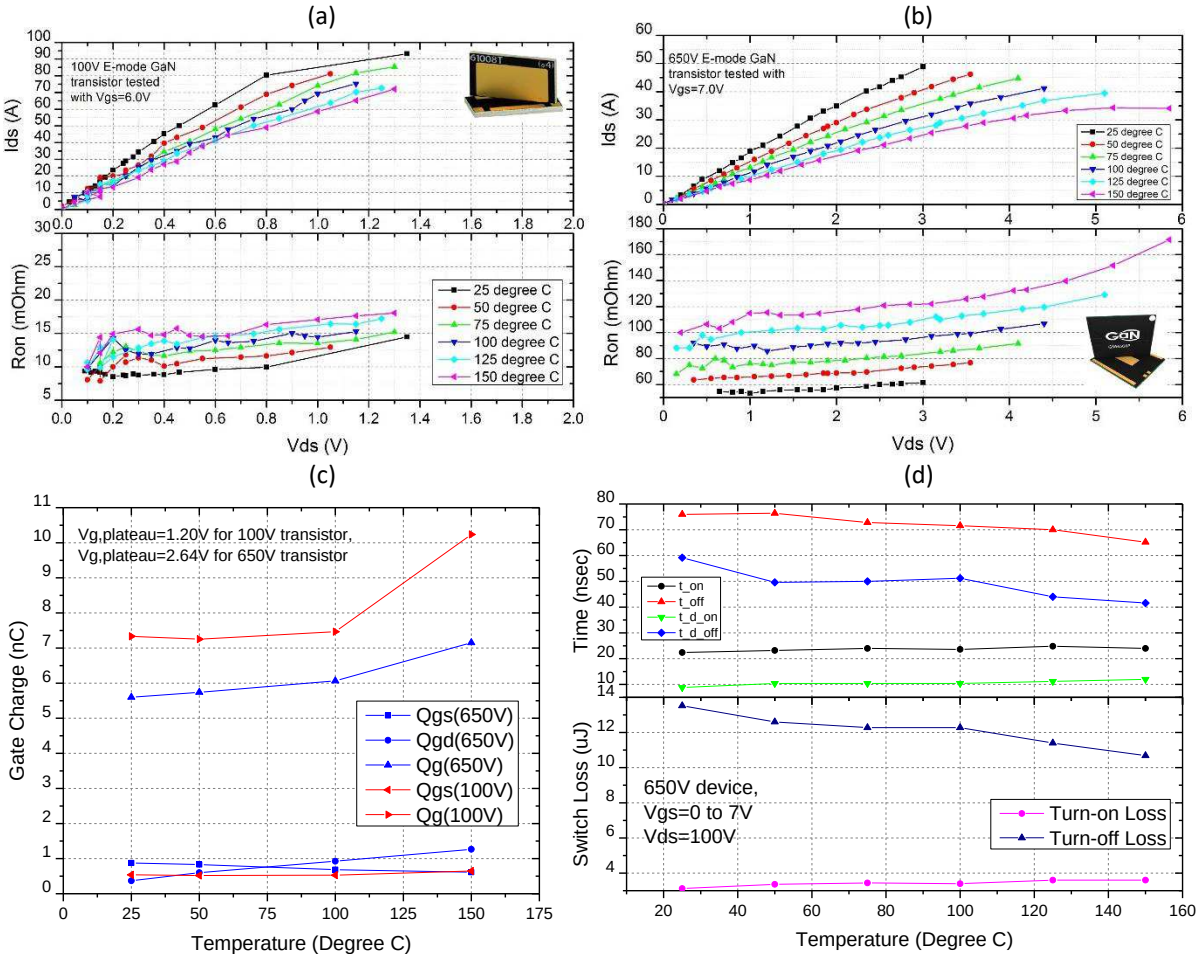

Figure 1. (a) 100V GaN transistor Id-Vd and On-resistance with Vgs=7.0V at different temperatures, (b) 650V GaN transistor Id-Vd and On-resistance with Vgs=7.0V under different temperature, (c) Temperature impact on gate charge for both 100V, (d) 650V transistor switching time and switch loss under different temperature.

4.2 Vertical GaN Power Rectifier with Magnesium Ion Implanted at Elevated Temperature:

We have successfully designed, fabricated and characterized the first vertical GaN power rectifiers developed at FREEDM. Three type of GaN power rectifiers with different edge termination and anode cell pitch were designed. A process flow was created for the device fabrication in university cleanroom environment. Magnesium ion implantation at elevated temperature was employed to form power rectifier and control electrical field distribution, after depositing Ni/Au as Schottky metal, we have evaluated the reverse bias performance of fabricated samples. Not only most of those PIN rectifier can support >1100V, but also the JBS rectifier reverse leakage vary across different Mg+ implant width design, the JBS with optimized design can deliver similar reverse performance as that of PIN diode. This is very interesting and exciting results as our fabrication does not involve any post implant activation process, which is still a big technical challenge. Now the backside Ohmic contact process is on-going, we hope to finish the backend process and extract forward I-V characteristic in spring 2017. Those results will be summarized to report at the site visit.

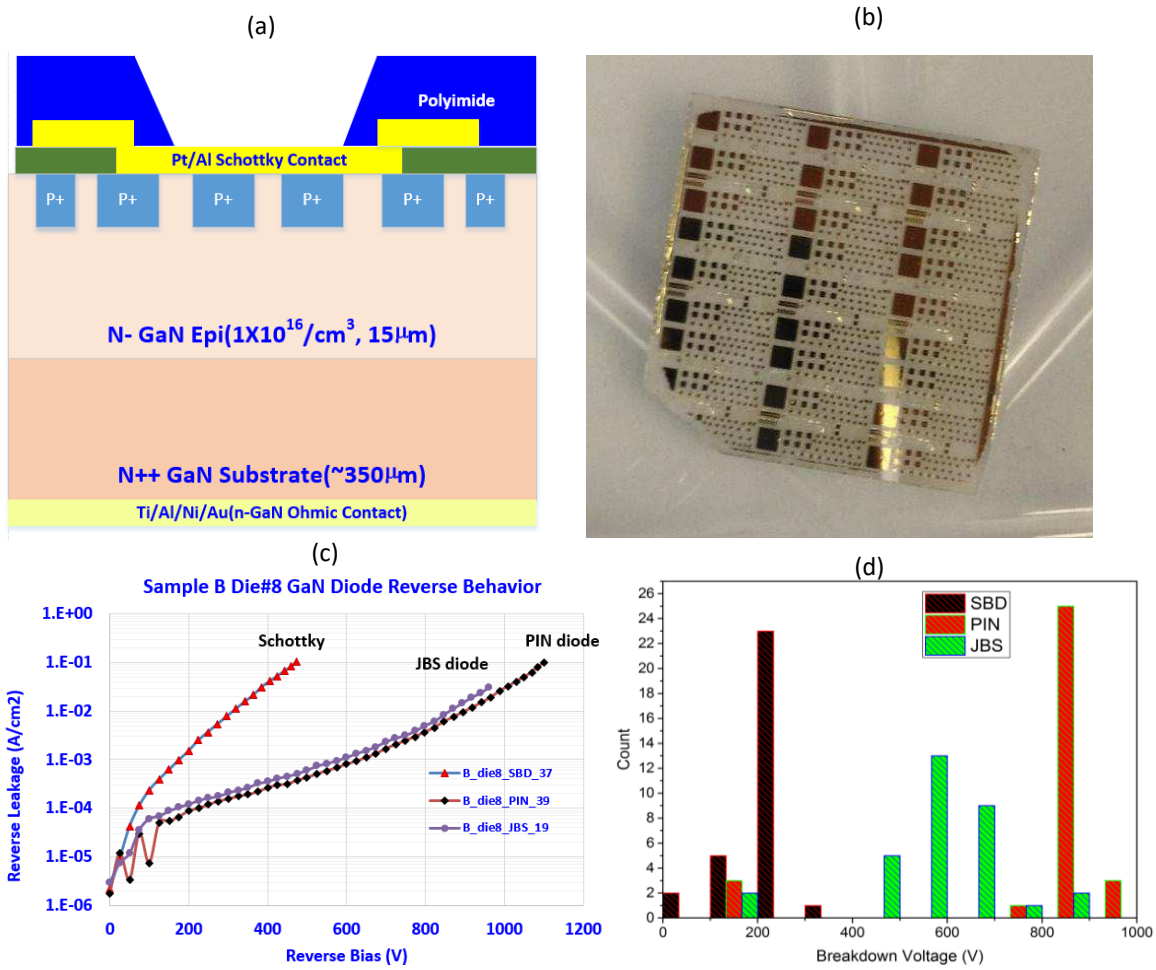

Figure 2. (a) Vertical GaN junction barrier Schottky (JBS) schematic diagram. (b) Optical image of fabricated 5mm x 5mm GaN free-standing sample. (c) Reverse bias performance for three type of GaN rectifier with circular anode electrode with 120μm in diameter. (d) Breakdown statistics histogram of fabricated GaN power rectifier when BV criteria is set as leakage <10mA/cm^2.

5. Other Relevant Work Being Conducted Within and Outside of the ERC

No other related projects are underway at the center schools. Outside the center, many groups on working on vertical GaN power devices and the P layers are formed by MOCVD. Our approach is novel and more competitive in commercial production of the device in the future.

6. Milestones and Deliverables

GaN vertical JBS power rectifier with breakdown voltage >1200V.

7. Plans for Next Five Years

With the successfully demonstrating GaN vertical power rectifier, in the long term, the team will continue to explore the GaN power device with vertical architecture, to design with new device structure to realize the full potential of the GaN material. Since 2014 we have built good relation with Nissin on elevated temperature implantation, we also can access GaN epitaxial, high temperature high pressure annealing facility, and other RTA process, all those support and collaboration from industrial and academy worldwide give us great flexibility on GaN power device research.

In this year, the team will focus on finish GaN power rectifier fabrication and characterization, try to make another wafer run with optimized fabrication process, finally, we plan to deliver a 1mm x 1mm size power rectifier with 1200V voltage blocking capability to package, evaluate and demonstrate its superior performance at circuit level.

8. Member Company Benefits

No member companies are involved in this project.

9. References (Published after last report)

1. Wang, Sizhen, Fei Xue, Alex Q. Huang, and Siyang Liu. "Physics understanding of high temperature behavior of Gallium Nitride power transistor." In *Wide Bandgap Power Devices and Applications (WiPDA), 2016 IEEE 4th Workshop on*, pp. 324-327. IEEE, 2016.