Y9.FS1.2.2: GaN Low Voltage Power Device Development

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1. Project Goals

The overall objective of the GaN power device project is to fabricate and demonstrate normally-off Metal-Oxide-Semiconductor (MOS) GaN/AlGaN High Electron Mobility Transistors (HEMTs) power devices for the solid state transformer (SST) and distributed storage devices (DESD) having 600V of blocking voltage characteristics and 50-Ampere current capability with a specific on resistance of 1-2 mohm-cm^2. The specific goals for this year are 1) to fabricate vertical power GaN devices, 2) to initiate 1200V GaN devices fabrication, and 3) to evaluate device reliability at elevated temperatures.

2. Role in Support of Strategic Plan

The proposed FREEDM 20KVA solid state transformer (SST) converts the high voltage (7kV) input to the low voltage (120V) output at a switching frequency of 10 KHz. The secondary side of the SST needs medium voltage (600V), high current (100A) power devices. In order to achieve extremely high SST efficiency (>97%) power loss should be minimized. For this purpose wide band gap GaN-based power devices will be implemented due to the superior physical properties of the GaN materials relative to Si. This project is critical to enabling SST and directly supports the strategic plan of the SST and DESD thrusts.

3. Fundamental Research, Technological Barriers and Methodologies

Due to basic epi material availability, today's GaN power devices are fabricated using lateral device structure. Lateral GaN HFET devices have very low parasitic capacitance therefore are very suitable for high speed applications. In terms of conduction losses, GaN device is about two time worse than vertical devices due to larger device cell size, lateral current flowing pattern (heat concentrated with the top 1um of a 500um wafer) and poor thermal performance when compared with SiC MOSFET. Therefore, a large die size is needed to reach high current levels in a single die. In addition, the quality of dielectric can lead the reliability and stability issues such as device threshold voltage instability or AC-DC dynamic dispersion that should be addressed. These have been major challenges facing the GaN research in the last few years.

To address above issues, we are shifting our strategy to the following two aspects: 1) focusing on medium current level devices such as 5A and 2) focusing on scientific merit contribution to the GaN community by studying high temperature device reliability and stability. The gate dielectric is an important component and we proposed and studied high-k and low-k dielectrics by using atomic layer deposition. By using an atomic layer deposited (ALD) SiO_2 tunnel dielectric and a high-k blocking dielectric low leakage, high performance, normally-off GaN devices are realized. The team has used the atomic layer deposition (ALD) technique to evaluate several high-k dielectrics (HfO_2 and Al_2O_3), low-k dielectric (SiO_2), or their alloys (HfAlO, $HfSiO_x$) in order to achieve a reliable and stable GaN device characteristics so that it will be delivered to the Center for the secondary side of SST. Lateral HFET devices suffer from large current handling capability relative to the die size.

4. Achievements

<u>4.1 Dielectric stability and reliability evaluation</u>

Reliability and V_T stability issues are one of the biggest concerns for GaN based power devices. In Y8, we characterized high temperature MOSHFET DC static behaviors. In Y9, our focus shifted more on studying

high temperature reliability aspects and finding ways to improve the same. For instance, we tested threshold voltage variance at 150°C and concluded that threshold voltage shift, ΔV_T, was found ~1V when MOSHFET with 30nm ALD SiO_2 gate dielectric was stressed up to 1000s duration, in on-state, with V_{DS}=0.1V and V_{GS}=V_T+7.5V. No change was observed in the gate leakage current. V_T shift may be due to the charge redistribution or interface degradation. A further optimized gate dielectric should help narrow V_T shift to less than 0.5V.

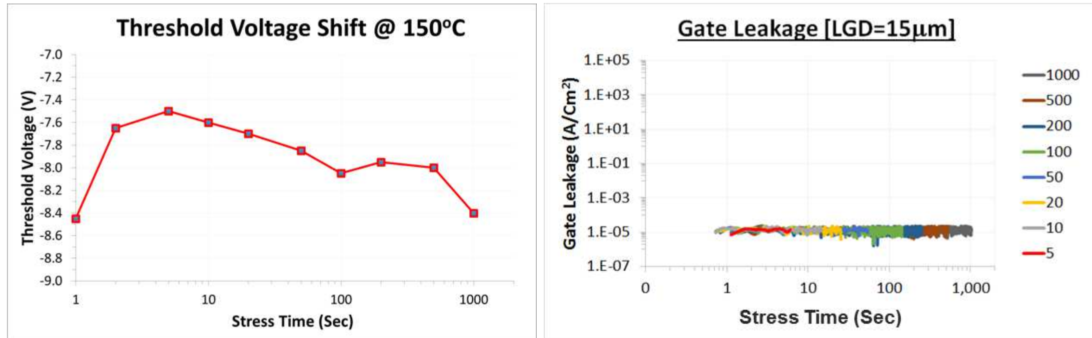

Figure 1. Threshold voltage shift at 150C & gate leakage of a GaN MOSHFET with 30nm ALD SiO_2

We have also evaluated the reliability of high-k dielectric in Y9 as we have seen better performance in terms of VT shift and hysteresis. In order to further improve reliability of high-k dielectric, we modified ALD deposition condition where ALD oxidants (ozone or water) is a variable and studied effect on various DC static characteristics. Despite having the same physical oxide thickness (20nm ALD HFO_2) and thermal budget (600°C post deposition anneal), incorporation of ozone resulted in a lower specific on-resistance (value extracted from linear portion of I_D-V_D curve of a MOSHFET at V_{GS}=V_T+3V, area = 9.5x10^{-6} cm^2 including 2µm source and drain, L_{GD}=10µm) and a much lower V_T shift compared to an HFET that would typically have a V_T~3V. Devices with ozone as an oxidant also showed orders of magnitude lower drain and gate leakage (Table 4B).

Table 1. DC I-V characteristics extracted from GaN MOSHFETs with 20nm ALD HfO_2 and Lgd = 10µm

	Specific R_{on} (mΩ-cm^2)	Threshold Voltage (V)	Peak Transconductance (mS/mm)	Drain Leakage (A/mm)	Gate Leakage (A/cm^2)	Hysteresis (V)
Single Pulse H_2O	1.579	-13.75	110.41	1E-08	1E-04	0.4
Single Pulse H_2O with No PDA	1.418	-14.25	62.60	1E-04	1.8	0.7
Double Pulse H_2O-H_2O	1.756	-14.50	70.39	1E-07	5E-02	0.3
Double Pulse H_2O-Ozone	1.381	-4.90	97.64	8E-10	2E-06	0.4

In order to further understand the role of ozone, we investigated physical characterization by doing grazing incident angle x-ray diffraction on GaN MOSHFETs with identical conditions above (20nm ALD HfO_2 & 600°C PDA). A Grazing angle XRD scan helped determine crystallinity of the splits whereby devices with double pulse oxidants showed less crystallinity compared to a device with single pulse H_2O oxidant.

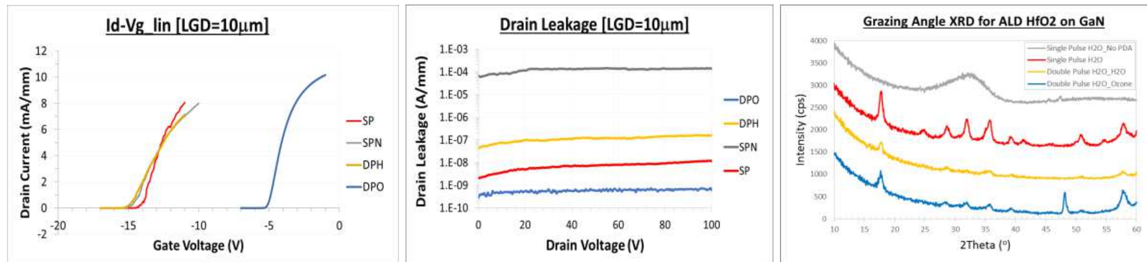

Figure 2. (a) DC Ids-Vgs and (b) drain leakage current extracted from GaN MOSHFETs with 20nm ALD HfO_2 and Lgd = 10μm; SP = Single Pulse H_2O, SPN = Single Pulse H_2O with No PDA, DPH = Double Pulse H_2O-H_2O, DPO = Double Pulse H_2O-Ozone, (c) Grazing angle XRD results for HfO_2 dielectrics

5. Other Relevant Work Being Conducted Within and Outside of the ERC

Our group is the only group doing gate dielectric reliability work in the FREEDM center. Outside of the ERC, many universities and companies from U.S.A, Europe, and Asia are studying the effect of device stability and reliability for 650V GaN MOSHEMT.

6. Milestones and Deliverables

Report high temperature GaN MOSHFET Reliability and stability evaluation at high temperature (> 150 ^{o}C)

7. Plans for Next Five Years

Gate dielectric is an essential part for reliable and stable operation of power device especially on GaN substrate. Many other research groups are studying high temperature reliability and we will continue to evaluate high temperature reliability and stability. Our dielectrics can be implemented into the vertical GaN or other wide bandgap semiconductors like Ga_2O_3.

8. Member Company Benefits

No member companies are involved in this project.

9. References (Published after last report)