Flexible Epoxy-Resin Substrate Based 1.2 kV SiC Half Bridge Module with Ultra-low Parasitics and High Functionality

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***Abstract*—To take full advantages of Wide Bandgap power semiconductor devices, breakthroughs on power module development are heavily explored nowadays. This paper introduces a 1.2kV SiC half bridge intelligent power module utilizing 80μm flexible epoxy-resin as substrates instead of traditional Direct-bonded Copper, for better thermal-stress management and lower cost. The investigation on the flexible epoxy-resin material indicates that it has low leakage current even at 250 °C, and high thermal conductivity up to 8 W/mK. No bonding wires are applied in the half bridge power module, instead, double-side solderable SiC MOSFET and diodes are fabricated and utilized for low parasitics and double-side cooling function. To further decrease the entire parasitic inductance on the power loop, a "Stack Structure" is proposed in this work to vertically connect highside and lowside switches with lower interconnection path than traditional power module technology. Simulation indicates that the parasitic inductance on the power loop is less than 1.5 nH. More functionality is achieved by integrating the main power stage with gate driver circuits. Digital isolations are also included in the half bridge module, together with a Low Dropout regulator to eliminate the numbers of auxiliary power supply required by the power module. The size of the entire module is about 35mm × 15mm ×7mm. Electrical simulations and measurements, including leakage current, parasitic extractions, device characteristics, verified that the designed module can work properly with no degradation on the SiC devices, with 12ns turn-off and 48ns turn-on at 800V bus voltage, and 0.63 mJ, 0.23 mJ as turn-on and turn-off loss, respectively.**

Keywords—Epoxy-resin substrate, Intelligent Power Module, Wide Bandgap Power Device, Low Parasitics, Double-side Cooling, High Functionality

I. INTRODUCTION

Due to the superior material properties of Wide bandgap (WBG) semiconductors, WBG power devices has been developed for converter applications in which tranditional Si power devices show limitations [1, 2, 3, 4]. To take full advantage of WBG power devices, the development of power modules technology is being extensively explored for applications including high frequency, high voltage and high temperature [5, 6]. To fulfill in situ characterization and tests of SiC devices with high voltage ratings at higher ambient temperature, a packaging solution for high voltage (> 12kV) and high temperature (225°C) applications has been developed by the PREES Lab from NCSU [7]. In terms of high frequency, efforts are focused to reduce parasitic inductance, e.g. SKiN and Direct Pressed Die technologies developed by Semikron [8], Planar packaging developed by ORNL [9, 10], PowerStack technology by Texas Instruments [11], etc. Companies are also seeking for different interconnection materials and technologies to further improve the performance of power modules, in terms of thermal issue and reliability, e. g. Insulated Metal Baseplate (IMB) based power module by Mitsubishi [12, 13, 14], Power Overlap technology by GE [15], etc.

Additionally, substrate technologies for power module has been discussed and developed for a while. The copper-clad ceramic substrate, such as Direct-Bonded-Copper (DBC) with Al2O3, AlN or Si3N4, is widely applied in power modules. The clad substrates are a benchmark with relatively high thermal conductivity, low coefficient of thermal expansion (CTE), and excellent heat-resistance [16, 17]. However, The cost of DBC substrates is another concern, pushing industries seeking for more cost-effective power module substrate solutions.

In this paper, a high density intelligent half bridge power module utilizing flexible 80μm-thick epoxy-resin based material as substrate is introduced. Within the size 35mm × 15mm × 7mm, SiC MOSFETs and Schottky diodes are integrated together with gate driver circuits, digital isolators, Low Dropout regulators (LDO) for more functionality. Double side solderable SiC devices are applied in the module to enable double-side cooling and replace traditional wire-bonding technology for ultra-low parasitics. A stacked structure is designed and implemented in the half bridge power module to further lower the inductance on the power loop by limiting the interconnection path between high-side and low-side switches. The preliminary investigation on the thin epoxy-resin material for substrate applications are firstly introduced. Then the design and fabrication processes for the

high density Intelligent Power Module (IPM) are discussed in details. The most recent test results, including the static and dynamic characteristics of the power module, are analyzed as the verification of the high density IPM design concept and capability and performance.

II. Properties of Epoxy-Resin Based Dielectric

This work initiates to propose flexible substrate for power module applications [19]. The primary properties of the epoxy-resin based dielectric material is as shown in Table. I. The thermal conductivity is up to 8 W/mK, which is among the similar materials with high thermal conductivity. It can operate at more than 250 ºC, able to handle power module with junction temperature even higher or operation condition at high ambient temperature, taking full advantages of high operation temperature capability of SiC power devices. The CTE is also close to copper (16.7 ppm / ºC), compared with ceramic in traditional DBC substrate (4.5-7 ppm/ºC), this is good for better thermal-mechanical stress management on power module during fabrication and services.

Table I. Properties of proposed Resin-epoxy Based Dielectric

Parameter	Value	Unite
Thermal Conductivity	8	W/mK
Tg	270	ºC
Modulus	30	GPa
CTE	9/22	ppm/ºC
Dk	6.3	/
Df	0.009	/
Dielectric Strength	5.6 @ 120 µm	kV

According to Table. I, it indiates that the dielectric strength is 5.6 kV with 120 µm thickness, enabling its applications in the high voltage area, such as 1200V SiC MOSFET based motor drive [18].

The Epoxy-resin Dielectric can be manufactured with minimum thickness as 80µm, and it can be bonded with copper and aluminum plate directly through a temperature profile. As shown in Fig. 1, the dielectric can be bonded with 70µm on one side, with 210µm copper on the other side. The surface roughness is essential to ensure a good bonding quality. In this work, the 80µm dielectric with 70µm/210µm on different sides are applied in the power module as substrates.

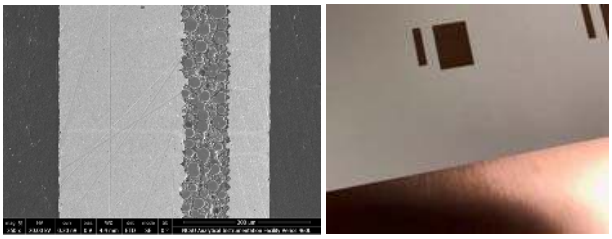


Fig. 1 Cross-section SEM image for bonding interface between Epoxy-Resin Dielectric and Copper plate (left), dielectric with coppe bonded on the top surface (right)

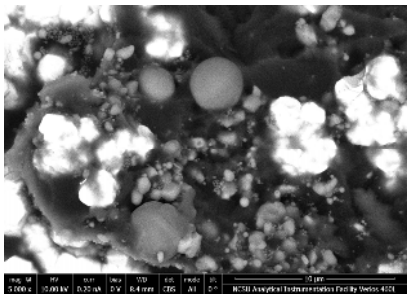


Fig. 2 SEM Image for Internal Microstructure of the Epoxy-resin Dielectric Material

The detailed composition of the epoxy-resin dielectric is also investigated as shown in Fig.2, at 5000X magnification. There are large amount of round shaped particles distributed in the epoxy-resin, the particle size ranges from 5 µm to 40 µm. An more detailed EDS and XRD analysis indicates that the large particles are aluminum oxide, and there are also a few amount of aluminum nitride particles distributed inside the materials. Those two types of particles make significant contribution to the high thermal conductivity of this material.

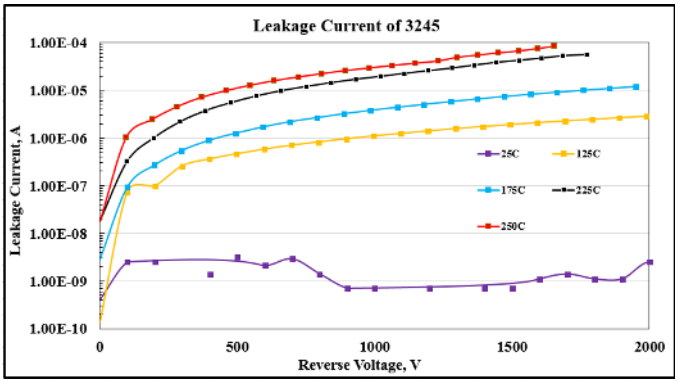


Fig.3 Leakage Current of Epoxy-resin Dielectric at different Temperature

The dielectric properties of the epoxy-resin dielectric is investigated by measuring it leakage current at different voltage and temperature, as shown in Fig. 3. The leakage current at DC condition is around 1nA, indicating good dielectric capability. At high temperature up to 250ºC, the leakage current at 1200V is still limited to 20 µm, which is comparable with SiC devices leakage at similar conditions. The results indicate that the dielectric is good for substrate of 1200V power module applications.

Reliability tests including thermal aging and thermal cycling is also performed to evaluate the performance of the material. And more data will be released in the near future.

III. Design of Electrical Circuit and Power Module

In the circuit design, the main power loop is the half bridge topology, with a high side SiC MOSFET and its corresponding SiC schottky diode, and a lowside pair. Its corresponding gate driver circuits are all integrated to lower the interconnection path and improve the power density.

A. Circuit Schematic Design

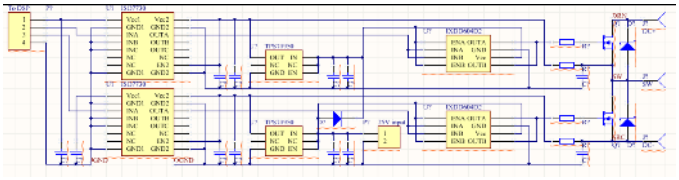


Fig. 4 Circuit Schematic for the Half bridge IPM

The circuit schematic is as shown in Fig. 4. Gate driver circuits are designed for each individual device pair, including high-side devices and low-side devices. Bootstrap diode and capacitor are applied to provide power supply for both gate drivers. Digital isolators are also integrated for protection between main power loop and the signal from microcontroller during applications.

To further illuminate the amount of auxiliary power supplies required for this IPM, LDOs are included to convert the 20V power supply for gate driver circuits to the 5V for the digital isolation secondary side. The primary side of the digital isolator is connected to some terminals in the module for interconnection with external circuits, such as microcontrollers, etc.

B. Physical Structure of the SiC Half Bridge IPM

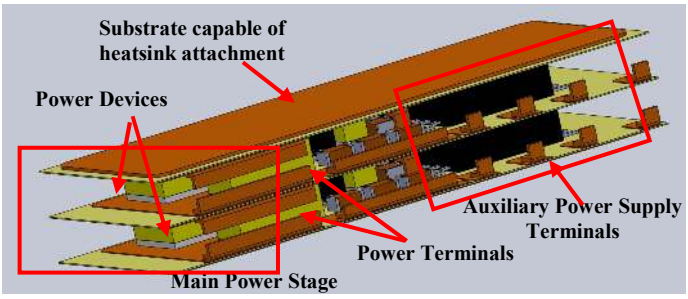


Fig. 5 Physical Structure Design of the Half Bridge IPM

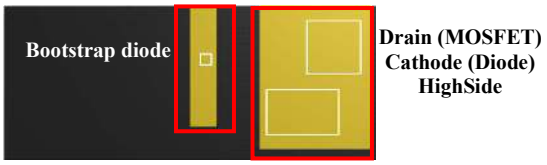
As shown in Fig. 5 is the physical structure design of the half bridge IPM. High-side switch and low-side switch are on two different substrates which are stacked together, and they are connected by the power terminal at the switch node at the middle layer. Yellow bulks inside the module are spacers to match the height difference between bare SiC devices and digital isolators on different levels. The corresponding gate driver circuits for each switch on the same level with it. And all the external connections to the circuits are going through the small terminals as shown in the figure.

The back side of top and bottom substrate are with 210 μm copper, which is able to directly attached by heat sinks on both sides of the module. All the terminals are on the same side of the module, to make the module able to be placed on the PCB board for system level integrations, and at the same time allowing for double-side cooling by heat sinks. In this design, the high density IPM can be applied in the system with lowest parasitics inductance and maximum cooling functions.

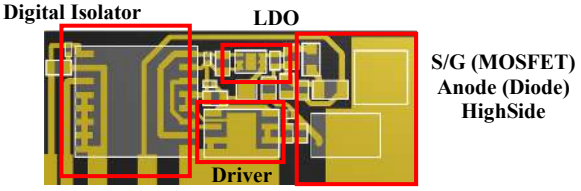
C. Circuits Layout Design for the Power Module

The layout design is as shown in the Fig. 6. Since double side solderable SiC power devices are applied for double side cooling, the entire layout design is divided into 4 parts.

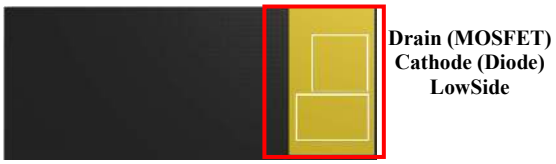
For the highside switch which is located at upper layer in the module, a bootstrap power supply is required, so a double-side solderable diode need a pad to make the topside connection, as shown in the Fig. 6(a), it is a narrow long strip. The pads for power devices are all the largest one on each layout, to maximize the heat dissipation capability during the operation. And all the power devices are flipped connected on the bottom substrate of each layer, to make sure the gate of SiC MOSFET directly connection with gate driver circuits with lowest loop parasitics.



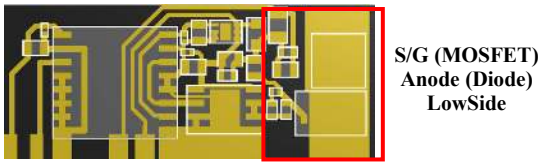
(a) Top side interconnection for highside switch



(b) Bottom side interconnection for highside switch



(c) Top side interconnection for lowside switch



(d) Bottom side interconnection for lowside switch

Fig. 6 Layout design for electrical circuits in the module

All the interconnections between four different layouts is achieved by the terminals located on the single side of the designed power module. So the small terminals are carefully arranged to avoid unnecessary loop in the entire circuits design. The rectangle pads at the bottom edge as shown in Fig. 6(b) and Fig. 6(d) are the location for different terminals attachment.

IV. Simulation Results

The designed power module is targeted for high power density and low parasitics applications, so the parasitics are extracted according to the Q3D simulation results to verify the

design. Then the switching performance of the module is simulated using inductive load switching circuits.

A. *Parasitics Analysis*

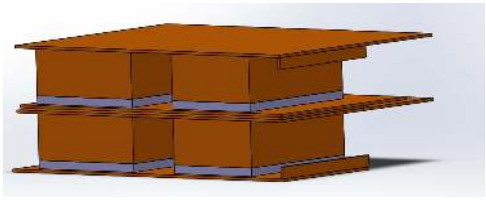


Fig.7 3D Modeling of the main power loop of the half bridge power module

The parasitics will have direct impact on the main power loop in the power module, lower parasitics will reduce the loss during operation of the system, and eliminate the EMI issue. To extract the parasitic inductance and resistance on the power loop, the entire two-layered IPM module is simplified and the main power loop model is as shown in Fig. 7. Only three terminals, including bus terminals and a switching node terminals are included, together with power devices with exact same size of the real die on two layers.

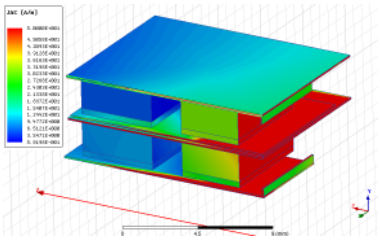


Fig. 8 Current distribution across the main power loop

From the Q3D simulation results, a current distribution is obtained as shown in Fig. 8. As shown in the figure, the current density is concentrated around the three terminals. This is due to the current is mainly flow from the DC+ terminal to the DC- terminal and it is not evenly distributed in the loop.

Table II. Parasitics Extraction along the Power Loop at 1MHz

Location	Inductance / nH	Resistance / mΩ
DC+ → DC-	1.3034	0.443
High-side MOSFET Drain	0.4390	0.188
High Side MOSFET Source	0.1994	0.102
High-side Diode Anode	1.8660	0.380
High-side Diode Cathode	2.2345	0.462
Low-side MOSFET Drain	0.4932	0.157
Low-side MOSFET Source	0.2327	0.149
Low-side Diode Anode	1.9968	0.436
Low-side Diode Cathode	2.0781	0.547

The parasitic inductance and resistance are extracted, and the number is as listed in the Table II. From the table, it can be found that the parasitic inductance in the entire power loop is only 1.30 nH, which is among the lowest parasitic inductance value in currently available developed half bridge module.

B. *Switching Transients in Double Pulse Circuits*

The extracted parasitics is then imported into the circuit model, and the spice simulations are applied to compare the impact from the low parastics on the switching behavior with that of the ideal circuit with no parasitics. The inductive-load switching circuit is applied to do the evaluation, and the turn-off waveform of the device in the circuits without and with parasitics are as shown in Fig. 9 and Fig. 10

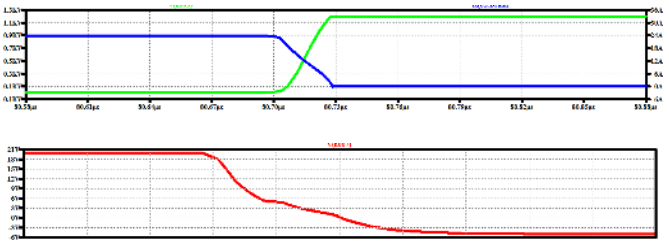


Fig. 9 Switching waveform of low-side switch in the circuit with no parasitics

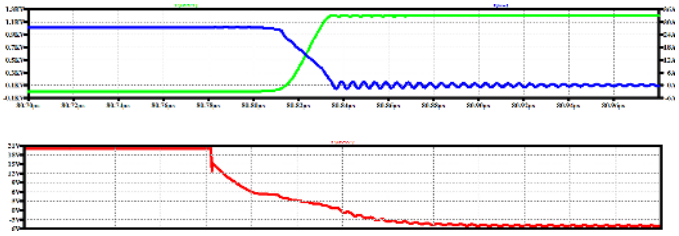
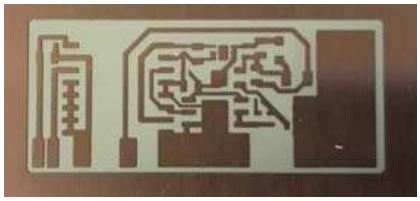


Fig. 10 Switching waveform of low-side switch in the circuit with extracted parasitics

In the simulation, the bus voltage is set as 1000V, and targeted current rating is set as 32A. According to the waveform, only limited ringings appear in the current and voltage waveforms, which is less than 2A for drain current and less than 50V for Vds.

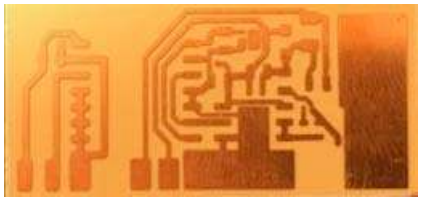
V. FABRICATION OF THE DESIGNED POWER MODULE

A. *Layout on Epoxy-resin Based Dielectric*

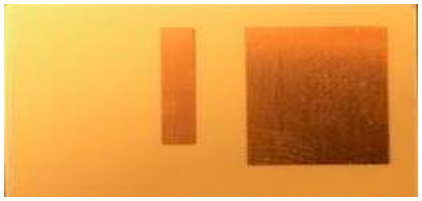


(a) layout at the bottom of highside switch layer

(b) layout at the top of Low side switch layer



(c) layout at the bottom of the low side switch layer



(d) layout at the top of the highside switch layer

Fig. 11 Fabricated layout on the four layers for circuits interconnection in the power module

Similar as the etching process for layout fabrication on the DBC substrate, the designed layout of the power module is fabricated with industry standard copper etching process. The minimum line width and clearance in the current layout design is 0.2mm, and the etching is done on the copper with 70µm thickness.

B. *Double-side solderable SiC devices*

Double-side solderable SiC devices have been proposed and investigated by the industry for years, due to its capability to enable wirebond-less interconnection and double side cooling functions in the power module. In this work, the double-side solderable SiC devices are fabricated based on the current commercially available devices with aluminum as top side metallization.

As shown in Fig. 12, the SiC Schottky diode is metallized with copper on the topside. The Electron-beam process is applied for the copper deposition. Mask is applied to protect the passivation portion on the die surface during the metallization process. The thickness of the copper is calibrated as around 2.0 µm.

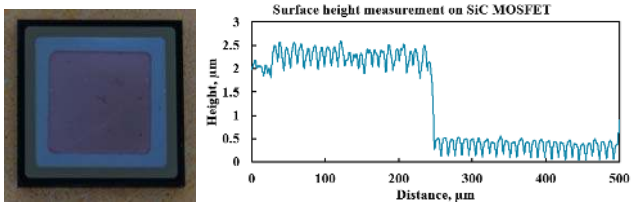


Fig. 12 SiC diode with Copper as topside metallization and its thickness profile

Fig. 13 SiC MOSFET with Gold Bumps on the topside for Interconnection

The SiC MOSFET is also fabricated with the same process as that applied on the SiC diode. Since the gate pad is very small, the deposited metal layer is different to be with good quality. In this work, the new approach is proposed. By directly plating gold bumps through wire bonding technology on the top surface of the die, the topside capability for soldering process will be modified. At the same time, since the bump height can be easily larger than deposited metal layer, the electrical isolation between die surface to the substrate interconnection layer will also be improved.

C. *Circuits Assembly on Flexible Dielectric*

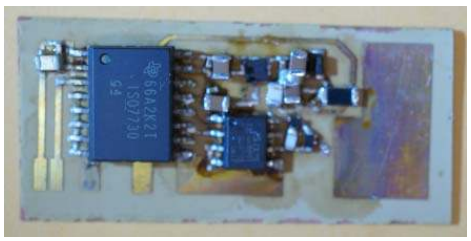


Fig. 14 Assembly of the gate driver circuits together with isolator and LDO on flexible dielectric substrate

The circuit on one single layer of the power module without main power devices is assembled as shown in the Fig. 14. The entire dimension of the space for components placement is around 15mm × 25mm.

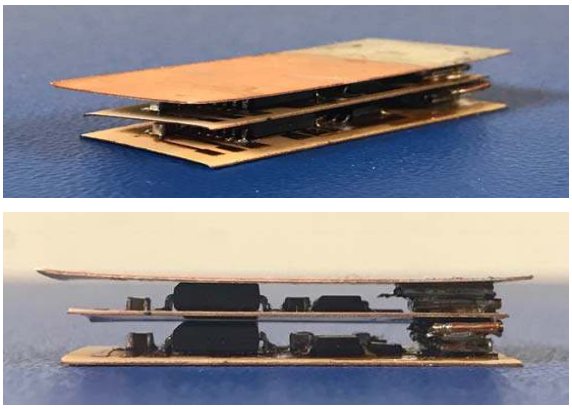


Fig. 15 Entire assembly of the whole power module with stacked structure before encapsulation

As shown in Fig. 15 is the assembled power module with stacked structure with different views. Moly spacers are applied to match the height difference between SiC devices with digital isolator, which is the largest components in the

power module. Encapsulation is injected then for protection and electrical isolation purpose. During the assembly process, 4 types of solder pastes are applied for attachment in different parts, to make sure each of the profiles does not bring in problems in the former ones.

VI. Measurement and Test Resutls

A. Static Chracterization of the Module

The static characteristics of the SiC MOSFET and diode in the module is reported in [20]. The forward and reverse characteristics of SiC diode, the blocking and output characteristics of SiC MOSFET in the designed flexible substrate based power module is verified, and proved to be close to the device behavior as shown in the datasheet of the product. Also described in [20] is the measurement result of the designed gate driver circuits together with LDO and digital isolators.

After the assembly process, the forward voltage drop of the schottky diode in the power module and body diode of SiC MOSFET is measured, and they are 0.69V and 1.29V respectively, as shown in Fig. 16.

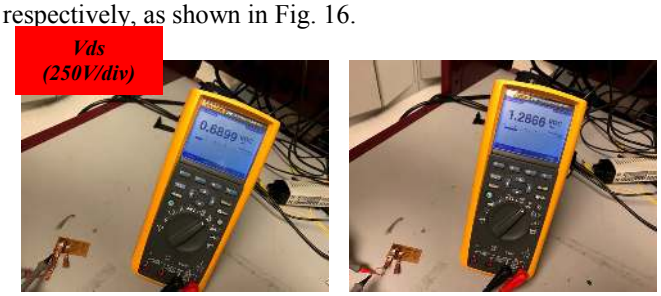


Fig. 16 Measurement of the forward characteristics of the SiC Schottky dioe and SiC MOSFET body diode

B. Dynamic Chracterization of the Module

The proposed power module is featured with ultra-low parasitic inductance on the power loop by the stacked structure for interconnection, after the assembly process the double pulse tests are applied to further evaluate the performance of the power module during switching transient.

The test set up is as shown in Fig. 17. Only the power stage is evaluated at this point, so external gate driver board is applied to turn on and turn off the SiC MOSFET. During the test, the stacked power stage is encapsulated in the silicone gel for electrical isolation.

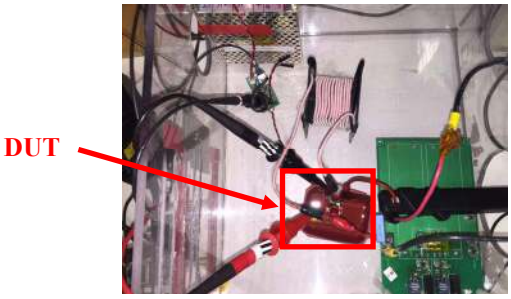


Fig. 17 Double Pulse test set up for the stacked power stage

During the test, the Vds is up to 800V, and Id is up to 30A. The turn-on and turn-off transient waveforms are as shown in Fig. 18 and Fig. 19.

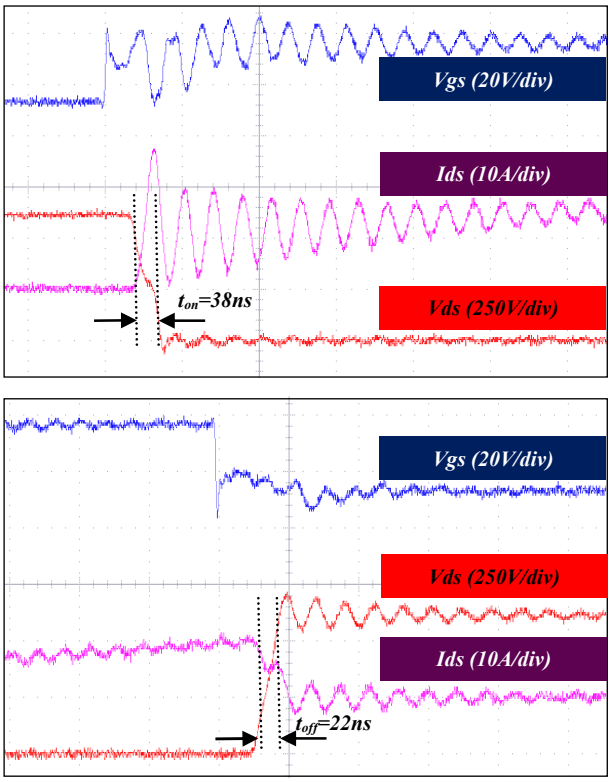


Fig. 18 Turn-on (upper) and Turn-off (lower) Transient at Vds = 600V

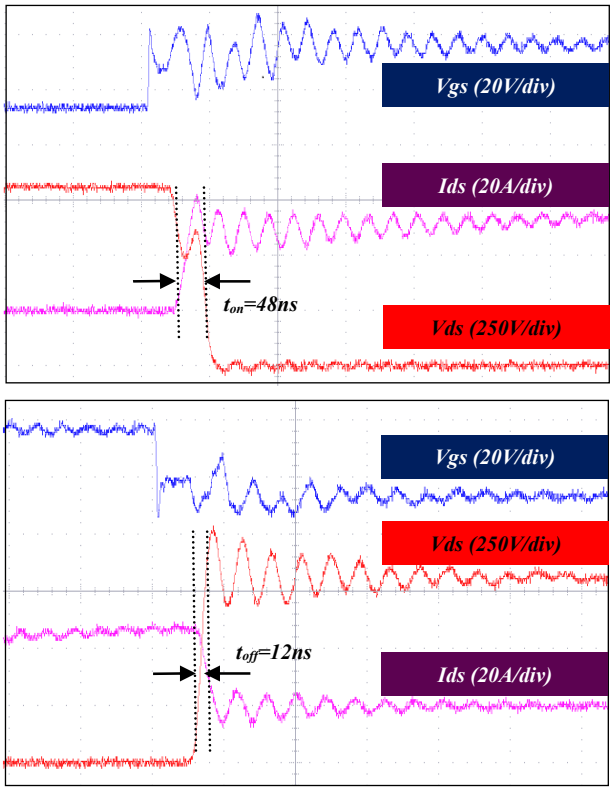


Fig. 19 Turn-on (upper) and Turn-off (lower) Transient at Vds = 800V

During the test, the gate resistor is set as 5 ohm for turn on and 2.5 ohm for the turn off. According to the transient waveform, it can be found that the turn on transient is around 38 ns for 600V bus voltage and 48 ns for 800V bus voltage, and the turn off transient are 22ns and 12ns respectively. For the Vds=800V, a noise came in to lower the gate voltage and delayed the turn-on transient.

Ringing on both sets of waveforms is significant, especially for the 600V bus voltage, this is due to the position of the decoupling capacitor is not close enough to the bus terminals on the power stage in the current test setup. Also, the external gate driver board poses more delay and gate loop inductance during the switching transient, due to the long interconnection path between the driver and gate of the SiC MOSFET.

The switching loss for power module operating at 800V is also evaluated by the measured current and voltage data, as shown in Fig. 20.

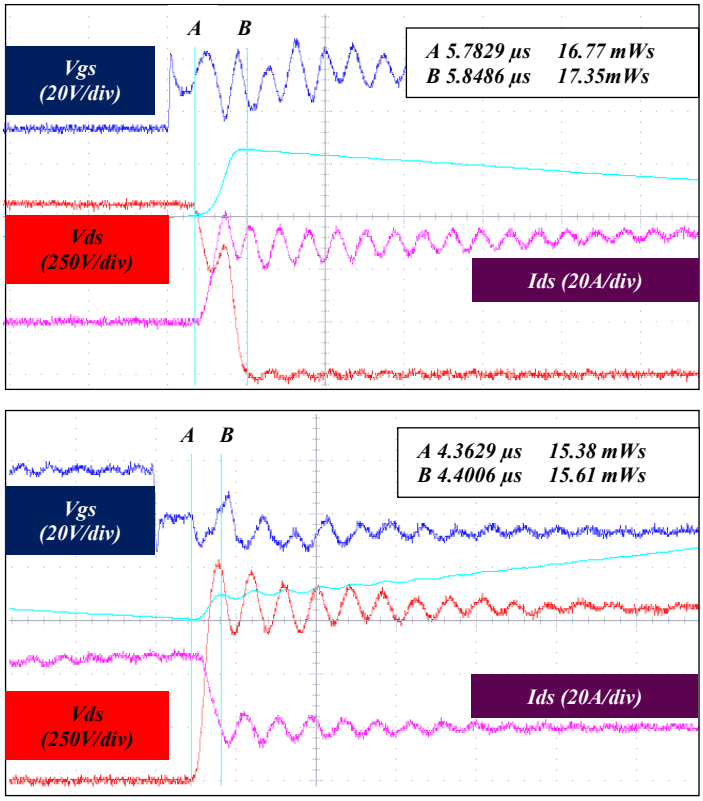


Fig. 19 Turn-on (upper) and Turn-off (lower) Transient at Vds = 800V

The loss curves during turn-on and turn-off are as shown in the blue line in Fig. 19. The turn on loss during the entire turn-on transient is 0.63 mJ, and the turn off loss during the entire turn-off transient is as shown 0.23 mJ.

The dynamic performance evaluation of the entire power module with integrated gate driver circuits, together with ioslators, is currently undergoing and more detailed data will be discussed in the near future.

VII. Conclusion

In this work, a flexible thin dielectric substrate material with high thermal conductivity is proposed to be the power module substrate for better mechanical stress management and cost-effective approaches for power module development. The properties of the dielectric material is discussed, with its capability to bond with copper and aluminum for metal clad laminates. The investigation on this material proves that it can be a good candidate for power module substrate.

A half bridge power module with vertically interconnected high-side and low-side switches is designed, based on the flexible thin dielectric substrate material. Q3D and spice simulations indicates that only less than 1.5 nH parasitic inductance is in the designed power module. The module also features double-sided cooling capability, by employing double-side solderable SiC MOSFETs and diodes. An innovative top-side solderable SiC device fabrication process is introduced, with gold bumps though regular wirebonding process.

Static measurements on the half bridge power module indicates that no degradation on the performance of the SiC devices appears in the power module. Double pulse tests indicates that the design of the power stage can go at least up to 800V bus voltage and 30A capability, with turn off transient around 12ns.

This work initiated the development of WBG power module by utilizing epoxy-resin based ultra-thin substrate. A systematic description about the design, fabrication and characterizations of the power module is provided, together with some works that will be delivered in the near furture.

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