Flash MOS-HFET Circuit Operation

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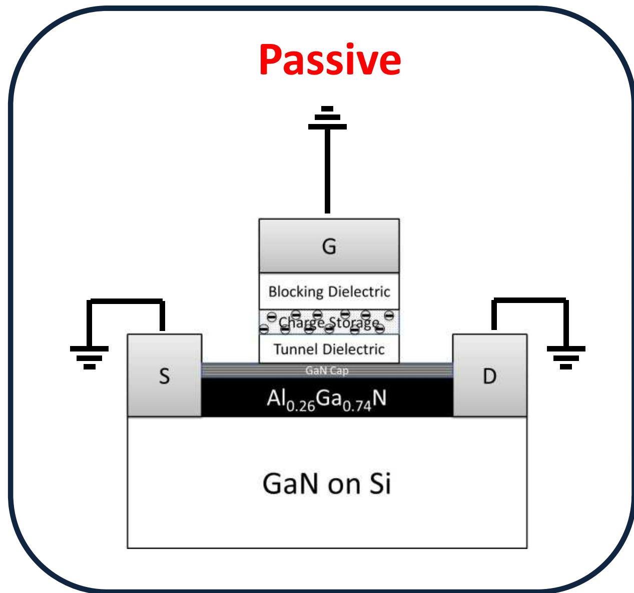
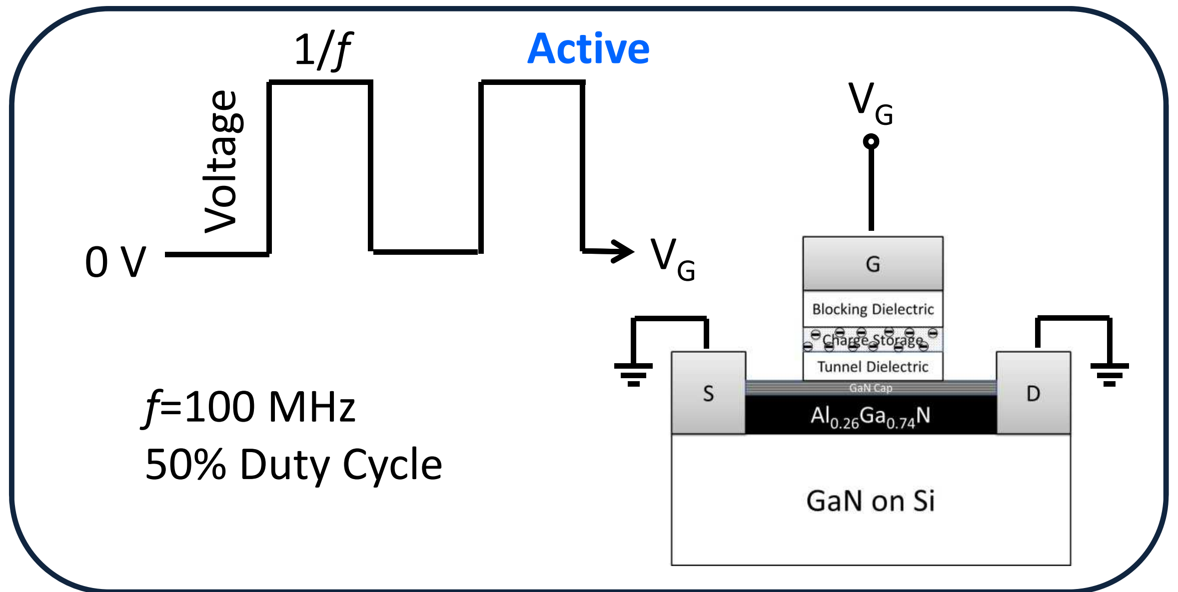
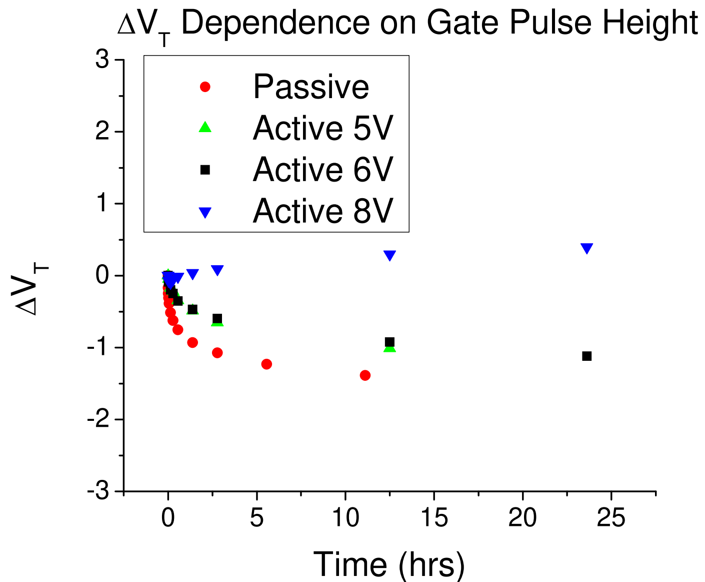
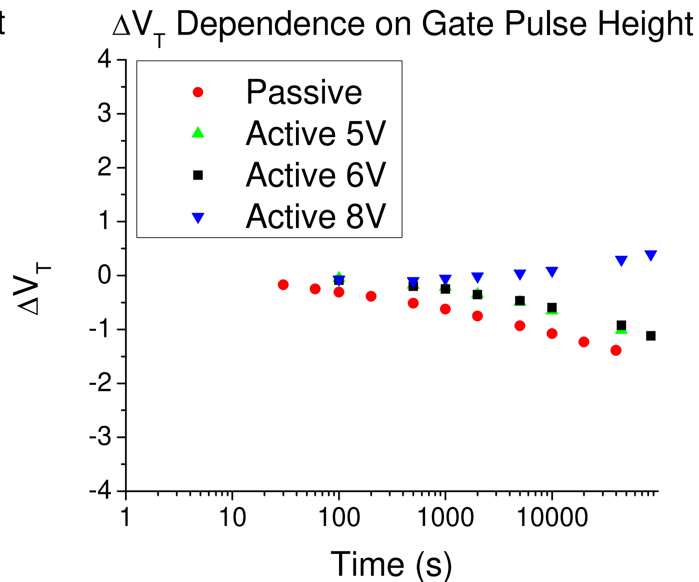
Dynamic Recharging Retention





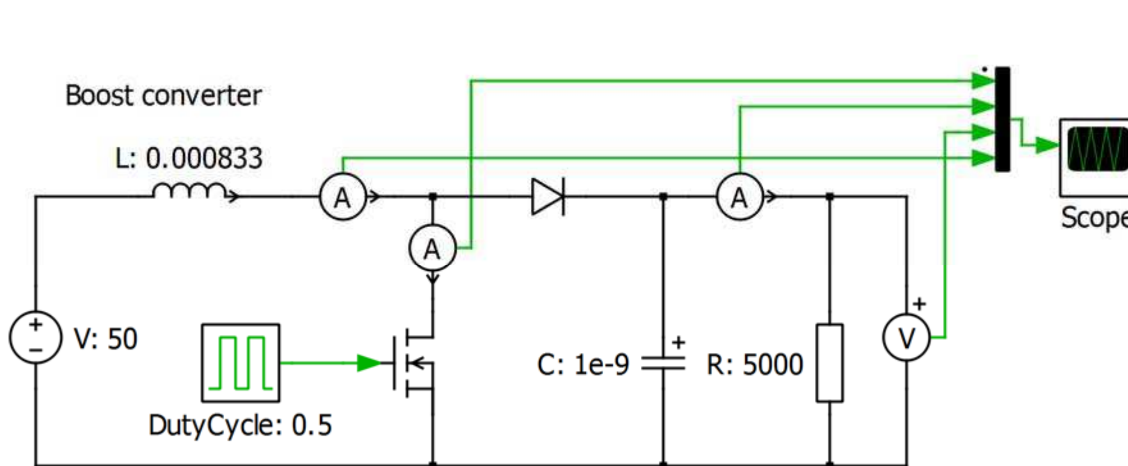


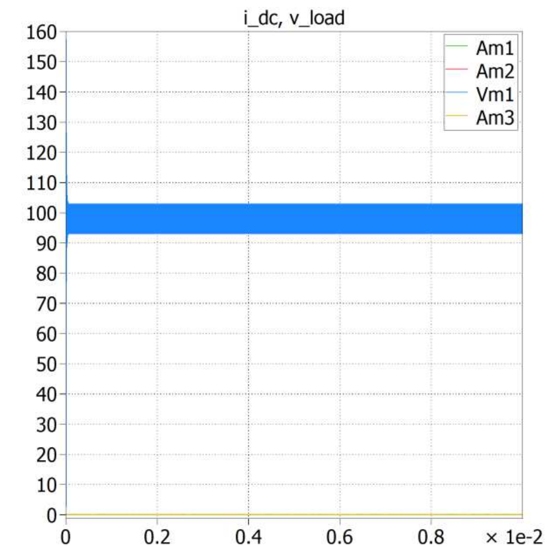


- Active retention with a gate pulse of 8 V prohibits decrease in threshold voltage
- Small increase in threshold voltage observed which is expected to saturate on a longer time scale

Power Converter Test Circuit

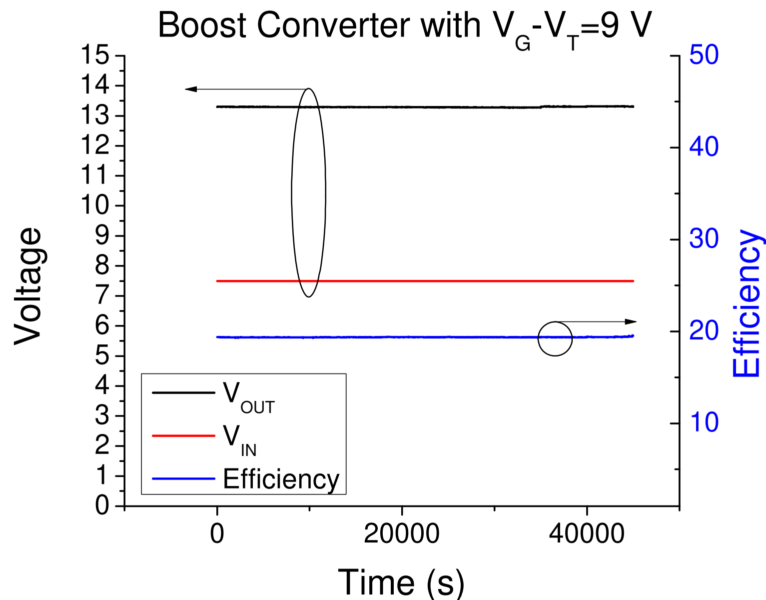
- Circuit below constructed to test retention during actual operation
- Boost converter designed for 50V to 100 V
  - Parasitic effects and equipment limitations have limited operation to low voltage
- Designed for 1 MHz, 50% Duty, 0 to 16 V V_G gate pulse
- Low current (50 mA) design
- Circuit and equipment configured for on-chip probe based testing

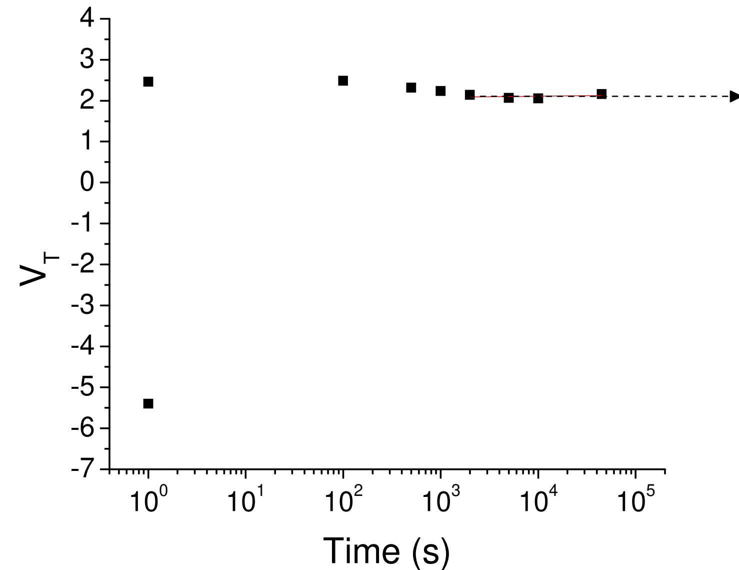




Flash MOS-HFET Circuit Operation

- Test device is a charge trap storage type Flash MOS-HFET
- Charging pulse 17 V above V_T
- Room Temperature
- V_{IN}=7.5 V, V_{OUT}=13.5 V
- f=1MHz
- 50 % Duty Cycle
- 11.5 V Gate Pulse





- Threshold voltage stable for duration of measurement
- Output voltage and efficiency remain nearly constant for duration of measurement
- Linear extrapolation of last four data points for V_T predicts stable, constant V_T of 2.1 V during circuit operation
- Efficiency and device output remain stable for duration of the measurement as well
- Slight increase in V_T for last data point