Predictive Control of a Series-Interleaved Multi-Cell Three-Level Boost Power Factor Correction Converter

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***Abstract*—This paper presents a new predictive power-factor-correction (PFC) controller for series-interleaved three-level boost (TLB) converters. Compared to the state-of-the-art TLB PFC controllers, where a two-cycle prediction and a detection of an operating region are necessary, the proposed controller achieves a low total harmonic distortion of the input current by using a single equation to predict the input current in all operating regions of the converter, in just one operating cycle. The average current control is achieved by sampling at the peak of the triangular carrier. The proposed PFC controller significantly reduces the distortion of the input ac current near the zero-crossing points, resulting in low total harmonic distortion of the input current. The operation of the proposed controller was evaluated and its stability and robustness to parameter changes was confirmed analytically. The controller operating principles were verified in simulations and validated by experiments on a medium-voltage 50-kW converter prototype.**

***Index Terms*—Multi-cell topology, PFC, predictive control, solid-state transformer, three-level boost.**

I. Introduction

THE solid state transformers (SST)-based power electronics systems have been extensively investigated in recent years due to high efficiency, high power density and controllability they offer when connected to medium voltage (MV) power grids. Researchers are considering using SSTs in wide range of applications, such as smart distribution grids and microgrids [1]–[6], power distribution systems for data centers [7]–[9], and electric vehicle fast charging systems [10]–[12]. Recent developments in wide band-gap (WBG) semiconductor power devices, especially silicon carbide (SiC) devices, have enabled SSTs to operate at higher switching frequencies, with substantial reduction in losses and significant improvement in converter power density. Due to the limited voltage blocking capability of the state-of-the-art SiC power devices, the input-series-output-parallel (ISOP) modular topologies are commonly used in MV SST converters proposed in the literature [13]–[16]. By connecting multiple converter modules in series at the input, the converter is able to handle the high input voltage, while the parallel connection at the output enables a low-voltage and high-current output required in most SST applications. One such topology is a multi-cell Boost (MCB) topology, which offers numerous advantages in terms of cost, switch utilization and efficiency metrics, compared to the other unidirectional topology candidates [5]. Each module of the MCB topology consists of a three-level boost (TLB) power-factor-correction (PFC) stage, a split dc link, and an isolated dc/dc stage with three-level neutral-point clamped (NPC) inverter at the input and a diode bridge at the output. The controller proposed in this work is developed for series-connected TLB converters that can be used as a PFC stage in EV fast charging, data center power supply, or other dc power distribution applications.

The TLB topology (see Fig. 1) was first proposed in 1995 in [17] aiming to solve the inductor cost problem and device voltage limitations in high-voltage, high-power boost power-factor-correction (PFC) applications. The TLB topology has the following merits [18], [19]: (1) low electromagnetic interference (EMI) due to 3-level waveform; (2) the input inductor generates $\frac{1}{4}$ the current ripple compared to the boost converter (3) input current is continuous due to the location of the inductor; (4) relatively efficient silicon usage due to the large duty cycle in the entire operating range; and (5) low voltage stress on switches and diodes.

The TLB topology is typically used as a power-factor-correction circuit. Therefore, the controller needs to regulate the input current and the output voltages, while ensuring voltage balance between the two capacitors making up the output voltage. A number of approaches have been proposed to achieve these control targets. In [20] authors regulate the TLB dual output voltage and the input current using a Lyapunov function (i.e. sliding mode control). The controller is implemented using analog circuitry and the duty cycle is implemented using switching logic which requires region detection by comparing the input voltage and the bus voltage. The proposed approach shows good performance in both input current regulation and split bus voltage balancing. However, the resulting modulation scheme is not interleaved and the switching frequency varies, especially when the input voltage is close to the split dc-bus voltage. The frequency variation increases when there is an error in sensing, or if there is an imbalance in the split dc-bus voltages. Another common approach, presented in [21]–[26] uses look-up tables to generate gating signals, based on the output from the current controller,

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the voltage balancing controller, and the region detector. The region detector determines the feasible TLB switching patterns based on the instantaneous value of the input voltage (see Section II for details). The benefits of this approach include maximum gain for voltage balancing and high bandwidth due to the logic gate implementation. Proportional current control [21], [22] as well as hysteresis current control [23]–[26] were implemented to provide a high controller bandwidth. The main drawbacks of the approaches presented in [21]–[26] include: (1) interleaving of converters was not investigated (2) balancing control influences current regulation and (3) relatively high control complexity. Importantly, operating region detection is needed, which requires precise input voltage measurement and robustness to incorrect region detection.

In [27]–[30], researchers showed that the TLB average model transfer function of input current to bus capacitor voltage is unique in all operating regions. As a result, an interleaved multi-loop controller was designed that does not explicitly detect the converter operating region. Although significant improvements have been achieved in simplifying the control complexity, the proposed multi-loop controllers use proportional-integral (*PI*) control. Since TLB has a similar average model with the traditional boost, the zero-crossing distortion and trade-off between integral gain and stability problems for the *PI* control still exist [19]. Namely, since the integrator needs time to wind up at the zero-crossing point, the current waveform is affected and leans to the left [27]. Moreover, due to the effects of the intrinsic right-half-plane zero of the boost topology, which varies with respect to the load, the *PI* controlled PFC cannot maintain a well-regulated line current for a wide load range. A feedforward controller mitigates the zero current crossing distortion [31], [32]; however, as pointed out in [33], [34], this method is not able to solve the issue completely.

Recently, model predictive control (MPC) has garnered a lot of attention due to its superior performance compared to proportional-integral control. First presented in [35], MPC handles both linear and nonlinear models, and provides the maximum achievable bandwidth. Predictive control approaches have been studied thoroughly for boost converters. Reference [36] used the dynamic model of the inductor current and dc bus voltage to implement predictive control for the TLB. A regression method is used in [37] to predict the next cycle current for a digital controller delay compensation. However, with the switch function in the prediction equation, the control relies on region detection for correct operation. As shown in Section III.A, incorrectly determining the region boundary leads to current waveform distortion, and even instability in severe cases.

In this paper, a new predictive current control based on the interleaved leading-triangle modulation is proposed for the TLB topology, with stable performance and noticeable improvement in THD and reduced zero-crossing distortion. We show that for an interleaved switching pattern, the next state duty-cycle equations are unique. By applying the leading triangle modulation and suitable sampling strategy, we achieve average current control. Stability analysis shows that this new control method is intrinsically stable and that two-cycle prediction is not needed. We extend this theory to multi-level boost converter and demonstrate the proposed control on a multi-level boost topology used in a medium-voltage electric vehicle fast charger proposed in [38].

TABLE I: Operating Region and Mode Distribution of TLB

Region	**Operating Mode**	**Current Ripple Slope**
$\lvert v_{in}\rvert < \frac{v_{bus}}{2}$	1	$\frac{\lvert v_{in}\rvert}{L_{boost}}$
$\lvert v_{in}\rvert \leq \frac{v_{bus}}{2}$	2,3	$\frac{2\lvert v_{in}\rvert - v_{bus}}{2L_{boost}}$
$\lvert v_{in}\rvert \geq \frac{v_{bus}}{2}$	2,3	$\frac{2\lvert v_{in}\rvert - v_{bus}}{2L_{boost}}$
$\lvert v_{in}\rvert > \frac{v_{bus}}{2}$	4	$\frac{\lvert v_{in}\rvert - v_{bus}}{L_{boost}}$

The rest of the paper is organized as follows: Section II discusses the TLB, the building block of the multi-level boost converter. In Section III, we describe the operating principle, sampling, and modulation strategy for the proposed predictive control of the TLB, and we discuss the extension of the proposed control to the multi-level boost topology. In Section IV, we consider the stability and one-cycle delay effect to further justify the performance benefit of the proposed control. In Section V, the whole picture of the PFC control applied in a three-cell TLB topology is described in detail. In section VI, we present the simulation results considering various load conditions, parameter variations and calculation delay. In Section VII, we supply experimental results at 50 kW, 2.4 kVac input, 400 Vdc output. Finally, in Section VIII we draw the relevant conclusions.

II. Operating Principle of TLB

The TLB topology has four operating modes [17]–[30], [36], [37], [39] defined by four possible states of the two switching devices, namely $(1,1),(1,0),(0,1),(0,0)$ (see Fig. 1). In this work, we will assume that the TLB is operating in the interleaved mode, meaning that the carrier waveforms of the two boost switches are shifted by 180°. This approach leads to lower current ripple, where the current ripple magnitude is the same as that of the two interleaved parallel boost and is a quarter of the magnitude in conventional boost converter [17]. Further, the interleaved TLB operation is defined by two distinct operating regions, determined by comparing the input voltage v_{in} to the dc link capacitor voltage $v_{c1} = v_{c2} = \frac{v_{dc}}{2}$, assuming capacitor voltages are balanced. Since the voltage ratio of the TLB is the same as for the conventional boost converter, which is $\frac{v_{dc}}{v_{in}} = \frac{1}{1-d}$, comparing the input voltage v_{in} to half of the dc link voltage $\frac{v_{dc}}{2}$ will determine if the interleaved duty cycle is greater or less than 50%. With a 180°interleaving phase shift, a PWM duty greater than 50%, will eliminate the switching state $(0,0)$. Similarly, a PWM duty smaller than 50%, eliminates the switching state $(1,1)$. Based on Kirchhoff's Law, the operating modes and the resulting current ripple slope for each operating region are listed in Table I.

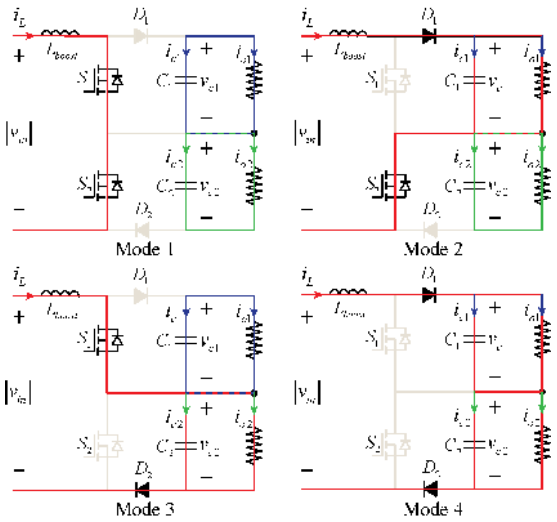

Fig. 1: Operating Modes of the TLB

Region One ($v_{in} < \frac{v_{bus}}{2}$), where the duty cycle for the interleaved TLB is larger than 50%. In this region, the sub-circuit is changing between *Mode 1* and either *Mode 2* or *Mode 3*, depending on which switch is active. In *Mode 1*, both switches are *ON*, the inductor sees a positive voltage v_{in}, resulting in increasing inductor current. In *Mode 2* or *Mode 3*, one of the switches turns *OFF*, and since $v_{in} < \frac{v_{bus}}{2}$, the voltage across the inductor $v_{in} - \frac{v_{bus}}{2}$ is negative, resulting in decreasing inductor current. The average inductor voltage and the current ripple is:

$$\langle v_L \rangle_{T_s} = |v_{in}| - (1-d)v_{bus} \tag{1}$$

$$\Delta i_{L\_up} = \frac{|v_{in}|}{Lf_s}(d-0.5) \tag{2}$$

$$\Delta i_{L\_down} = \frac{0.5v_{bus} - |v_{in}|}{Lf_s}(1-d) \tag{3}$$

Where d is the duty cycle and f_s is the switching frequency for each switch of the interleaved TLB. Here we assume that the TLB is working in an interleaved switching pattern. So the active up ripple time interval is $\frac{d-0.5}{f_s}$ and the down ripple time interval is $\frac{1-d}{f_s}$.

Region Two ($\frac{v_{bus}}{2} < v_{in} < v_{bus}$), where the duty cycle for the interleaved TLB is less than 50%. In this region, the sub-circuit is changing between *Mode 4* and either *Mode 2* or *Mode 3*. For *Mode 2* and *Mode 3*, only one dc-link capacitor is involved in the circuit. The inductor sees a positive voltage $v_{in} - \frac{v_{bus}}{2}$, resulting in increasing inductor current. In *Mode 4*, both switches are turned *OFF* with both the dc-link capacitors connected in the circuit. Since $\frac{v_{bus}}{2} < v_{in} < v_{bus}$, the $v_{in} - v_{bus}$ inductor voltage is negative causing a decreasing inductor current. The average inductor voltage and the current ripple is:

$$\langle v_L \rangle_{T_s} = |v_{in}| - (1-d)v_{bus} \tag{4}$$

$$\Delta i_{L\_up} = \frac{|v_{in}| - 0.5v_{bus}}{Lf_s}d \tag{5}$$

$$\Delta i_{L\_down} = \frac{v_{bus} - |v_{in}|}{Lf_s}(0.5-d) \tag{6}$$

Based on (1) and (4), the two working regions share the identical average model, which coincides with the single boost model presented in [27]. However, the current ripple equations are not the same, which means that the dynamic equations for the two working regions are different. This presents difficulties for implementing predictive control. Typically, the operating region needs to be detected correctly by comparing the input voltage to half of the DC bus voltage. The region detection is required in [36] where a predicitve controller is implemented. In [40], the authors point out that a *K* level boost should have 2^{K-1} operating modes and $K-1$ working regions, which makes the region detection very difficult when multiple cells are used. In our work, we reformulate the problem to obviate the need for region detection, as described in the following section.

III. Proposed Predictive Control for TLB

A. Control Principles

By transforming the dynamic circuit model into discrete time frame and applying the optimal duty cycle determined by estimating the current in the next-state, predictive current control provides faster dynamic response and better accuracy compared to *PI* current-control. Valley and peak current controls are widely applied to the conventional single switch boost PFC due to the simplicity and adequate calculation time [41]–[43]. The straightforward control principle is to predict the whole current path of one switching period and force the current at the end of the cycle to follow the reference. However, in PFC application with a varying current ripple, valley and peak current control may produce low order harmonics [44]. As a result, average-current predictive control is commonly used. In order to regulate the average value of the current over one switching cycle, low-pass filter [45], integrator [41] and artificial ramp comparator methods [46] were proposed. In existing approaches [40], [46]–[48], the prediction path ends at either the midpoint of the upward current ripple or the midpoint of the downward ripple, and the sampling point coincides with the peak or the valley of the current ripple (see Fig 2(a)). Since in [46] and [47] the control is implemented based on an analog comparison scheme, there is no specific sampling point shown in the figure.

The prediction methods, proposed in [40], [46]–[48] can be applied to the TLB, but require detection of the operating region. Taking the prediction path applied in [40] as an example, by sampling at the beginning of the duty cycle to predict the average downward ripple current value within the switching period, the predictive control can be summarized as below,

$$i_L[k] + i_{ripple\_up}(d) - \frac{1}{2}i_{ripple\_down}(d) = i_{avg\_ref}[k+1] \tag{7}$$

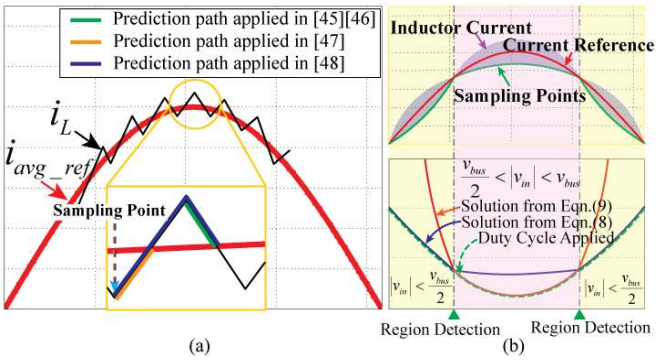

Fig. 2: Region detection required predictive control for TLB: (a) prediction path from reference [40], [46]–[48], (b) region detection mechanism for TLB

However, as demonstrated in [17], the relationship between the input/output voltage, duty cycle and the ripple current in TLB is different in the two working regions, resulting in a piecewise solution for the next state prediction. Considering operation in *Region 1*, and substituting (2) and (3) into (7), we obtain:

$$d[k+1] = \frac{i_{ref\_avg} - i_L[k]}{v_{bus} + 2|v_{in}|} \cdot \frac{4L}{T_s} + \frac{v_{bus}}{v_{bus} + 2|v_{in}|}, \; |v_{in}| < \frac{1}{2} v_{bus} \tag{8}$$

Similarly, considering operation in *Region 2*, and substituting (5) and (6) into (7), we obtain:

$$d[k+1] = \frac{i_{ref\_avg} - i_L[k]}{|v_{in}|} \cdot \frac{2L}{T_s} + \frac{v_{bus} - |v_{in}|}{|v_{in}|}, \; |v_{in}| > \frac{1}{2} v_{bus} \tag{9}$$

Referring to Fig 2(b), the two duty cycle solutions intersect at the point $|v_{in}| = \frac{v_{bus}}{2}$ where the region detection should happen. A region selector can be implemented to switch the calculating equations based either on the duty cycle in the previous cycle, or based on the comparison between the bus voltage and input voltage. Both methods will cause some oscillation around the transition point, which may cause the distortion in current and may even drive the system into instability.

To solve the issue of having to select the correct operating region, the proposed predictive control uses triangular modulation and samples the current at the peak of the triangle carrier, which is the mid-point of either the upward or downward current ripple. Given the sampling point, a prediction is made to force the next mid-point of the ripple current to follow the current reference. Figure 3 illustrates the approach in both operating modes.

For the working region $v_{in} < \frac{v_{bus}}{2}$, the sampling point is at the mid-point of the downward ripple. The controller predicts half of the downward ripple, the upward ripple and again half of the downward ripple based on the current sample. In order to force the next downward ripple to follow the reference current, the current waveform equation is as follows:

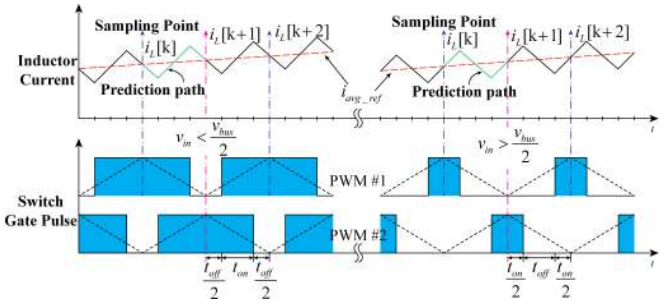

Fig. 3: Modulation, sampling and prediction principles for the proposed predictive control: (left) when the switch duty exceeds 50%, (right) when the switch duty is below 50%

$$i_L[k] + \frac{1}{2} i_{ripple\_down}(d) + i_{ripple\_up} + \frac{1}{2} i_{ripple\_down}(d) = i_{avg\_ref}[k+1] \tag{10}$$

Because TLBs switching frequency is much higher than the grid frequency, input voltage, current reference and bus capacitor voltages are assumed to be constant. Substituting (2) and (3) into (10) gives the solution for the duty cycle,

$$i_L[k] + \frac{|v_{in}|}{Lf_s}(d - 0.5) - \frac{0.5v_{bus} - |v_{in}|}{Lf_s}(1 - d) = i_{avg\_ref}[k+1] \tag{11}$$

$$d = 2Lf_s \frac{i_{avg\_ref}[k+1] - i_L[k]}{v_{bus}} + \frac{v_{bus} - |v_{in}|}{v_{bus}} \tag{12}$$

For the working region $v_{in} > \frac{v_{bus}}{2}$, the sampling point is at the mid-point of the upward ripple. Therefore, half of the upward ripple, the downward ripple and another half of the upward ripple are predicted. Similar to the above analysis, the current waveform can be expressed as:

$$i_L[k] + \frac{1}{2} i_{ripple\_up}(d) + i_{ripple\_down}(d) + \frac{1}{2} i_{ripple\_up}(d) = i_{avg\_ref}[k+1] \tag{13}$$

Substituting (5) and (6) into (13) gives:

$$i_L[k] + \frac{|v_{in}| - 0.5v_{bus}}{Lf_s} d - \frac{v_{bus} - |v_{in}|}{Lf_s}(0.5 - d) = i_{avg\_ref}[k+1] \tag{14}$$

$$d = 2Lf_s \frac{i_{avg\_ref}[k+1] - i_L[k]}{v_{bus}} + \frac{v_{bus} - |v_{in}|}{v_{bus}} \tag{15}$$

Since (12) and (15) are the same, we conclude that no working region detection is needed for this control method. Looking closely at (12) and (15), one can notice that the equations consist of a static component $\frac{v_{bus} - |v_{in}|}{v_{bus}}$ which reflects the operating point of the TLB converter where variables vary at line frequency, and a dynamic component $2Lf_s \frac{i_{avg\_ref}[k+1] - i_L[k]}{v_{bus}}$ which regulates the current at the switching frequency.

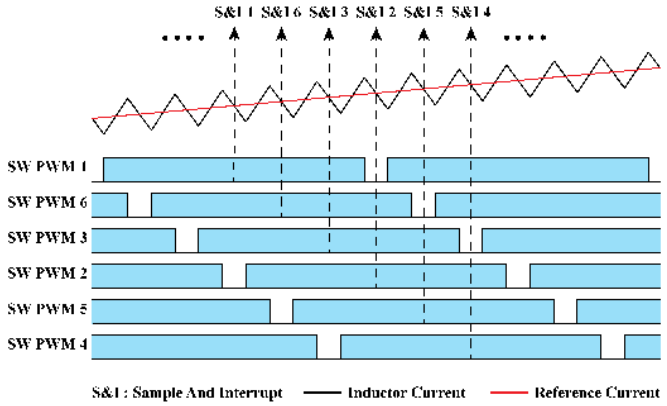

Fig. 4: Sampling and prediction scheme in a six-switch multi-level boost topology predictive control

B. Extension to N-Switch Multi-Level Boost

Cascading multiple TLB in series to form a multi-cell boost topology is necessary to handle higher input voltages in medium-voltage applications [5], [24]. As a result, an extension to *N-switch* boost predictive control is necessary. The sampling and prediction scheme for a six-switch multi-cell TLB topology is shown in Fig. 4. In the multi-cell TLB topology, *M* TLB converter modules are connected in series. Each of the TLB works in an interleaving pattern and all the TLB modules are interleaved with a phase shift $\frac{2\pi}{M}$. Prediction calculation occurs at every mid-point of the *ON* event for each PWM and the next cycle duty is applied to all 2M switches. For the N-switch ($N = 2M$) multi-level boost topology, N working regions will exist, each spanning $\frac{v_{bus}}{N}$ volts. The voltage across the inductor changes between the two values below in each region.

$$\begin{aligned} v_{L\_up} &= |v_{in}| - \frac{m v_{bus}}{N} \\ v_{L\_down} &= |v_{in}| - \frac{(m+1) v_{bus}}{N} \end{aligned}, \quad m \in [0, N-1] \tag{16}$$

According to Fig. 4, the predictive path is similar to what is described in III.A, which consists of half downward ripple, one upward ripple and half of the downward ripple again. Therefore, the control equation evaluates one upward current ripple plus one downward current ripple. Thus, the predicted inductor current equation in each region can be expressed as:

$$\begin{aligned} i_{avg\_ref}[k+1] = i_L[k] &+ \frac{v_{L\_up}}{L} t_{up} \\ &+ \frac{v_{L\_down}}{L} \left(\frac{T_s}{N} - t_{up} \right), \; m \in [0, N-1] \end{aligned} \tag{17}$$

Since the ripple is in the interleaving frequency ($N f_{sw}$) and all the PWMs are central aligned, the relationship between t_{up} and the duty cycle d can be derived. According to Fig. 4, the *ON* on time for each switch is:

$$\begin{aligned} t_{on} &= t_{up} + \frac{1}{2} t_{down} + \frac{N-1-m}{N} T_s \\ &\quad + \frac{1}{2} t_{down} + t_{up} \\ t_{down} &= \frac{T_s}{N} - t_{up} \\ d &= \frac{t_{on}}{T_s} \end{aligned} \quad , \quad m \in [0, N-1] \tag{18}$$

Simplifying (18), the expression for t_{up} becomes

$$t_{up} = (d - \frac{N-1-m}{N}) T_s, \quad m \in [0, N-1] \tag{19}$$

Combining (17) and (19), the region index m is eliminated, and the predicted duty cycle for *N-switch* multi-level boost is,

$$d = N L f_s \frac{i_{avg\_ref}[k+1] - i_L[k]}{v_{bus}} + \frac{v_{bus} - |v_{in}|}{v_{bus}} \tag{20}$$

IV. Performance Considerations

A. Sensitivity Analysis

Since the proposed predictive control is based on calculations involving the circuit parameters, an accurate estimation of these parameters is essential to avoid oscillations, and even instability [33]. Referring to (15), the duty cycle prediction is a function of i_L, L, v_{bus} and $|v_{in}|$. We assume that the low frequency values v_{bus} and $|v_{in}|$ are accurate, and note that the inductance L and the input current samples i_L are related linearly, but with opposite sign. Therefore, the current sampling error Δi_L can be treated as a negative inductance error ΔL. Thus, the controller sensitivity can be evaluated by looking at its sensitivity to the variation in input inductance. We will assume a general case where we have *M* TLBs with $N(= 2M)$ switches in the topology. Assuming accurate estimation of the inductance, the duty cycle for one switching period is,

$$d_{ideal} = N L_0 f_s \frac{i_{avg\_ref}[k+1] - i_L[k]}{v_{bus}} + \frac{v_{bus} - |v_{in}|}{v_{bus}} \tag{21}$$

However, in the real case, the estimation of the inductance is not perfect. The duty cycle is calculated based on the estimated inductance L:

$$d_{calculated} = N L f_s \frac{i_{avg\_ref}[k+1] - i_L[k]}{v_{bus}} + \frac{v_{bus} - |v_{in}|}{v_{bus}} \tag{22}$$

If a difference between L and L_0 exists at kth sampling instant, the calculated and ideal duty cycles will differ in the next switching instant. Subtracting (22) from (21), results in:

$$\Delta d[k] = \frac{\Delta i_L[k]}{v_{bus}} (Z_0 - Z) \tag{23}$$

where $\Delta i_L[k] = i_{avg\_ref}[k] - i_L[k]$, $Z_0 = N L_0 f_s$, and $Z = N L f_s$. The resulting current error at the sampling instant $k+1$ is:

$$\Delta i_L[k+1] = \Delta d[k] \cdot (m_1 - m_2) \cdot T_s \tag{24}$$

where m_1 and m_2 are upward and downward slope of the inductor current ripple. According to (16) and Table I, the slope difference $m_1 - m_2$ in any working region is $\frac{v_{bus}}{NL_0}$. Thus, the current perturbation in next 1 and m cycles are,

$$\begin{aligned}\Delta i_L[k+1] &= \frac{\Delta i_L[k]}{v_{bus}} \cdot (Z_0 - Z) \cdot \frac{v_{bus}}{NL_0} \cdot T_s \\ &= \Delta i_L[k] \frac{Z_0 - Z}{Z_0}\end{aligned} \tag{25}$$

$$\Delta i_L[k+m] = \Delta i_L[k] \cdot \left(\frac{Z_0 - Z}{Z_0}\right)^m \tag{26}$$

From (26), it can be concluded that for $Z > Z_0$, the stable criterion is $Z < 2Z_0$. However, since the $Z_0 - Z$ component is negative, the stabilizing process contains oscillations. And for $Z < Z_0$, system is always stable with no oscillations. However, the input inductance cannot be too small (Z cannot be too small compared to Z_0) for two reasons. First, since the inductance affects the dynamic part of the predictive equation, if the inductance is too small the dynamic performance of the predictive control will be affected. Second, since the inductance affects the gain of the control system, a small inductance will introduce steady state error into the control. Thus, the inductance value is adopted to be 10% lower than the minimum datasheet value (or the designed value if custom made) at the expected input current, which gives a good compromise between the stability and the steady-state response accuracy.

B. One-Cycle Delay Consideration

One-cycle delay is well-known phenomenon in the predictive control implementation. This delay happens because the optimal duty cycle determined at the instant k cannot be applied until after the instant $k+1$, since the calculations of the predictive algorithm are not finished before the switching event that corresponds to that optimal duty cycle. Therefore, the optimal duty cycle calculated using the measurement at instant k will be applied after instant $k+1$, resulting in an oscillation in the line current. Many techniques have been proposed to eliminate the one-cycle-delay including change in the modulation pattern [49], and change in the sampling point [50]. Reference [33], [51] use a two-cycle prediction where the prediction is aiming to regulate the inductor current value at instant $k+2$ based on the current sampling at instant k, $i_L[k]$ and the duty cycle in period k, $d[k]$ generated from the previous calculation. Assuming that the slow-changing variables are all constant within two consecutive cycles, the current at instant $k+2$ can be predicted as follows:

$$\begin{aligned}i_L^*[k+2] = i_L[k] &+ \frac{v_{L\_up}}{L} t_{up}[k] \\ &+ \frac{v_{L\_down}}{L}\left(\frac{T_s}{N} - t_{up}[k]\right) + \frac{v_{L\_up}}{L} t_{up}[k+1] \\ &+ \frac{v_{L\_down}}{L}\left(\frac{T_s}{N} - t_{up}[k+1]\right)\end{aligned} \tag{27}$$

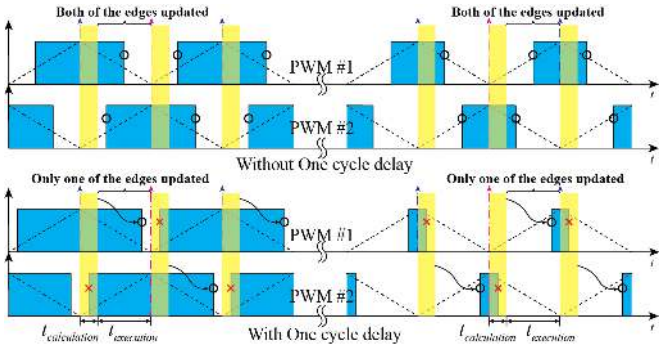

Fig. 5: One-cycle delay situations for the proposed interleaved predictive PFC control

$$d[k+2] = NLf_s \frac{i_{avg\_ref}[k+2] - i_L^*[k+1]}{v_{bus}} + \frac{v_{bus} - |v_{in}|}{v_{bus}} \tag{28}$$

where $i_L^*[k+1] = i_L[k] + \frac{v_{L\_up}}{L} t_{up}[k] + \frac{v_{L\_down}}{L}\left(\frac{T_s}{N} - t_{up}[k]\right)$. Since the predicted duty is calculated before instant $k+1$, the duty is implemented immediately at instant $k+1$. Although the two-cycle prediction can mitigate the overrun and delay problems [51], the prediction path is doubled compared to the one-cycle prediction, as pointed out in [49]. Also, the two-cycle prediction makes the control more sensitive to the inaccuracy in inductance estimation, voltage and current sampling and quantization, and variations of the v_{in}, v_{bus} [49]. This is especially the case in the ac/dc PFC applications where the input voltage changes. Furthermore, since the predicted duty cycle takes one more switching period to be implemented, the two-cycle prediction performs worse in terms of dynamic response and the current traction as pointed out in [52]. Thus the one-cycle prediction will have better response to a current reference change than a two-cycle prediction, as illustrated in Fig. 13 in Section VI.

However, in our approach, a one-cycle delay only happens when one of the switching events (either the rising or falling edge of the PWM pulse, as shown in Fig 5) is too close to the sampling point where the calculation starts.

At instant k, with the current perturbation $\Delta i_L[k]$, the calculated duty cycle is,

$$d[k] = \frac{\Delta i_L[k]}{v_{bus}} Z + \frac{v_{bus} - |v_{in}|}{v_{bus}} \tag{29}$$

Similarly, at instance $k+1$,

$$d[k+1] = \frac{\Delta i_L[k+1]}{v_{bus}} Z + \frac{v_{bus} - |v_{in}|}{v_{bus}} \tag{30}$$

Unlike leading-edge modulation, in which a duty cycle is applied at $k+1$, a leading-triangule modulation distributes the duty change to both the rising and falling edges. So, even though the calculated duty cycle is not applied in one switching event (either rising or falling edge of PWM pulse), the next event will have enough time to execute (see Fig. 5). Therefore, the duty applied at $k+1$ is, $\frac{D[k]+D[k+1]}{2}$ and the duty variation at time $k+1$ can be calculated as,

$$\Delta d[k+1] = \frac{\Delta i_L[k+1] Z_0}{v_{bus}} - \frac{\Delta i_L[k+1]}{2} \cdot \frac{Z}{v_{bus}} \tag{31}$$

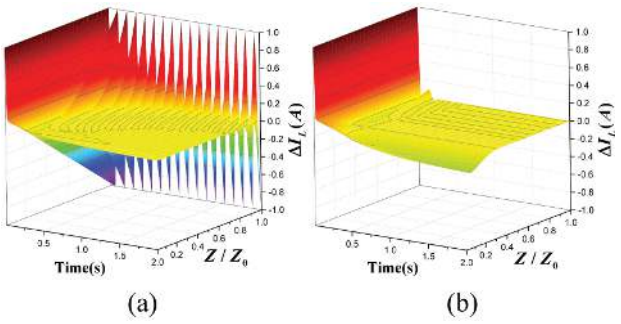

Fig. 6: Current perturbation for the proposed interleaved predictive PFC control with one-cycle delay in case of (a) leading edge modulation, (b) leading triangle modulation

and the resulting current perturbation is

$$\Delta i_L[k+2] = \Delta i_L[k+1] - \frac{Z}{2Z_0}(\Delta i_L[k+1] + \Delta i_L[k]) \quad (32)$$

which can be re-written as

$$\Delta i_L[k+2] = \left(1 - \frac{Z}{2Z_0}\right)\Delta i_L[k+1] - \frac{Z}{2Z_0}\Delta i_L[k]. \quad (33)$$

The discrete time expression (33) can be transformed into z domain

$$\Delta i(z) = (1-\Gamma)\Delta i(z)z^{-1} - \Gamma\Delta i(z)z^{-2} + u(z), \quad (34)$$

where $\Gamma = \frac{Z}{2Z_0}$ and $u(z)$ is the input of the system. Solving the equation (34) for $\Delta i(z)$ yields

$$\Delta i(z) = \frac{u(z)z^2}{z^2 - (1-\Gamma)z + \Gamma}. \quad (35)$$

The system is stable if and only if all of its poles are strictly inside the unit circle,

$$\left|\frac{(1-\Gamma) \pm \sqrt{(1-\Gamma)^2 - 4\Gamma}}{2}\right| < 1 \quad (36)$$

which is always true for $Z < Z_0$.

The three-dimensional plot of current perturbation Δi_L vs. time, for different values of Z, in case of the leading-triangle modulation with one-cycle delay, is shown in Fig 6(b). A 1 A current perturbation is applied in the first two sampling cycles. For a comparison, a plot for leading-edge modulation with the same perturbation applied is shown in Fig 6(a). As shown in Fig. 6, the system is stable with the current perturbation. Also, compared to the leading-edge modulation, the leading-triangle modulation exhibits less oscillations and faster damping.

V. Controller Implementation

The implementation of the proposed multi-level boost predictive controller is shown in Fig 7. The figure shows a generalized implementation extended to a topology with M TLB modules. The controller updates the duty cycles of all the switches at the interleaving frequency, which corresponds to $N = 2M$ times the switching frequency of each TLB switch (Nf_{sw}). It should be noted that the only two switches

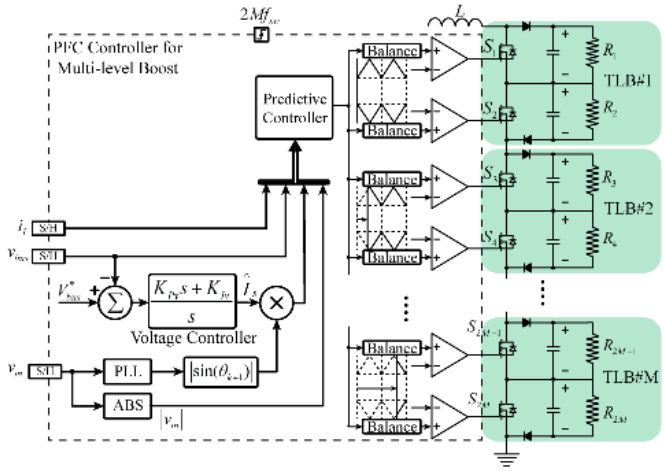

Fig. 7: Proposed predictive control applied to a N-switch M-TLB-Module Multi-level Boost topology

may be affected in any controller execution cycle (see Fig. 4). The inductor current i_L, the dc bus voltage V_{bus} and the input voltage V_{in} are sampled at the same rate (Nf_{sw}). The predictive controller determines the duty cycle based on (15), which requires the values of i_{avg_ref}, i_L, v_{bus}, and $|v_{in}|$. The values of i_L, v_{bus}, and $|v_{in}|$ are sampled, while i_{avg_ref} is calculated by the dc bus voltage controller.

The dc bus voltage controller uses proportional-integral (PI) control, and serves as an outer loop that regulates the V_{bus} indirectly by controlling the magnitude of the input inductor current. In dual-loop current control, the outer loop bandwidth is usually 10-20 times lower than the inner loop bandwidth [27]. Since the current controller's bandwidth is near infinite when applying predictive control, the bandwidth of the voltage loop can be increased to achieve a better dynamic performance. We have selected the bandwidth of the bus voltage controller to be $\frac{1}{20}$ of the switching frequency. The dc bus control can be written as.

$$\hat{I}_s = K_{Pv} \cdot (V^*_{bus} - v_{bus}) + K_{Iv} \cdot \int_0^t (V^*_{bus} - v_{bus})dt \quad (37)$$

To generate the next state sinusoidal reference i_{ref_ave}, the controller implements a phase-locked-loop (PLL) algorithm based on the sampled ac input voltage v_{in}, and generates $|\sin(\theta_{k+1})|$ from the PLL output. The implementation of the PLL is based on [53], where the grid voltage signal $v = v_{grid}\sin(\theta_{in}) = v_{grid}\sin(\omega_{grid}t + \theta_{grid})$ is multiplied by the cosine of the PLL's output angle $v' = \cos(\theta_{out}) = \cos(\omega_{PLL}t + \theta_{PLL})$. Applying a trigonometric identity gives,

$$v_d = \frac{v_{grid}}{2}[sin((\omega_{grid} - \omega_{PLL})t + (\theta_{grid} - \theta_{PLL})) + sin((\omega_{grid} + \omega_{PLL})t + (\theta_{grid} + \theta_{PLL}))] \quad (38)$$

Then a notch filter followed by a PI controller was applied to filter out the double-frequency component and high-frequency noise coming from the phase detector. In steady state operation, the $(\omega_{grid} - \omega_{PLL})t$ is negligible and $sin(\theta_{grid} - \theta_{PLL})$ can be approximated with $\theta_{grid} - \theta_{PLL}$ (since the angle difference is small), which yields,

$$err = \frac{v_{grid}(\theta_{grid} - \theta_{PLL})}{2} \tag{39}$$

Finally, the filter's output err is used in the VCO to obtain the $sin(\theta_{out})$ and $cos(\theta_{out})$ as follows:

$$\sin(\theta_{out}) = \sin(\int(\omega_0 + K_o \cdot err)dt) \tag{40}$$

$$\cos(\theta_{out}) = \cos(\int(\omega_0 + K_o \cdot err)dt) \tag{41}$$

The current reference is then a product of the sinusoidal reference and the voltage controller output.

$$i_{ref\_ave}[k+1] = |\sin(\theta_{k+1})| \cdot \hat{I}_s \tag{42}$$

Besides controlling the overall dc bus voltage V_{bus}, a multi-level converter control must ensure that the voltages across all capacitors v_{cap_i}, are balanced [28]. Thus, an additional voltage balancing loop is needed. A summary of state-of-the-art capacitor voltage balancing approaches is given in [54]. In this work, we apply a simple proportional integral (PI) controller to *N-1* capacitors. The bandwidth of the PI controllers are set 5x higher than the main outer voltage loop to ensure that the balancing control can compensate the disturbance during the transition of the main voltage regulation. The target split dc bus capacitor voltage is selected by averaging all the dc bus voltages,

$$\hat{V}_{balance} = \frac{\sum_{i=1}^{N} v_{cap\_i}}{N} \tag{43}$$

Thus, for the first N-1 switch, the extra duty needed for the balancing function is,

$$\begin{aligned}\Delta D_{balance\_i} &= K_{Pb} \cdot (\hat{V}_{balance} - v_{cap\_i}) \\ &+ K_{Ib} \cdot \int_0^t (\hat{V}_{balance} - v_{cap\_i})dt,\ i \in [1, N-1]\end{aligned} \tag{44}$$

In order to fully decouple the split dc bus balancing control with the main voltage controller, the *N-th* switch ensures that the total balancing duty is 0.

$$\Delta D_{balance\_N} = -\sum_{i=1}^{N-1} \Delta D_{balance\_i} \tag{45}$$

Therefore the duty cycle becomes,

$$d_{applied\_i} = d + \Delta D_{balance\_i}, \quad i \in [1, N] \tag{46}$$

VI. Simulation Results

The controller is tested in a converter topology adopted from [11], [38] and shown in Fig. 8, with 2.4 kVac at its input. The topology consists of a diode rectifier, three input-series-connected TLB converters, and three isolated dc/dc converters connected in parallel at the output. The output of each TLB converter feeds into two dc-link capacitors, with 800 V across each capacitor. The isolated dc/dc converters transfer the energy to the resistive load at the output, at the rated output votlage of 400 V. The proposed predictive control approach is simulated in PSIM simulation software.

To simplify the simulation, the NPC load stage is modeled as a resistive load. The total load was varied from 15 kW to 50 kW. Also, for the comparison a PI current controller is designed based on [55], which provides a detailed parameter selection strategy to achieve optimal THD performance for the PFC. The control parameters of the *PI* current loop are determined using the following equations [55].

$$K_{pI,PI} = \frac{1}{|G_{PL,I}(f_{CI,PI})| \cdot \sqrt{1 + (\frac{f_{ZCC}}{f_{CI,PI}})}} \tag{47}$$

$$K_{iI,PI} = 2\pi f_{ZCC} K_{pI,PI}$$

where $|G_{PL,I}(f_{CI,PI})|$ is the magnitude of the controlled plant transfer function $\frac{V_o}{sL}$ at the crossover frequency, and f_{ZCC} is the zero frequency of the current compensator. Based on the system presented in [11], the parameters for the simulation comparison can be calculated as $K_{pI,PI} = 0.0228$ and $K_{iI,PI} = 43003$

The simulation results are shown in Fig. 9, and the simulated THD is plotted in Fig 10. These results show that the predictive controller's performance is not affected by moderate load variation.

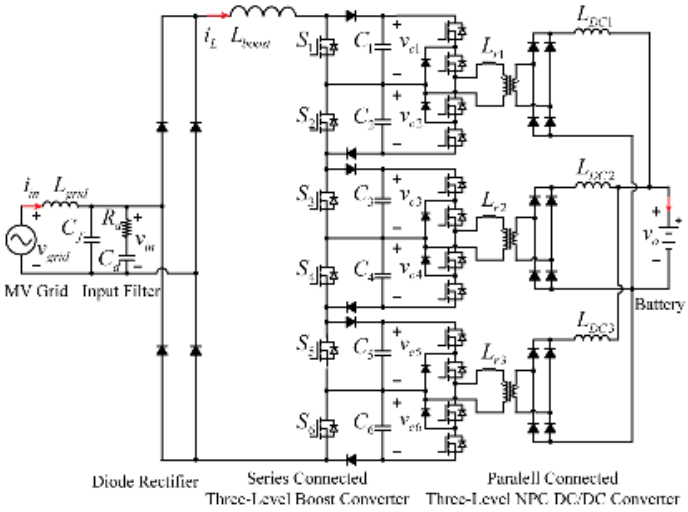

Fig. 8: Topology from [11] used to test the proposed predictive control

The simulations of the effects of parameter sensitivity and one-cycle delay are performed using an inductor with the inductance varying from 0.8 mH at no current to 0.74 mH at input current of 18 A RMS. The simulation results with wrongly estimated input inductance of 0.75 mH and 0.6 mH are shown in Fig 11. All simulations are done at 50 kW output power, 10 kHz switching frequency, 2.4 kV input voltage and 400 V output voltage. The measurement errors are simulated by adding Gaussian white noise with maximum magnitude of 0.15 A to the current feedback samples. The results show that the input inductance value (green trace) rolls off as the input current level increases. An overestimation of the inductance (yellow trace) results in current oscillations. The simulation results for the proposed controller with a leading-edge modulation and a leading-triangle modulation, both with 1 μs calculation delay, are shown in Fig 12. The results show

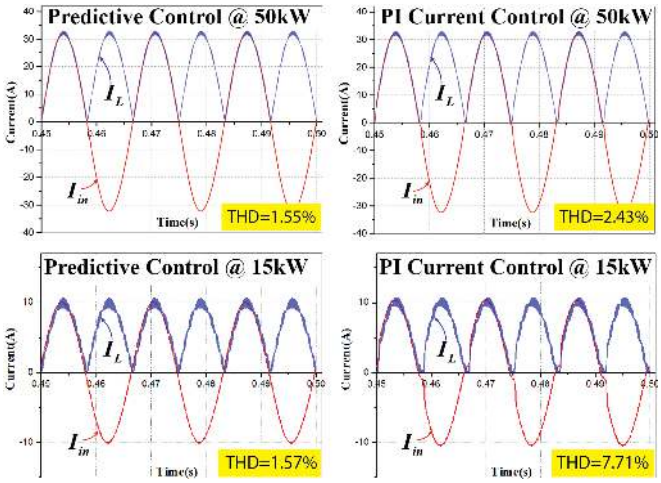

Fig. 9: Comparison of the proposed predictive control with a *PI* controller from [55]

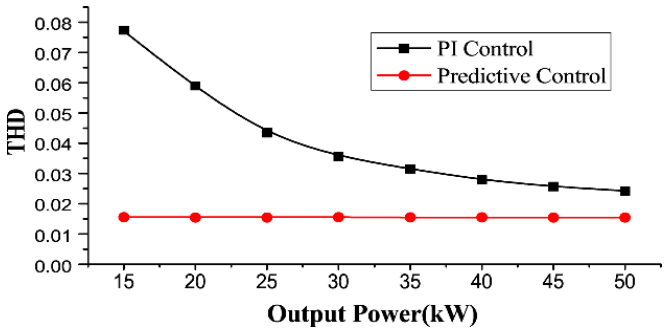

Fig. 10: The input current THD for the proposed predictive control and the *PI* control at different loads

that the leading edge modulation results in one-cycle delay oscillation, while the leading-triangle modulation performs stably. In order to compare the dynamic performance of one-cycle and two-cycle prediction methods, a controller with a two-cycle prediction is developed and its response to a step change in the input current is compared with the response of the one-cycle prediction method. The current reference peak value was changed from 12.5 A to 16.5 A at time 0.195 s, as shown in Fig 13. The measurement errors, inductance variation and the calculation delay are kept the same as for the parameter sensitivity analysis illustrated in Fig. 11 and 12. The simulations show that the two-cycle prediction method is more sensitive to the inductance and measurement errors, and that the overshoot and the settling time are worse in the case with the two-cycle prediction.

VII. Experimental Results

A 50 kW converter prototype, shown in Fig. 14, with the topology from Fig. 8 is built and used to validate the proposed controller. The semiconductor devices and passives used in the prototype converter are listed in TABLE II. The predictive PFC control strategy and NPC control algorithms are implemented on a TMS320F28377D Dual-Core Delfino Microcontroller. The high bandwidth predictive PFC control is executed on one of the two available processor cores, while the low-bandwidth control algorithms including the bus voltage control, NPC output voltage control and the split bus voltage

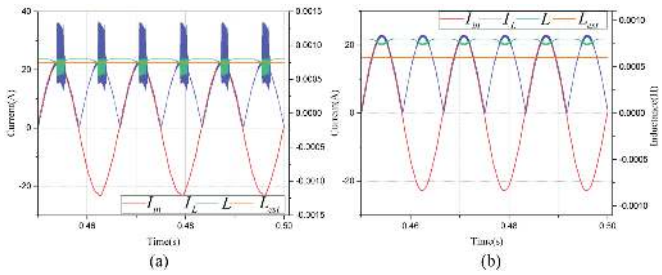

Fig. 11: The sensitivity of the proposed controller to parameter variations: (a) an input inductance of 0.75 mH is used in the predictive equation, and (b) an input inductance of 0.6 mH is used in the predictive equation

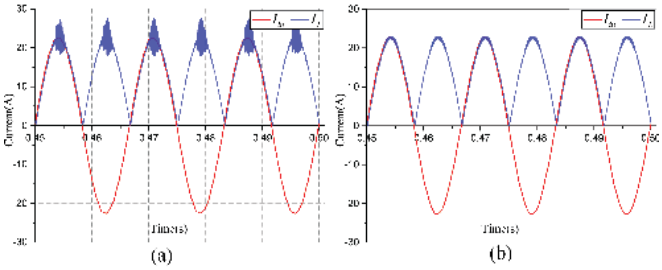

Fig. 12: Modulation method comparison between (a) leading edge modulation and (b) leading triangular modulation with 1 $\mu s calculation delay$

control are executed on the other core. The high bandwidth control algorithm executes in 3 µs. Therefore, the one cycle prediction can easily be accommodated, since the predictive control calculations can take up to 16.6 µs and still ensure stable one-cycle prediction implementation.

The estimated inductance is selected to be 0.6 mH to aviod any instability issues. First, the proposed control is validated on a single TLB converter (N=2, M=1), the obtained waveforms for the moderate load testing are shown in Fig. 15(a) and the corresponding input current THD and lower-order harmonics are shown in Fig. 15(b). The single-TLB tests are performed at 7.85 kW output power, with 500 V RMS input voltage and 1100 V across both TLB capacitors.

The controller operation is then validated on a multilevel converter shown in Fig. 6, with 2.2 kV RMS at the input, 4.8 kV dc bus voltage, 400 V dc output and 50 kW. The obtained waveforms are shown in Fig. 16(a), and the corresponding input current THD and lower-order harmonics are shown in Fig. 16(b). As can be seen in Fig. 16(b), the input current is more distorted than in the case of single TLB module (Fig. 15(b). This is because of the significant low-order harmonics that were present in the grid voltage at the time of the tests (5th and 11th harmonics were dominant). Since the applied control approach uses a PLL-generated pure sinusoidal waveform rather than the measured input voltage waveform (to eliminate the noise in the sensed input voltage signal), the low-order harmonics in the input voltage propagate into the input current (as can be seen Fig. 16(b) where 5th and 11th harmonics are dominant). This can be easily eliminated by adding the dominant low-order input voltage harmonics to the generated sinusoidal reference.

In order to compare the performance of the proposed predictive controller to the traditional PI controller, both controllers are tested in the MV fast charger system, at 25

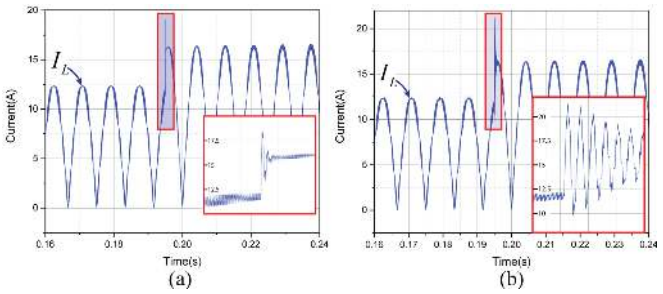

Fig. 13: Step response comparison between (a) one-cycle prediction and (b) two-cycle prediction

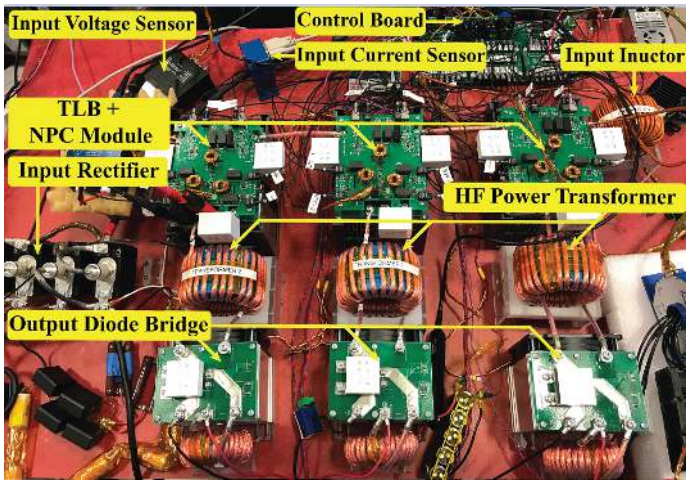

Fig. 14: MV fast charger as the testbench for the proposed predictive PFC control

kW load. The traditional PI controller was used in the early development stage of the MV fast charger, but it was later replaced by the better performing proposed predictive control. Moving to the proposed predictive controller has enabled a reduction in capacitance of each output capacitor from 1100 µF to 180 µF and a reduction in switching frequency (and therefore the losses) from 25 kHz to 10 kHz, and still having the input current THD lower than in the previous system with the PI controller. The test results for both controllers were shown in Fig. 17 and Fig. 18. The PI controller was optimized for the smallest input current waveform distortion around zero-crossing points (to achieve the smallest THD), therefore the slight oscillations in the input voltage and current of the PI response.

Comparing the results for the predictive control at different power levels (i.e. Fig. 16 and 17), it can be seen that better THD was achieved in the 25 kW test. This is mainly because of the smaller output capacitors voltage ripple at smaller output power. To further investigate the sensitivity of the proposed controller to the load change, another test at 15 kW load (30% of the rated load) is performed under same voltage conditions as the 25 kW test (1.8 kV RMS at the input and 300 V dc at the output). The obtained waveforms and the corresponding harmonic analysis windows are shown in Fig. 19. The results show slight deterioration of the input current THD at light load, which is not consistent with the simulation result shown in Fig. 10. This is because the modules in the converter prototype are not identical, and the small differences

TABLE II: Device Selection List for the MV Fast Charger Testbench

Component	Part No.
Input Rectifier Diodes	SKNa 102/45
Boost & NPC MOSFEs	APTMC120AM55CT1AG
Boost & NPC Diodes	APT2X60DC120J
NPC DC Side Diode Bridge	APT40DC120HJS
Input Inductor	800 μH
DC Bus Capacitor	TDK MKP1848S$\times$9
Ouput Inductor	70 µH

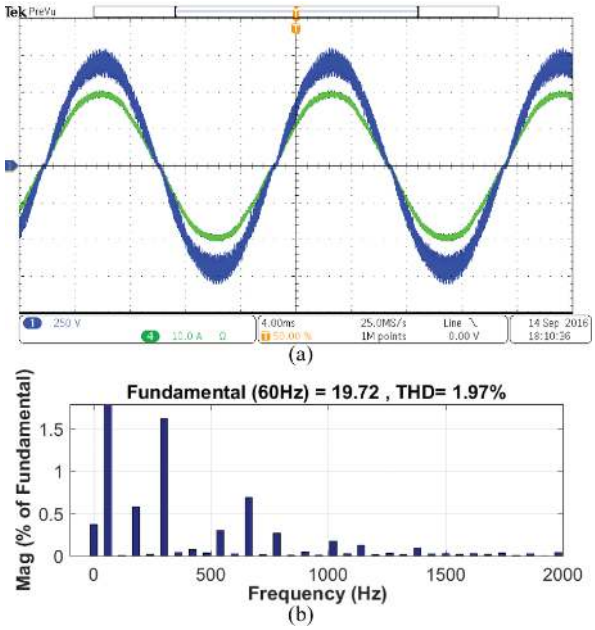

Fig. 15: Test results for a single TLB module, with 500 V RMS at the input, 7.85 kW load: (a) the steady state response of the system, (b) corresponding harmonic analysis window. The blue trace represents input voltage and the green trace represents input current

between the modules would cause a slight unbalance of the dc link voltages. To achieve the dc link voltage balancing, the *PI*-based balancing controllers are implemented, as described in Section V. The balancing controllers keep the capacitors' voltage balanced by slightly correcting the duty cycle of each of TLB's switches. At moderate load operation, this additional part of the duty cycle is negligible compared to the part coming from the predictive controller. However, at light load, the part of the duty cycle coming from the predictive controller becomes smaller and the effect of the balancing part of the duty cycle becomes more pronounced. In simulations, the modules were identical and no balancing action was necessary.

VIII. Conclusions

A new predictive controller for series-interleaved multi-cell three-level boost power factor correction converter has been presented in this paper. The proposed controller uses a universal equation for all operating regions of the multi-cell three-level boost converter, which substantially reduces the control complexity and improves controller stability. The proposed controller works at the interleaved frequency and the generated next state duty cycle is applied to every switch of

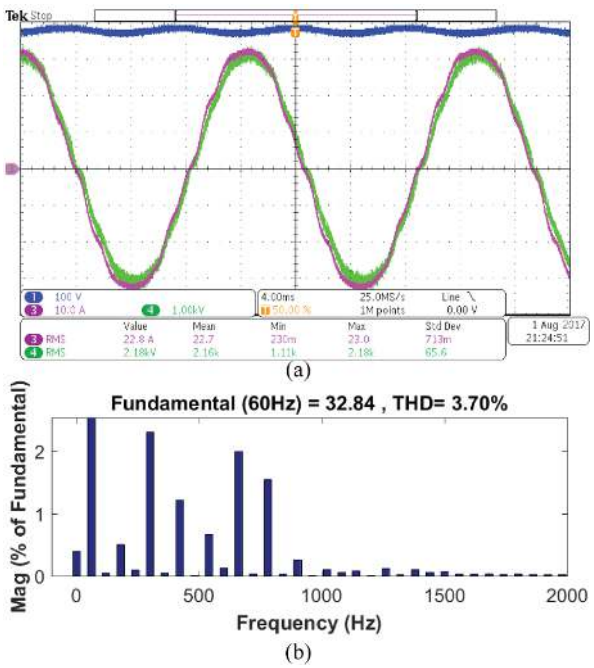

Fig. 16: Test results for 3 series-connected TLBs, with 2.2 kV RMS at the input, 50 kW load: (a) the steady state response of the system, (b) corresponding harmonic analysis window. The blue trace represents the output voltage, magenta trace represents input current and the green trace represents input voltage

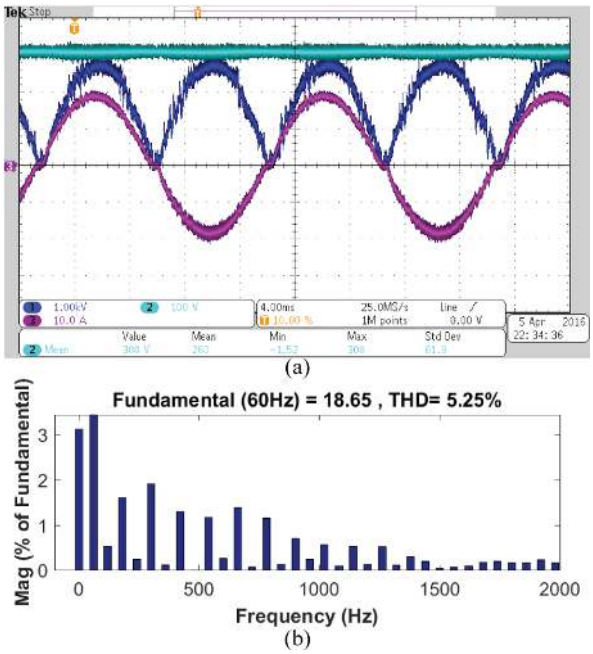

Fig. 18: Test results for 3 series-connected TLBs with PI control at the same working condition as in Fig. 17: (a) the steady state response of the system, (b) corresponding harmonic analysis window. dark blue trace represents rectified input voltage, light blue trace represents dc output voltage, and purple trace represents input current

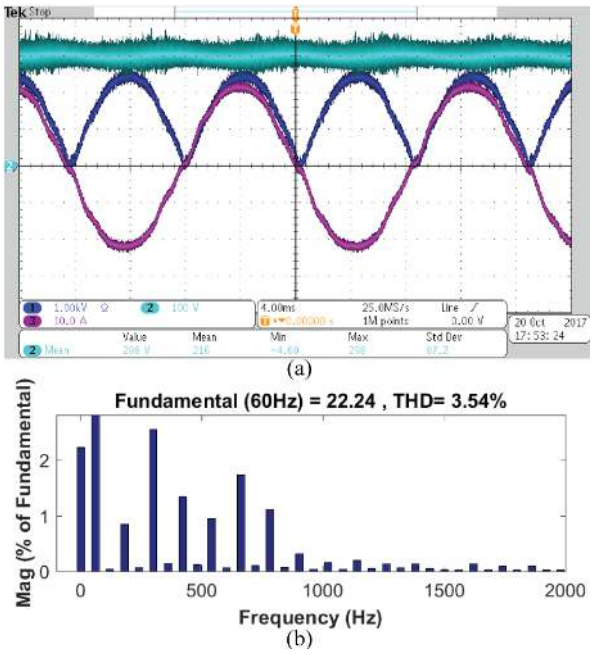

Fig. 17: Test results for 3 series-connected TLBs with proposed predictive control, at 2.2 kV RMS at the input, 25 kW load: (a) the steady state response of the system, (b) corresponding harmonic analysis window. dark blue trace represnets rectified input voltage, light blue trace represents dc output voltage, and purple trace represents input current

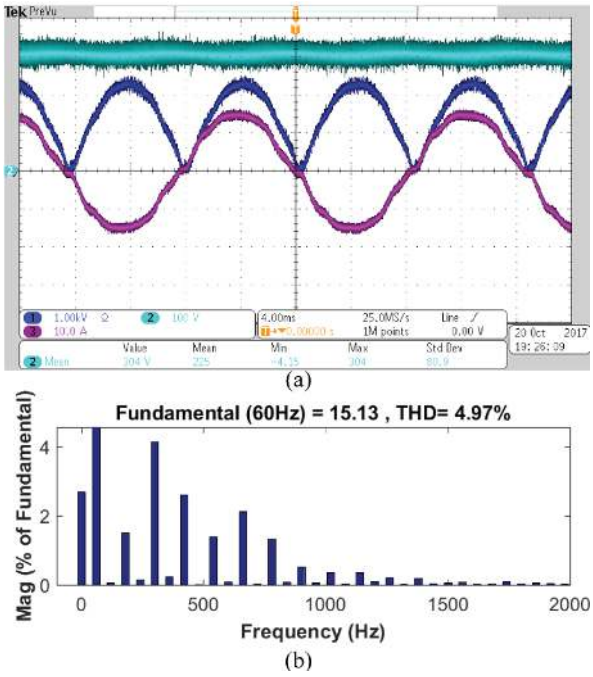

Fig. 19: Test results for 3-series-connected TLBs, with 1.8 kV RMS at the input, 15 kW load: (a) the steady state response of the system and (b) corresponding harmonic analysis window. The dark blue trace represents rectified input voltage, light blue trace represents dc output voltage, and purple trace represents input current

the multi-cell three-level boost simultaneously, thus providing the fastest achievable control. Furthermore, the proposed controller benefits from the inherent advantages of the predictive control over the average model based current control, thus improving the performance around the current zero crossing and minimizing the THD. Due to the high bandwidth and high dc gain, the proposed method is able to shrink the volume of the passive components including the input filter, line inductor and the dc-link capacitors. The simulation and experimental results show that the proposed predictive control method performs very well in achieving the control goals for the 50 kW MV converter that can be used in EV fast charging,

data center power supply, or other dc power distribution applications.

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REFERENCES

[1] M. Kang, P. N. Enjeti, and I. J. Pitel, "Analysis and design of electronic transformers for electric power distribution system," *IEEE Transactions on Power Electronics*, vol. 14, no. 6, pp. 1133–1141, 1999.

[2] E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronic-based distribution transformer," *IEEE Transactions on Power Delivery*, vol. 17, no. 2, pp. 537–543, 2002.

[3] S. Bifaretti, P. Zanchetta, A. Watson, L. Tarisciotti, and J. C. Clare, "Advanced power electronic conversion and control system for universal and flexible power management," *IEEE Transactions on Smart Grid*, vol. 2, no. 2, pp. 231–243, 2011.

[4] X. She, X. Yu, F. Wang, and A. Q. Huang, "Design and demonstration of a 3.6-kv–120-v/10-kva solid-state transformer for smart grid application," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3982–3996, 2014.

[5] D. Rothmund, G. Ortiz, and J. Kolar, "Sic-based unidirectional solid-state transformer concepts for directly interfacing 400v dc to medium-voltage ac distribution systems," in *Telecommunications Energy Conference (INTELEC), 2014 IEEE 36th International*. IEEE, 2014, pp. 1–9.

[6] R. J. G. Montoya, A. Mallela, and J. C. Balda, "An evaluation of selected solid-state transformer topologies for electric distribution systems," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*. IEEE, 2015, pp. 1022–1029.

[7] A. Pratt, P. Kumar, and T. V. Aldridge, "Evaluation of 400v dc distribution in telco and data centers to improve energy efficiency," in *Telecommunications Energy Conference, 2007. INTELEC 2007. 29th International*. IEEE, 2007, pp. 32–39.

[8] B. Hafez, H. S. Krishnamoorthy, P. Enjeti, S. Ahmed, and I. J. Pitel, "Medium voltage power distribution architecture with medium frequency isolation transformer for data centers," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*. IEEE, 2014, pp. 3485–3489.

[9] G. Zhabelova, A. Yavarian, V. Vyatkin, and A. Q. Huang, "Data center energy efficiency and power quality: An alternative approach with solid state transformer," in *Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE*. IEEE, 2015, pp. 001 294–001 300.

[10] M. Vasiladiotis and A. Rufer, "A modular multiport power electronic transformer with integrated split battery energy storage for versatile ultrafast ev charging stations," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 3213–3222, 2015.

[11] S. Srdic, X. Liang, C. Zhang, W. Yu, and S. Lukic, "A sic-based high-performance medium-voltage fast charger for plug-in electric vehicles," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–6.

[12] D. Sha, G. Xu, and Y. Xu, "Utility direct interfaced charger/discharger employing unified voltage balance control for cascaded h-bridge units and decentralized control for cf-dab modules," *IEEE Transactions on Industrial Electronics*, 2017.

[13] J. E. Huber and J. W. Kolar, "Solid-state transformers: On the origins and evolution of key concepts," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 19–28, 2016.

[14] W. van der Merwe and T. Mouton, "Solid-state transformer topology selection," in *Industrial Technology, 2009. ICIT 2009. IEEE International Conference on*. IEEE, 2009, pp. 1–6.

[15] S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Power and Energy Society General Meeting, 2010 IEEE*. IEEE, 2010, pp. 1–8.

[16] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, 2013.

[17] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Applied Power Electronics Conference and Exposition, 1995. APEC'95. Conference Proceedings 1995., Tenth Annual*, vol. 1. IEEE, 1995, pp. 434–439.

[18] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac-dc converters," *IEEE Transactions on industrial electronics*, vol. 50, no. 5, pp. 962–981, 2003.

[19] B. Mahdavikhah and A. Prodić, "Low-volume pfc rectifier based on nonsymmetric multilevel boost converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1356–1372, 2015.

[20] J. Pinheiro, D. Vidor, and H. Grundling, "Dual output three-level boost power factor correction converter with unbalanced loads," in *Power Electronics Specialists Conference, 1996. PESC'96 Record., 27th Annual IEEE*, vol. 1. IEEE, 1996, pp. 733–739.

[21] M. Rajesh and B. Singh, "Analysis, design and control of single-phase three-level power factor correction rectifier fed switched reluctance motor drive," *IET power Electronics*, vol. 7, no. 6, pp. 1499–1508, 2014.

[22] H. Ma, C. Yang, and Y. Zhang, "Analysis and design for single-phase three-level boost pfc converter with quasi-static model," in *IECON 2011-37th Annual Conference on IEEE Industrial Electronics Society*. IEEE, 2011, pp. 4385–4390.

[23] B.-R. Lin, H.-H. Lu, and Y.-L. Hou, "Single-phase power factor correction circuit with three-level boost converter," in *Industrial Electronics, 1999. ISIE'99. Proceedings of the IEEE International Symposium on*, vol. 2. IEEE, 1999, pp. 445–450.

[24] B.-R. Lin, C.-N. Wang, and H. H. Lu, "Multilevel ac/dc/ac converter by using three-level boost rectifier and five-level diode clamped inverter," in *Power Electronics and Drive Systems, 1999. PEDS'99. Proceedings of the IEEE 1999 International Conference on*, vol. 1. IEEE, 1999, pp. 444–449.

[25] B. Lin and H. H. Lu, "A novel pwm scheme for single-phase three-level power-factor-correction circuit," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 2, pp. 245–252, 2000.

[26] B. Lin and H. Lu, "Single-phase power-factor-correction ac/dc converters with three pwm control schemes," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 36, no. 1, pp. 189–200, 2000.

[27] H.-C. Chen and J.-Y. Liao, "Multiloop interleaved control for three-level switch-mode rectifier in ac/dc applications," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3210–3219, 2014.

[28] ——, "Design and implementation of sensorless capacitor voltage balancing control for three-level boosting pfc," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3808–3817, 2014.

[29] V. Yaramasu and B. Wu, "Three-level boost converter based medium voltage megawatt pmsg wind energy conversion systems," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*. IEEE, 2011, pp. 561–567.

[30] H.-C. Chen and J.-Y. Liao, "Modified interleaved current sensorless control for three-level boost pfc converter with considering voltage imbalance and zero-crossing current distortion," *IEEE Transactions on industrial electronics*, vol. 62, no. 11, pp. 6896–6904, 2015.

[31] M. F. Schlecht, "Harmonic-free utility/dc power conditioning interfaces," *IEEE transactions on power electronics*, no. 4, pp. 231–239, 1986.

[32] S. Wall and R. Jackson, "Fast controller design for single-phase power-factor correction systems," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 5, pp. 654–660, 1997.

[33] J.-H. Park, D. J. Kim, and K.-B. Lee, "Predictive control algorithm including conduction-mode detection for pfc converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 9, pp. 5900–5911, 2016.

[34] M. Chen and J. Sun, "Feedforward current control of boost single-phase pfc converters," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 338–345, 2006.

[35] S. Kouro, P. Cortés, R. Vargas, U. Ammann, and J. Rodríguez, "Model predictive controla simple and powerful method to control power converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1826–1838, 2009.

[36] V. Yaramasu and B. Wu, "Predictive control of a three-level boost converter and an npc inverter for high-power pmsg-based medium voltage wind energy conversion systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5308–5322, 2014.

[37] J. Baggio, H. Hey, H. Grundling, H. Pinheiro, and J. Pinheiro, "Discrete control for three-level boost pfc converter," in *Telecommunications Energy Conference, 2002. INTELEC. 24th Annual International*. IEEE, 2002, pp. 627–633.

[38] S. Srdic, C. Zhang, X. Liang, W. Yu, and S. Lukic, "A sic-based power converter module for medium-voltage fast charger for plug-in electric vehicles," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 2714–2719.

[39] J. Baggio, H. Hey, H. Grundling, H. Pinheiro, and J. Pinheiro, "A pfc rectifier for telecommunications high power applications," in *Telecommunications Energy Conference, 2002. INTELEC. 24th Annual International*. IEEE, 2002, pp. 634–640.

[40] D. Draghici, M. Gurbina, A. Ciresan, and D. Lascu, "Predictive leading-edge modulation average current control in dc-dc converters," in *Optimization of Electrical and Electronic Equipment (OPTIM), 2014 International Conference on*. IEEE, 2014, pp. 588–594.

[41] S. Chattopadhyay, V. Ramanarayanan, and V. Jayashankar, "A predictive switching modulator for current mode control of high power factor boost rectifier," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 114–123, 2003.

[42] W. Zhang, G. Feng, Y.-F. Liu, and B. Wu, "Dsp implementation of predictive control strategy for power factor correction (pfc)," in *Applied Power Electronics Conference and Exposition, 2004. APEC'04. Nineteenth Annual IEEE*, vol. 1. IEEE, 2004, pp. 67–73.

[43] P. Athalye, D. Maksimovic, and R. Erickson, "Dsp implementation of a single-cycle predictive current controller in a boost pfc rectifier," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, vol. 2. IEEE, 2005, pp. 837–842.

[44] R. Redl and B. P. Erisman, "Reducing distortion in peak-current-controlled boost power-factor correctors," in *Applied Power Electronics Conference and Exposition, 1994. APEC'94. Conference Proceedings 1994., Ninth Annual*. IEEE, 1994, pp. 576–583.

[45] M. Schupbach, B. Agrawal, and N. Mangal, "A digital predictive constant frequency controller for high frequency 3-phase silicon carbide pfc rectifier," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*. VDE, 2016, pp. 1–8.

[46] H.-S. Youn, J.-S. Park, K.-B. Park, J.-I. Baek, and G.-W. Moon, "A digital predictive peak current control for power factor correction with low-input current distortion," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 900–912, 2016.

[47] Z. Lu, M. Wang, and L. Zheng, "A predictive averaged current mode control for high power factor boost rectifier," in *Electrical Machines and Systems, 2005. ICEMS 2005. Proceedings of the Eighth International Conference on*, vol. 2. IEEE, 2005, pp. 1228–1231.

[48] L. Lai and P. Luo, "A predictive digital-controlled algorithm for power factor correction converter," in *Communications, Circuits and Systems (ICCCAS), 2013 International Conference on*, vol. 2. IEEE, 2013, pp. 390–393.

[49] Y.-T. Chang and Y.-S. Lai, "Parameter tuning method for digital power converter with predictive current-mode control," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2910–2919, 2009.

[50] J. R. Fischer, S. A. Gonzalez, M. A. Herran, M. G. Judewicz, and D. O. Carrica, "Calculation-delay tolerant predictive current controller for three-phase inverters," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 1, pp. 233–242, 2014.

[51] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 411–419, 2003.

[52] P. Athalye, D. Maksimovic, and R. Erickson, "Variable-frequency predictive digital current mode control," *IEEE Power Electronics Letters*, vol. 2, no. 4, pp. 113–116, 2004.

[53] "28x solar library module user's guide," 2014.

[54] X. She, A. Q. Huang, T. Zhao, and G. Wang, "Coupling effect reduction of a voltage-balancing controller in single-phase cascaded multilevel converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3530–3543, 2012.

[55] L. Huber, M. Kumar, and M. M. Jovanović, "Performance comparison of pi and p compensation in dsp-based average-current-controlled three-boost pfc rectifier," *IEEE Transactions on Power* no. 12, pp. 7123–7137, 2015.

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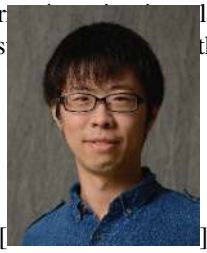

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