6.0kV, 100A, 175kHz Super Cascode Power Module for Medium Voltage, High Power Applications

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***Abstract*— A new 6.0kV/100A Super Cascode Power Module (SCPM) topology is proposed using dual serial strings of six SiC-JFETs with a common balancing circuit, and extendable to 8.0kV/200A for high-frequency, medium-voltage applications. Electrical and multi-physics simulations show improvements in dynamic response, and improved electro-thermal performance that exceed state-of-the-art Si-IGBT power module technology. The SCPM is fabricated and tested. Results are reported showing 47.8mΩ dynamic response, and ≤50ns rise and fall in current at 4kV for 110A switching from double-pulse testing (DPT).**

Keywords—super cascode, JFET, SiC, medium voltage, high power module

I. INTRODUCTION

High frequency switching of *>1kHz* for medium voltage (3.3kV-10kV) power modules continues to be a highly sought after building block of next-generation power electronics systems, from static converters for energy storage and solid-state transformers to industrial motor drives and electrified transportation [1]-[2]. Power modules based on bipolar Si-IGBTs are limited to switching frequencies in the low kHz range due to long turn-off times. Newer wide-bandgap (WBG) devices, e.g. SiC JFETs and GaN HEMTs, have the potential to replace the slower Si-IGBTs at high voltages, for example transitions *>10kV/μs*, [10]-[15]. Using six *1.2kV/16mΩ*, normally-on SiC-JFETs (USCi UJN1202Z dies), a *6.0kV/100A* super cascode power module (SCPM) was designed, fabricated, and tested in the industry standard E3-package to compare electrical and thermal performance with commercial Si-IGBT power modules of similar rating, such as Powerex CM200HG-130H, and Infineon FZ250R65KE3, or with similar *6.5kV* SiC MOSFETS [3]. The internal package was designed to accommodate a GEN-2 higher power rated *1.7kV/6mΩ* normally-on SiC-JFETs (USCi UJ3N1701Z dies) that targets *6.5kV/200A*.

II. SCPM ELECTRICAL CIRCUIT DESIGN & SIMULATION

The earliest SCPM method was initially reported by R. Epelt, et. al. in 2004 [1], and the concept of having a dynamic balancing network was further proposed by J. Biela, et. al. in 2009 [5]. Xueqing Li, et. al. proposed a different SCPM structure [6]. This newly proposed SCPM has a few key differences compared with previously available designs. The new design is optimized for manufacturability, all balancing network capacitors used are less than *2kV* commonly available models, and all balancing network connections are between the gates of each JFET stage. In addition, an FR-4 PCB technology is used to house selected balancing network components so that manufacturing and product varation costs can both be reduced.

In this paper, a newly proposed super cascode electrical topology, Fig. 1, that matches the turn-on and turn-off speeds of the super cascode reported by Biela, et. al., and improves dynamic balancing performance metrics of the previous designs. In the proposed SCPM structure, *R1* provides a bias current for *D1-D5*, which sets the static balancing voltage. The *R2-R6* set rise/fall times of the SCPM, while *C1-C5* are based on gate charge of *Q1-Q5* and body charge of *D1-D5*. Similar to the Biela's structure for each stage, $\Delta Q_C=Q_{DS}-Q_{Diode}$, and $Q_C=\Delta Q_C+\sum(\Delta Q_{C\_higher\_stages})$. Due to uneven power dissipation, which causes the lowest JFET in the string to dissipate much more power than other JFETs during switching, the proposed balancing network is tuned so that its dynamic balancing shifts a portion of the voltage from the lowest JFET, which reduces its power dissipation.

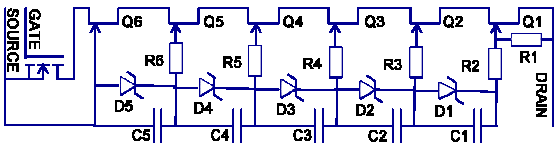

Fig. 1 Single-string super cascode with balance network

During each switching period (turn-on and turn-off), the voltage across adjacent JFETs decreases or increases depending on the blocking voltage of the active device. For instance, if drain potential of *Q2* is *1000V* above drain potential of *Q3* during off-state, then to turn on the SCPM, this voltage has to be reduced to near *0V*. To synchronize all JFETs, a capacitance string is added across the gate terminal of all JFETs. The capacitance of each capacitor is determined to maintain the relationship of any charge flowing through each capacitor and is equal to the charge stored in the drain-source junction of the corresponding JFET (ignoring Q_G, which is negligible compared with Q_{DS}). Due to the fact that the capacitors, *C1-C5*, are connected in series, charge from a higher stage will flow to ground through the lower stage capacitors.

Assuming each stage of an SCPM shares equal voltage in the off-state, then:

$$Q_{C,n}=Q_{C,n-1}+Q_{DS,n+1}, \text{ where } n=1, \ldots, 5 \text{ and } Q_{C,0}=0$$

In this design, all JFETs are the same, hence: $Q_{DS,n}=Q_{DS}$

To achieve equal balance, $V_{DS,n}=V_{DS}$, therefore:

$$C_n=C_{n-1}+Q_{DS}/V_{DS}, \text{ where } n=1, \ldots, 5, \text{ and } C_0=0$$

In this design, Q_{DS} is estimated to be *300nC*, V_{DS} target is *1kV*, therefore *C1=300pF, C2=600pF, C3=900pF, C4=1200pF* and *C5=1500pF*.

Further refinement requires capacitances *C1-C5* be adjusted to offset junction capacitance of avalanche diodes, along with any parasitic routing capacitance. Also, capacitor values need to be rounded to a simple combination of commercially available ceramic capacitors. It is recommended that the capacitors be made of Type I dielectric ceramics, as film capacitors are not suitable for the intended high temperature operation, and Type II and Type III ceramic dielectrics have strong voltage dependency.

In addition, capacitance values, *C1-C5*, can be fine-tuned to intentionally detune the capacitor network to create imbalance voltage sharing. More often than not, the actual operational bus voltage is always lower than the designed maximum voltage of the SCPM. Thus, it is preferable to intentionally allow lower stage JFETs to block lower voltage in order to shift switching loss to higher stage JFETs. Because *V=Q/C*, to increase dynamic blocking voltage of a stage, its corresponding capacitance should be reduced. Alternatively, to reduce dynamic blocking voltage, capacitance should be increased. Taking all of the above concerns into consideration for this design, the resistances, diodes, and capacitances are shown in Table 1.

The proposed SCPM design has two sides, and therefore 2x capacitance is required. The right column reflects actual capacitor combinations shared by both sides in SCPM.

Table 1 LTSpice simulation results using derived capacitance values

Component	Theoretical	Actual	Combination
C1	300pF	275pF	330pF+220pF
C2	600pF	580pF	470pF+470pF+220pF
C3	900pF	900pF	1000pF+470pF+330pF
C4	1200pF	1235pF	1000pF+1000pF+470pF
C5	1500pF	1500pF	1000pF+1000pF+1000pF
R1	Vishay 4MΩ high voltage		
R2~R6	Vishay 10Ω AlN high power		
D1~D5	Vishay AU1PM binned to breakdown slightly below 1400V (UJN1202Z breakdown voltage)		

It should be noted that the intention was to also increase *C5*, but this was prevented by material availability limitations. Moreover, additional capacitance can be placed with larger footprint, but then the concern of increased leakage inductance and increased baseplate coupling arise.

Based on the *R1-R6, D1-D5,* and the actual capacitor values from Table 1, a simulation in LTSpice was performed with USCi's (UJN1202Z) JFET model. Switching power loss for each of the JFETs, *Q1-Q6*, and LV MOSFET (USM141), *Q7*, are in Table 2 under a resistive load with *23nH* ESL.

Table 2 LTSpice simulation results using derived capacitance values for a single super cascode string

	Q1	Q2	Q3	Q4	Q5	Q6	Q7
E_{SW}(mJ)	479.2	658.9	776.6	847. 6	808.6	1008	5.47
V_{Off}(V)	1253	1076	976	923	863	890	15

Simulation results show *4.58W/kHz* worst case power loss per side at *6kV* bus voltage, *100A* resistive load, *50%* duty cycle, *175°C* device junction, and *40°C* baseplate. The SCPM has t_{off}*=22ns and* t_{on}*=49ns*, shown in Fig. 2.

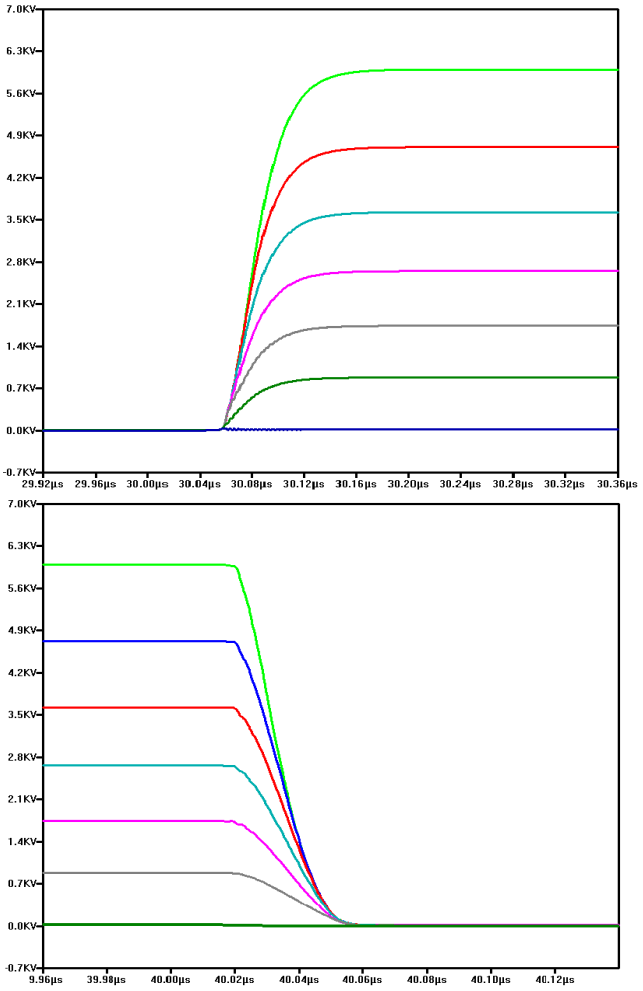

Fig. 2 Simulated SCPM voltage rise/fall across 6 JFETs and MOSFET

III. Static Electrical Test of SCPM

The first SCPM, *S1-6500-100*, was put through initial, static electrical testing in order to qualify the module for testing in several double pulse test circuit configurations. Forward I-V characteristic, Fig. 3a shows an R_{DSon} value of *48mΩ*, and a static reverse leakage current of *1mA* at *4.7kV*, as shown in Fig. 3b.

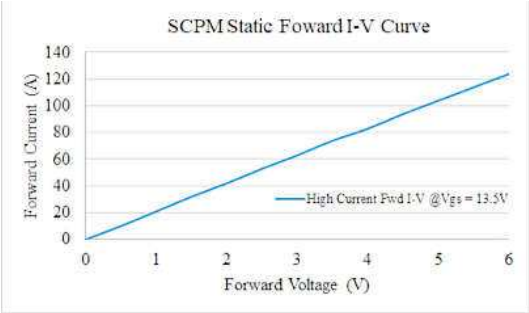

Fig. 3a S1 forward I-V @V_{GS}=13.5V

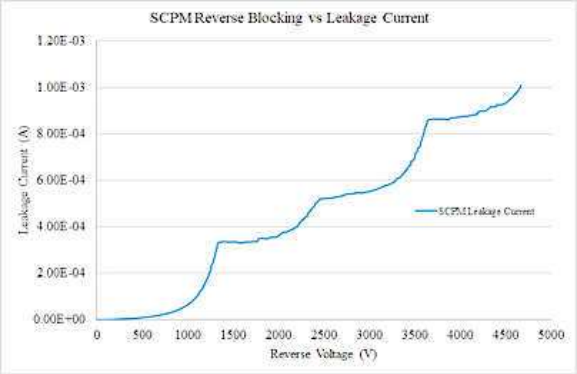

Fig. 3b S1 reverse blocking @V_{GS}=0V

The reverse leakage current plot shows steps due to the "activation" of the different stages, albeit from individual leakage differences. Since there are two parallel strings, each contributes approximately *500μA* at *4.7kV*.

IV. Double Pulse Testing

Three SCPMs (*S1/2/3-6500-100*) were put through DPT along with an *8.5kV/200A* diode module (*D1-8500-200*), which contained four strings of CREE *1.7kV/50A* SiC Schottky Barrier Diodes (SBD) (CPW5-1700-Z050B) placed into the same SCPM E-3 module, Fig. 4.

Fig. 4 An 8.5kV/200A diode module (D1-8500-200) used high-side device in DPT

The DPT circuit and setup, Fig. 5, was used to obtain the results in Table 3 for two configurations of high-side and low-side (DUT) devices. To assist testing, a *6.5kV*, *50A* TO247 discrete JFET-based SCPM (*SD1-6500-50*) was fabricated for SCPM-SCPM DPT.

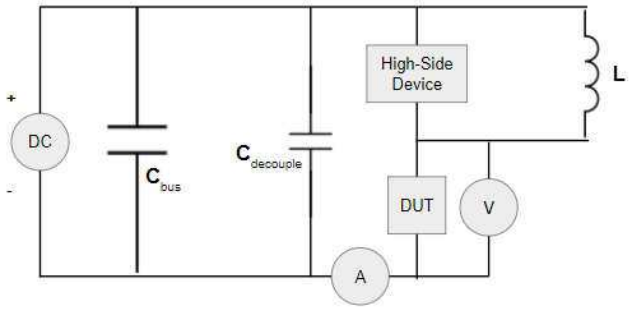

Fig. 5a Double-pulse test circuit schematic

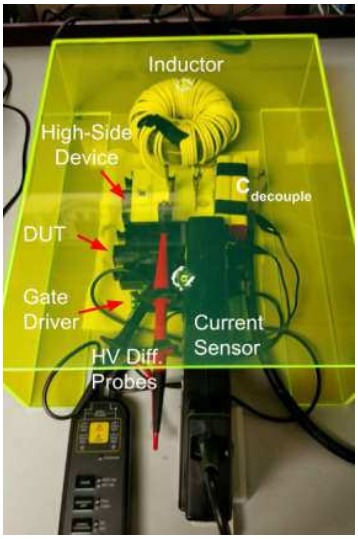

Fig. 5b Double-pulse test physical lab setup

Table 3 DPT Results for different high-side device and low-side device configurations

Devices (HS-LS)	V_{Bus}(V)	I_{Test}(A)	t_{Vr}(ns)	t_{If}(ns)	t_{Vf}(ns)	t_{Ir}(ns)
D1-S1	4000	110	45	50	200	45
SD1-S1	2500	50	75	100	150	28

The DPT setup contained a bus capacitor of *8μF*, a local decoupling capacitor of *0.2μF*, an inductor of *4mH* to obtain test results with DUT voltages and inductor currents similar to the oscilloscope waveforms of Fig. 6 where switching transition times could be extracted, using a *10%-90%* basis.

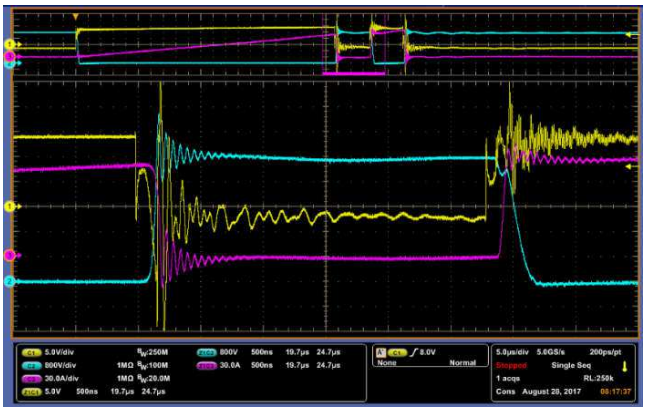

Fig. 6 Diode module as high side and SCPM as DUT at 4kV/110A

Double-pulse test configuration with *SD1* as high side device and *S1* as low side DUT exhibits generally inferior switching speed compared with *D1-S1* configuration because the low side MOSFET of *SD1* has reverse recovery time when operated in 3rd quadrant mode, see Fig. 7 and Fig. 8. This can be mitigated by adding a Schottky diode across the MOSFET of the high side SCPM in future revisions. The measured rising and falling switching times are longer than simulated values because the previous simulation was based on resistive load and hence contained no parasitic capacitance or reverse recovery of the high side device.

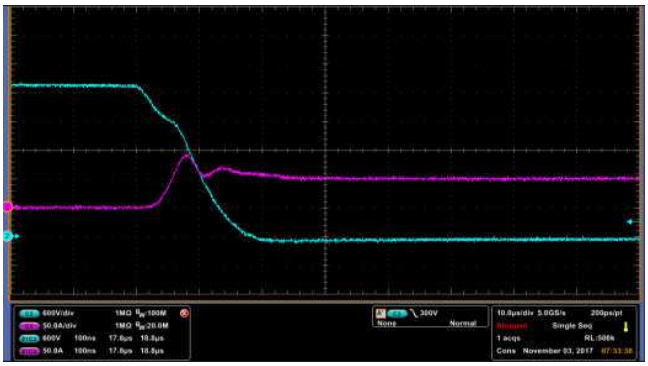

Fig. 7 SCPM as high side and SCPM as DUT at 3kV/50A – turn-on

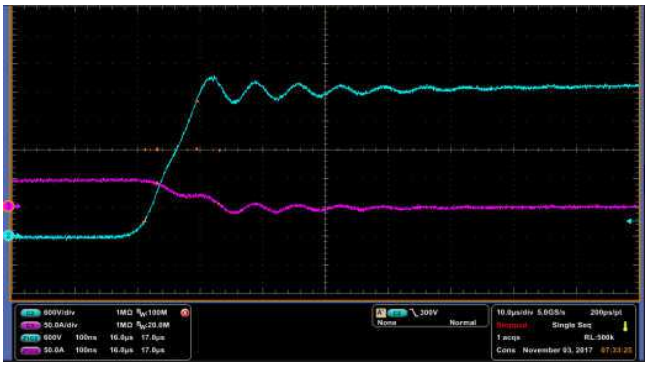

Fig. 8 SCPM as high side and SCPM as DUT at 3kV/50A – turn-off

V. SCPM Fabrication

The SCPM contains two 6 JFETs + 1 MOSFET strings connected in parallel to form a super cascode structure. The first generation *S1-6500-100*, *S2-6500-100* SCPM and *S3-6500-100* use USCi JFET UJN1202Z and MOSFET USM141 to achieve a target rating of *100A* per module. The UJN1202Z die is *5.5 mm X 3.5 mm*, rated *1.2kV/12mΩ*. The USM141 die is *1.93 mm X 2.49 mm*, rated *>20V, 3.6mΩ*. However, the design of the SCPM also accommodates the larger USCi JFET UJ3N1701Z and MOSFET AW1046 to achieve a second generation SCPM of *>200A* per module. The larger layout causes the first generation SCPMs to have a greater resistance, and higher thermal resistance per die with the smaller die.

The SCPMs were fabricated in the NCSU PREES laboratory (Laboratory for Packaging Research in Electronic Energy Systems) using industry compatible equipment and processes, Fig. 9. A standard E3, *0.5 cm* thick, AlSiC baseplate from CPS Technologies with a Cu spray for substrate soldering. Four patterns of substrates were supplied by Remtec, all having *12/25/12 mil Cu/AlN/Cu* cladding. The substrates, two in series and mirrored to form two strings for the JFETs and MOSFETs, had an ENIG finish (*120-280μm Ni / 2-6μm Au*) with solder mask. A four-layer FR-4 PCB formed the balancing circuit and was soldered between the two DBC strings. A three-level solder hierarchy, based on Nordson EFD solder pastes, was used in the sequence: *Sn5/Pb95* for the DBC and PCB substrates to AlSiC baseplate, *Sb5/Sn95* for the JFETs, MOSFETs, and SMDs to the DBC and PCB, and *Sn63/Pb37* for the power and signal terminals. A Hesse-Mechatronics BJ935 heavy-wire bonder, was used to interconnect bare die and SMDs to the DBC and PCB: *15 mil* Al wire for JFET source, *8 mil* Al wire for MOSFET source, and *5 mil* Al wire for device gates and SMDs. A Stratasys Connex 350 Objet 3D printer using rigid opaque photopolymers (VeroWhite and VeroBlack) created the module housings. High temperature 3M epoxy attached housing to baseplate. Wacker SEMICOSIL 915HT silicone gel was used for the HV encapsulation.

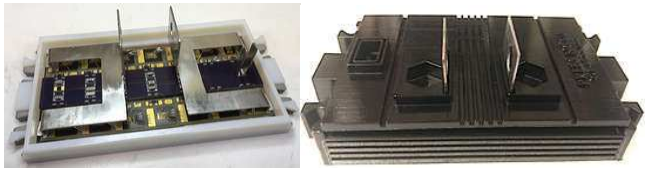

Fig. 9 SCPM S1 and S3: power stage with busbar interconnects and housing body

VI. Power Loop Inductance Analysis

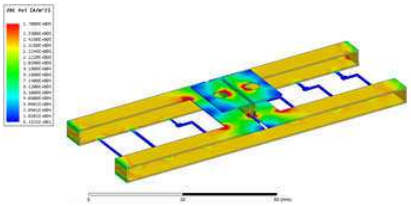

Fig. 10 Simplified 3D CAD model for resistance and inductance simulation

A simplified model of the modified E3-package terminal layout was developed to represent the DBC power traces and internal busbar structure, Fig. 10. Using ANSYS Q3D, a visualization of the current density, Fig. 10, and an inductance of *23nH* at *100kHz* was determined. A commercial *6.5kV* E3-packaged IGBT module typically has *25-50nH* [7].

To characterize the SCPM internal power loop inductance, a "dummy" module containing only power terminals and wire bonded pads was fabricated and inserted into the DPT setup for *4kV/110A* testing. The average measured inductance is *23.15nH* across three measurements, similar to the previously mentioned simulation values.

VII. Thermal Analysis

The SCPM was evaluated with two substrates *12/40/12 mils* and *12/25/12 mils*, soldered on a flat AlSiC baseplate (*0.5 cm* thick), Fig. 11, at *50W* dissipation per JFET and *20W* dissipation per MOSFET. For *40 mil* AlN substrate (for very high voltage), the simulated R_{th,jc_JFET} = *0.57°C/W* (UJN 1202Z), and R_{th,jc_MOSFET} = *0.76°C/W* (AW1046). For *25 mil* AlN substrate, the R_{th,jc_JFET} = *0.45°C/W*, and R_{th,jc_MOSFET} = *0.61°C/W*, Fig. 12. Thermal resistance with *40 mil* DBC is used to calculate maximum operating frequency; see Table 2.

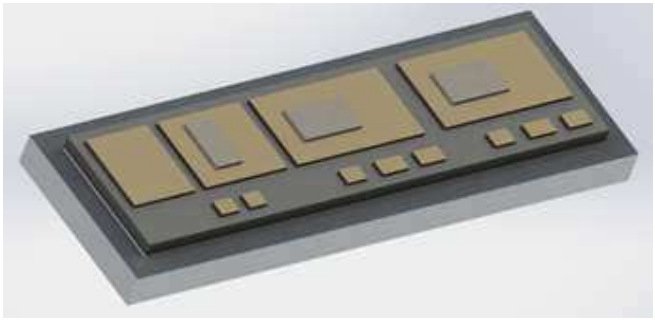

Fig. 11 SCPM substrate 3D CAD rendering

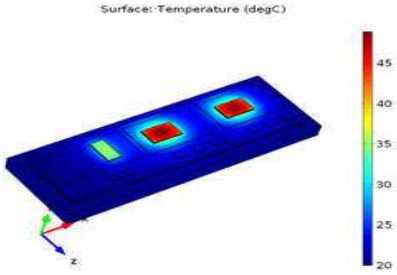

Fig. 12 Temperature distribution of MOSFET and two JEFTS of SCPM

The SCPM was also evaluated with two AlSiC cooling approaches with pin-finned baseplates, Fig. 13 and 14. The pin-finned layout is used in common standard commercial modules. Coolant flow direction is important, since the module has uneven power dissipation, i.e. the JFET closest to the MOSFET generates up to 2X the heat of the other JFETs [9]-[10]. This SCPM design purposely electrically balances the dissipation to bring the power loss of the lower JFET to <*30%* more than the others at *5kV/100A* resistive load, *100kHz* switching. Two coolant chambers were analyzed with one allowing for more mixing at the hotter end, Fig. 14.

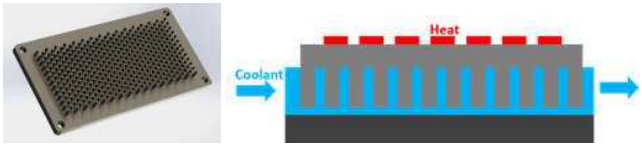

Fig. 13 Conventional pin-fin baseplate and liquid cold plate

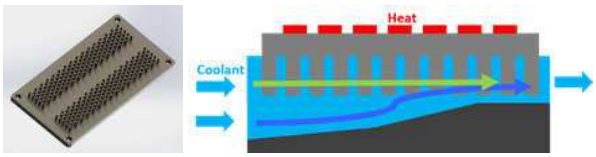

Fig. 14 Proposed pin-fin baseplate and low-temperature gradient cold plate

The FEA analysis based on *25°C* coolant temperature and *25 mil* DBC thickness shows that the temperatures of each die in the gradient cold plate are more uniform, but the highest temperature is slightly higher at *47.94°C* compared to uniform flow showing *46.99°C*, Fig. 15 and 16, and Table 4.

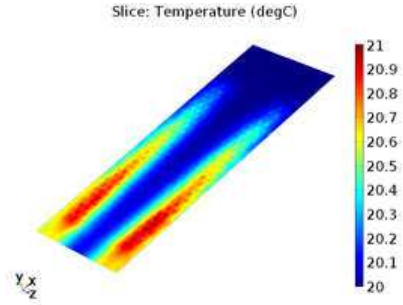

Fig. 15 Conventional design water temperature

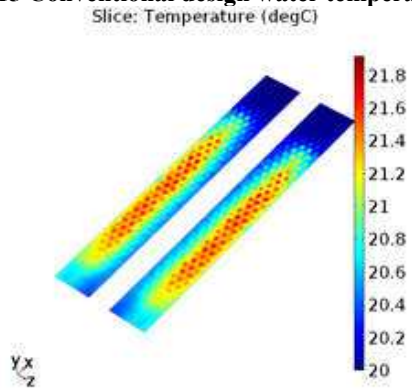

Fig. 16 Proposed design water temperature

Table 4 Max die temperature (JFET 1 is closest to cold plate inlet)

T_{max} (°C):	JFET 1	JFET 2	JFET 3	JFET 4	JFET 5	JFET 6
Design 1	46.15	46.62	46.76	46.99	46.91	47.13
Design 2	46.96	47.84	47.90	47.94	47.79	47.78

VIII. SUMMARY

A new Super Cascode Power Module topology is proposed and simulated to showcase improved switching and balancing performance over state-of-the-art solutions, see Table 5. The PREES SCPM-E3 series was purposely packaged in the E3 format for comparison with Si-IGBT modules. Our module shows slow voltage fall time due to the test diode module *D1* being designed for much higher current, hence the higher capacitance. Otherwise, the design is comparable with Li[5], with lower switching loss, as simulation shows.

Table 5 Si-IGBT module and SCPM rise/fall time comparisons

Design	Si-IGBT	Epelt[1]	Biela[4]	Li[5]	This work
Current t_r/t_f (ns)	~400/500	160/240	161/41	40/60	45/200
Voltage t_r/t_f (ns)	~400/500	60/80	31/182	37/73	45/50
P loss (W/kHz)	698[5]	N/A	N/A	16.3	9.16 (simulated)

Provided are details on the SCPM-E3 fabrication for creation of a *6.0kV/100A* SCPM with *6.5kV* static blocking capability, or with larger die, *8.0kV/200A*. Several SCPM and diode modules were fabricated in the NSCU PREES Lab, and forward/reverse electrical tests were performed to show static and dynamic electrical performance. Switching at *3.0kV/50A*, the SCPM showed t_r*=28ns and* t_f*=100ns* for current in an SCPM-SCPM half-bridge configuration. Switching at *4.0kV/110A*, the SCPM showed t_r*=45ns and* t_f*=50ns* for current in an SBD-SCPM configuration. Results highlight the effectiveness of WBG-based super cascodes capable of medium voltage fast transition switching, and also showcase good thermal performance. Future work increases avalanche energy handling capacity, demonstrates the full power capability of the SCPM using a continuous full-power test platform, and develops a WBG-optimized package for much higher performance at higher power densities.

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