# Stationary Reference Frame Based Current Control Structure With Improved Disturbance Rejection For Grid Connected Converters

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***Abstract*—A proportional resonant ($PR$) controller is commonly used for tracking the reference current with zero steady state error in the stationary reference frame ($abc$ or $\alpha\beta$) for the voltage source converter. Such a structure suffers from poor disturbance rejection capability when the grid voltages contain harmonic components. This results in higher harmonic distortion in the grid currents which is not desirable. This paper introduces a virtual loop based current control structure for improving the voltage and the current disturbance rejection capability. The virtual loop based current control structure also decouples the reference tracking and disturbance rejection leading to simpler controller designs. Frequency domain plots and analysis have been provided to validate the presented control structure. Detailed circuit simulation results have been used to verify the presented analysis.**

***Index Terms*—$abc$ frame current control, $\alpha\beta$ frame current control, resonant controller, grid voltage harmonics, voltage unbalances.**

## I. Introduction

Distributed Generation (DG) systems based on renewable energy resources have become quite popular due to their ability to curb greenhouse gas emissions and reduce dependency on fossil fuels. Such systems are integrated to the grid using power electronic based switching converters. This, combined with the steady increase in non-linear loads, can lead to serious power quality issues such as harmonic distortion of grid voltages. Pulse Width Modulated (PWM) voltage source converters are one of the most popular grid connected converter solutions extensively used in a variety of applications. Current control of such converters is important to regulate the real and reactive power flows while simultaneously achieving a stable and good dynamic performance. The current control can be achieved in the stationary ($abc$ or $\alpha\beta$) [1]–[3] or the synchronous ($dq$) reference frame [4]. With the introduction of proportional resonant ($PR$) controllers, current regulation in the $abc$ or $\alpha\beta$ reference frame has become attractive since the $dq$ frame transformation can be eliminated. Unfortunately, the $PR$ control based structures offer poor disturbance rejection capability when the grid voltages contain lower order harmonics [5]. These harmonics can affect the tracking capability of the $PR$ controllers leading to an increased distortion in the grid current. This may not be acceptable since the current distortion levels may not adhere to the maximum permissible distortion limit as defined in IEEE 519 [6].

A conventional proportional resonant ($PR$) current control structure [3] helps track a sinusoidal reference with zero steady state error in the $abc$ or the $\alpha\beta$ frame as shown in Fig. 1. The disturbance rejection performance of such a controller deteriorates when the grid voltages contain unwanted lower order harmonic components. Ideally, adding a grid voltage feedforward component from a phase locked loop (PLL) should mitigate the effects of voltage harmonics present in the grid. In practice, this approach may not really help as converter dead-time effects and any processor based computational delays might actually lead to an increase in the lower harmonic components of the ac currents.

Improved current control structures in the stationary frame have been discussed in literature with [5] being one of the most widely adopted structure. In this structure, dedicated resonant controllers are used for attenuating each harmonic disturbance component. This can lead to an increase in the design and implementation complexity of the control structure when multiple harmonic components need to be attenuated. Advanced control schemes based on state feedback, optimal control and adaptive control techniques have been explored for current control in voltage source converters [7]–[13]. Most of these techniques are computationally intensive and involve non-trivial design steps. A robust dual loop based control structure that uses two separate controllers in the synchronous $dq$ frame was recently introduced that can decouple the command tracking feature from disturbance rejection [14]. Even though the dual loop control structure looks quite promising, design of the disturbance rejection controller is not straightforward. This paper proposes a virtual loop based current control

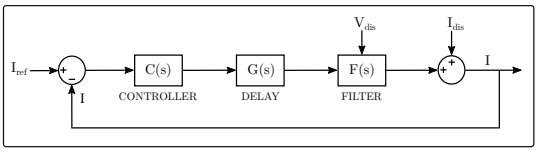


Fig. 1: A proportional resonant ($PR$) based current control structure in the $abc$ or $\alpha\beta$ frame [3].

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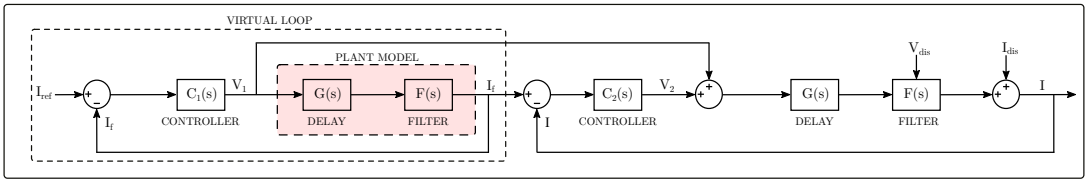


Fig. 2: A virtual loop based current control structure for improved voltage and current disturbance rejection.

structure that also makes use of two controllers for decoupling reference tracking from disturbance rejection. The advantage of the proposed structure is that the controllers can be independently designed in a simple manner. Though this paper analyzes the control structure in the $abc$ frame, the virtual loop based current control structure can also be used in the $dq$ frame.

This paper is organized as follows. Section II discusses the proposed virtual loop based current control structure. Section III details the controller design considerations for accurate reference tracking and improved disturbance rejection. Section IV presents several test cases to show the performance improvements possible with the proposed structure.

## II. Current Control Structure With Improved Disturbance Rejection

A new virtual loop based current control structure centered on a model based reference feed-forward is introduced for the $abc$ or $\alpha\beta$ frame. Such a virtual loop based structure uses 2 controllers, one for tracking the given reference and the other for improving the voltage and current disturbance rejection as shown in Fig. 2. This structure uses an internal plant model ($P_m(s)$) implemented in the virtual loop which mimics the computational delay along with the ac filter for decoupling the reference tracking from the disturbance rejection. $P_{ac}(s)$ refers to the actual plant and is defined as $P_{ac}(s) = G(s)F(s)$. To obtain the reference tracking expression, the following equations can be written as shown below.

$$I_{ref}(s) - I_f(s) = \frac{V_1(s)}{C_1(s)} \tag{1}$$

$$I_f(s) = V_1(s)P_m(s) \tag{2}$$

$$I_f(s) - I(s) = \frac{V_2(s)}{C_2(s)} \tag{3}$$

$$I(s) = (V_1(s) + V_2(s))P_{ac}(s) \tag{4}$$

Performing some mathematical manipulations on equations $(1)-(3)$ and rearranging the terms, we can obtain $V_1(s)$ and $V_2(s)$ as shown in $(5)$ and $(6)$.

$$V_1(s) = \frac{C_1(s)I_{ref}(s)}{1 + C_1(s)P_m(s)} \tag{5}$$

$$V_2(s) = \frac{C_2(s)P_m(s)C_1(s)I_{ref}(s)}{1 + C_1(s)P_m(s)} - C_2(s)I(s) \tag{6}$$

Substituting equations $(5)$ and $(6)$ in $(4)$ leads to the reference tracking expression for the virtual loop based current control structure shown in Fig. 2.

$$\frac{I(s)}{I_{ref}(s)}\Big|_{I_{dis}(s),V_{dis}(s)=0} = \frac{C_1(s)P_{ac}(s)}{1 + C_1(s)P_m(s)}\Big(\frac{1 + C_2(s)P_m(s)}{1 + C_2(s)P_{ac}(s)}\Big) \tag{7}$$

Assuming that the plant model has been accurately modeled ($P_m(s) \simeq P_{ac}(s)$), equation $(7)$ can be reduced as shown in equation $(8)$.

$$\frac{I(s)}{I_{ref}(s)}\Big|_{I_{dis}(s),V_{dis}(s)=0} = \frac{C_1(s)P_{ac}(s)}{1 + C_1(s)P_{ac}(s)} \tag{8}$$

Similarly, the output current to current disturbance attenuation transfer function can be defined using $I_{ref} = 0$, and equations $(1)$ and $(2)$ leading to $(9)$.

$$V_1(s)\Big(\frac{1 + P_m(s)C_1(s)}{C_1(s)}\Big) = 0 \tag{9}$$

Either $V_1(s) = 0$ or $P_m(s) = -\frac{1}{C_1(s)}$ based on the equation $(9)$. Since $C_1(s)$ is assumed not to be an inversion of $P_m(s)$ it can be assumed that $V_1(s) = 0$. The disturbance, $I_{dis}(s)$ and the output $I(s)$ can be related by equation $(10)$.

$$I(s) = (V_2(s)P_{ac}(s)) + I_{dis}(s) \tag{10}$$

Using equations $(1)-(3)$, along with $(10)$ and $V_1(s) = 0$, the output current to current disturbance attenuation transfer function can be defined as:

$$\frac{I(s)}{I_{dis}(s)}\Big|_{I_{ref}(s),V_{dis}(s)=0} = \frac{1}{1 + C_2(s)P_{ac}(s)} \tag{11}$$

The output current to voltage disturbance attenuation transfer function would be defined differently based on the type of ac filter which is used for interfacing the voltage source converter to the grid. Under the assumption that the ac filter is an inductive filter ($L$), the voltage disturbance rejection transfer function is given in $(12)$.

$$\frac{I(s)}{-V_{dis}(s)}\Big|_{I_{ref}(s)=0,I_{dis}(s)=0} = \frac{F(s)}{1 + C_2(s)P_{ac}(s)} \tag{12}$$

Equations $(7)$, $(11)$ and $(12)$ lead to some important observations-

- The reference tracking and disturbance rejection transfer functions are completely independent of each other when internal plant model is implemented accurately($P_m(s) \simeq P_{ac}(s)$).

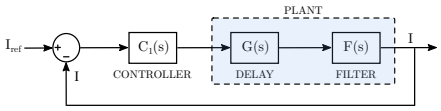


Fig. 3: Reference tracking design loop for the proposed control structure.

- The controller $C_1(s)$ can be designed for reference tracking and can be selected to be a $PR$ in the $abc$ or $\alpha\beta$ frame to track the sinusoidal reference with zero steady state error.
- The voltage and current disturbance/harmonic rejection is purely based controller $C_2(s)$.
- The closed loop bandwidths of both the reference tracking and disturbance rejection can be different.

## III. Controller Design

For the controller design, a voltage source converter interfaced to the grid using a simple $L$ filter was assumed. Table. I gives the circuit parameters for the voltage source converter.

TABLE I: Voltage Source Converter Parameters

| Parameter | Value |
|---|---|
| Grid frequency, $f_g$ | 60 $Hz$ |
| Switching frequency, $f_{sw}$ | 30 $kHz$ |
| AC filter inductance, $L$ | 2 $mH$ |
| AC filter resistance, $R_L$ | 0.2 $\Omega$ |
| DC link capacitance, $C_{dc}$ | 220 $uF$ |
| Reference tracking bandwidth | 600 $Hz$ |

### A. Controller Design for Reference Tracking

As discussed in Section II, controller $C_1(s)$ decides the reference tracking design. Hence, the virtual loop based current control structure shown in Fig. 2 can be reduced to Fig. 3. Let the plant, $P(s) = G(s)F(s)$ and the loop gain, $L_p(s) = C_1(s)P(s)$. A simple $PR$ controller can be used as $C_1(s)$ and designed as mentioned [3]. Since the design is in the $abc$ frame, the $PR$ has been tuned at the grid frequency. A typical $PR$ controller is represented by equation $(13)$ where $w$ refers to the fundamental frequency component that needs to be tracked and $K_r$ defines the gain of the resonant function. The $PR$ controller given by $(13)$ is generally modified as shown in $(14)$ to make it more suitable for digital implementation as mentioned [1] and [3] where the lower breakpoint frequency can be represented by $w_c$.

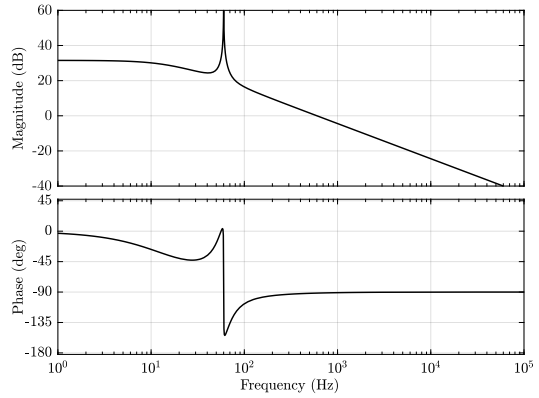


Fig. 4: Loop gain transfer function of the proposed virtual loop based current control structure.

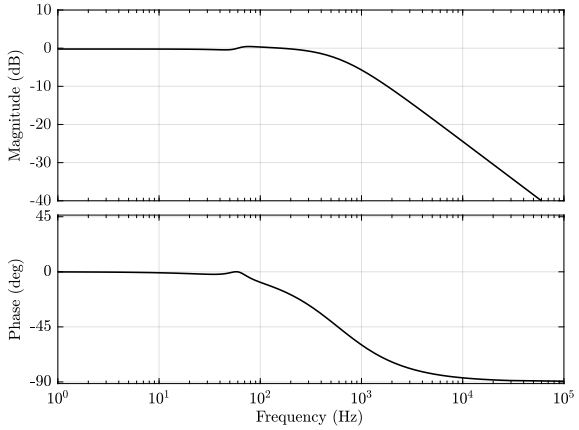


Fig. 5: Reference tracking transfer function of the proposed virtual loop based current control structure.

$$C(s) = K_p + \frac{K_r s}{s^2 + w^2} \tag{13}$$

$$C(s) = K_p + \frac{K_r w_c s}{s^2 + 2w_c s + w^2} \tag{14}$$

The associated loop gain and closed loop reference tracking plots are shown in Fig. 4 and 5.

### B. Controller Design for Voltage and Current Disturbance Rejection

The controller design for mitigating the voltage and current disturbances becomes more flexible since it no longer affects the reference tracking capability. Fig. 6 based on equations $(11)$ and $(12)$ can be used for designing the controller $C_2(s)$. In this paper, 2 different controllers namely, a proportional $(P)$ controller and a proportional integral $(PI)$ controller have been compared. The cut-off frequency for the loop gain, $L_s(s) = G(s) * D(s) * C_2(s)$ can be decided by the attenuation required at the different harmonic frequencies. The bandwidth limitation for the disturbance loop is determined by the Nyquist rate of the system. The sensitivity current disturbance transfer function is shown in Fig. 7. It can be

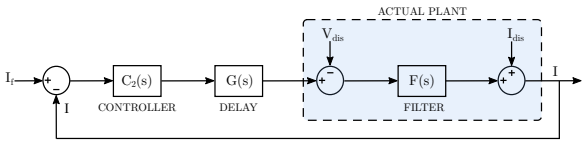


Fig. 6: Voltage and current disturbance rejection design loop for the proposed control structure.

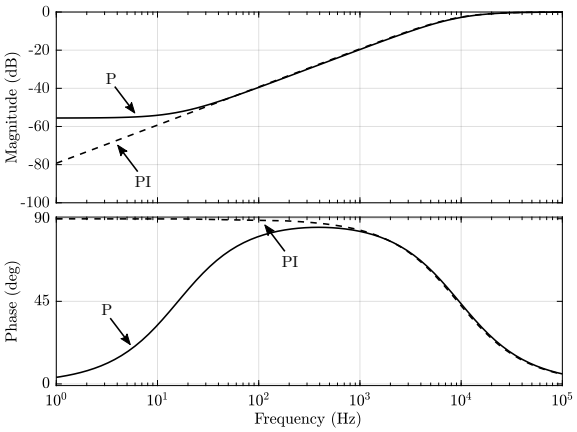


Fig. 7: Current disturbance transfer function of the proposed virtual loop based current control structure.

observed that $PI$ controller offers a very high attenuation at the lower frequencies due the integral action whereas the $P$ controller has a limited attenuation. Fig. 8 describes the attenuation to lower order voltage harmonic components. It is interesting to note that although $PI$ and $P$ have similar attenuation at the lower harmonic frequencies, the $PI$ has very good attenuation at $dc$. Hence, using a $PI$ as the disturbance controller would help reject any $dc$ offsets present in the grid voltages.

The control parameters that are used for plotting the frequency domain plots are listed in Table. II.

TABLE II: Control Parameters

| | Controller | Parameter | Value |
|---|---|---|---|
| Tracking Loop | $C_1(s)$ | $K_p$<br>$K_r$<br>$w_c$ | 7.53<br>1507.96<br>1.00 |
| Disturbance Loop | $PI$ $(C_2(s))$ | $K_p$<br>$K_i$ | 115.61<br>11561.00 |
| | $P(C_2(s))$ | $K_d$ | 120.00 |

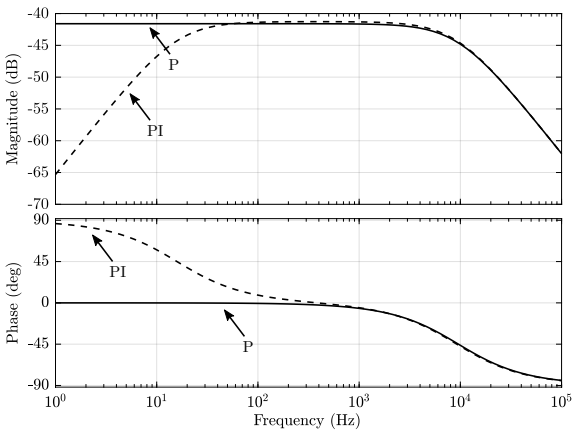


Fig. 8: Voltage disturbance transfer function of the proposed virtual loop based current control structure.

## IV. Results and Discussion

An inverter interfaced to the grid through a $L$ filter is chosen for validating the proposed control strategy using circuit simulations. The system parameters and the controller parameters used for the simulation based study are tabulated in Table I and Table II respectively.

The performance of the virtual loop based control structure is compared with that of the conventional $PR$ structure in $abc$ frame under distorted and unbalanced grid voltage conditions. A circuit simulation was performed where $5^{th}$ harmonic ($V_5$) and $7^{th}$ harmonic ($V_7$) voltage components were added to the grid voltages. The grid current THD is tabulated under different grid voltage distortion conditions as shown in Table III. The virtual loop based control structure is seen to be quite superior as compared to a conventional $PR$ control structure.

TABLE III: Grid Current THD Variation under Distorted Grid Voltage Conditions

| Test Condition | PR based control structure | Virtual loop based control structure |
|---|---|---|
| $V_5 = 5\%, V_7 = 0$ | 4.86% | 1.12% |
| $V_5 = 0, V_7 = 5\%$ | 4.45% | 1.12% |
| $V_5 = 5\%, V_7 = 5\%$ | 6.51% | 1.43% |

The grid current waveforms when the grid voltage is distorted with 5% of $V_5$ and 5% of $V_7$ are shown in Fig. 9. It can be seen that the virtual loop based control structure significantly reduces the THD in grid current. Fig. 10 also corresponds to the same operating condition with a distorted grid voltage where the effect of disabling and enabling the virtual loop controller dynamically is illustrated. As expected from Fig. 9, the current harmonics are significantly reduced when the virtual loop based controller is enabled.

Another simulation was performed wherein a 50% sag was suddenly introduced in $a$ and $b$ phases of the grid voltages. The simulation results with $PR$ controller and the virtual

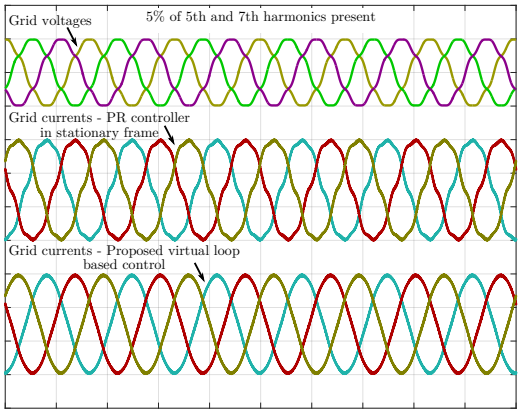


Fig. 9: Grid voltages (line-neutral) with 5% of $5^{th}$ and $7^{th}$ harmonics each [100V/div] and grid currents [10A/div] versus time [10ms/div].

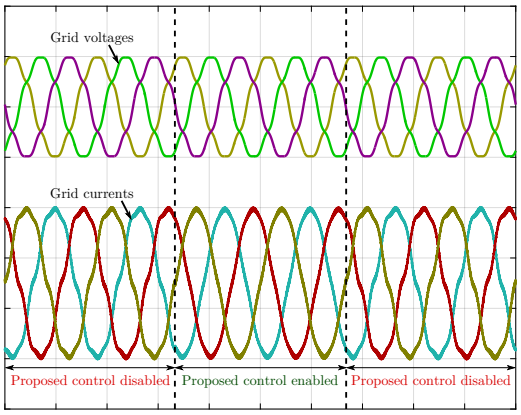


Fig. 10: Grid voltages (line-neutral) with 5% of $5^{th}$ and $7^{th}$ harmonics each [100V/div] and grid currents [10A/div] versus time [10ms/div].

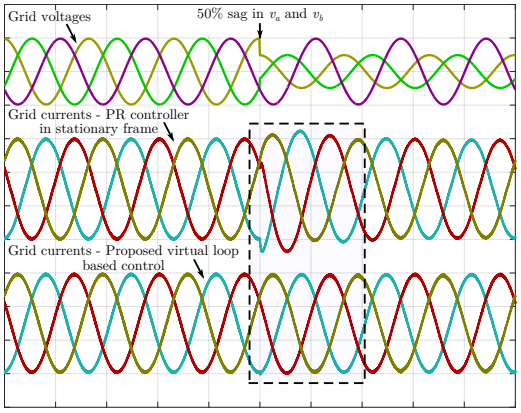


Fig. 11: Grid voltages (line-neutral) [100V/div] and grid currents [10A/div] versus time [10ms/div] during a 50% sag in both $a$ and $b$ phases.

loop based controller are given in Fig. 11. The highlighted portion in Fig. 11 shows the transients in grid currents when a voltage sag is introduced. With a conventional $PR$ controller, there is an instantaneous overshoot in grid current and the transients die down slowly whereas with the virtual loop based controller, the currents are immune to even such a severe grid unbalance condition. This can be attributed to the superior voltage and current sensitivity functions of the virtual loop based controller. In a practical system, such an overshoot is enough to instantaneously trip the converter when it is operating close to its rated power conditions. The proposed virtual loop controller can be advantageous when a low voltage ride through (LVRT) feature is desired in critical applications such as DG systems to prevent sudden loss of generation leading to a cascaded failure.

## V. Conclusion

A virtual loop based current control structure has been introduced to mitigate the lower order grid voltage harmonics and unbalances. This control structure decouples the reference tracking feature from the disturbance rejection capability by making use of an internal plant model. Two controllers are used for independently controlling the reference tracking and rejecting disturbances respectively. The controller design considerations have been presented. The effect of using different controller designs for mitigating disturbances have also been discussed in this paper. Frequency domain plots have been presented and analyzed to show the superior sensitivity feature of the proposed virtual loop based controller. The proposed virtual loop based current control structure has been validated with detailed circuit simulations.

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