

# Scale-up Methodology of a Modular Multilevel Converter for HVDC Applications

Mohammed Alharbi  
North Carolina State University  
Raleigh, NC 27695, USA  
mmalharb@ncsu.edu

Subhashish Bhattacharya  
North Carolina State University  
Raleigh, NC 27695, USA  
sbhatta4@ncsu.edu

**Abstract**— Modular Multilevel Converters is developing a realistic alternative to the conventional converters for Medium Voltage (MV) and High Voltage Direct Current (HVDC) applications. The MMC topologies utilize a high number of submodule (SM) cascaded in series per phase arm to achieve the desired high voltage level. These SMs can be as high as 512 SMs to produce a very low Total Harmonics Distortion (THD) (e.g. < 0.1%) of the MMC AC side interface voltage. However, employing a large number of SMs in the converter to synthesize a very low THD of an AC voltage with a high number of levels increases the control complexity. Typically, the MMC AC side interface voltage THD requirements are < 3% which can be achieved by 48-pulse stepped AC waveform. This paper presents the first step towards MMC scale-up control and performance analysis such that the behavior of a high number of SMs can be predicted by a cumulative set of a smaller number of SMs. A Back-to-Back (B2B) MMC based on the scale-up method is implemented in a Real Time Digital Simulator (RTDS) and MMC support units based FPGAs. The results demonstrate that the scale-up control method is providing a satisfactory performance and other features for HVDC systems such as a stable operation under multiple faulty SMs.

**Keywords**—Modular Multilevel Converter; MMC; Back-to-Back HVDC; Real Time Digital Simulator; RTDS

## I. INTRODUCTION

HVDC systems utilizing line-commutated converters based on thyristors have been extensively investigated and used for high power transmissions. However, the voltage source converters (VSC) use entirely controlled semiconductor devices which provide flexibility to control the active and reactive power independently and bi-directionally [1] and [2]. Besides, the VSC topologies allow many features compared to the thyristors-based converters such as power quality improvement, a connection of weak AC systems, renewable energy integrations and multi-terminal DC (MTDC) systems [2]-[4]. Typically, the switching frequency is desirable to be much higher than the line frequency in the conventional two-level and three-level converters [5]. However, the high switching frequency motivates higher power losses; thus, the switching losses limit the switching frequency [6].

Modular Multilevel Converter (MMC) based HVDC is an attractive topology for high voltage applications. As the number of stepped voltage waveforms increases, the synthesized output voltage of the MMC is practically a sinusoidal waveform with an excellent harmonic performance [7]-[11]. Further, MMC

systems have high efficiencies because the switching frequency can be as low as the line-frequency [12] and [13]. Therefore, the MMC topologies are efficient and suitable for high power transmissions, and as an alternative to the conventional converters in many applications.

The MMC topologies employ a large number of SMs per phase arm with floating capacitors. These floating capacitors have a substantial impact on the output waveforms. Therefore, the balancing of the floating capacitor voltages is essential to ensure safe and stable operations. The floating capacitor voltages are directly affected by the selection of modulation techniques [14]. Nearest Level Modulation (NLM) and Selective Harmonic Elimination (SHE) modulation, which is a staircase modulation for MMC systems, allow very low switching frequency (e.g. line frequency). However, the balancing of capacitor voltages with the low switching frequency is quite difficult [13]. The sorting algorithms are sufficient with these modulation techniques to balance the floating capacitor voltages. With the sorting methods, the floating capacitors with the lowest or highest voltages are inserted into the system according to the direction of the arm current [15]. Many different sorting methods are implemented to balance the capacitor voltages in [15]-[21].

In MMC based HVDC systems, a very low THD (< 0.1%) can be achieved using a high number of SMs per arm (e.g. 512 SMs). Typically, a high number of MMC SMs produces an AC side interface voltage with a high number of levels (e.g.  $2N+1$  or  $N+1$  where  $N$  is the number of SMs per phase-arm). However, constructing an MMC AC voltage with a high number of levels increases the control complexity [22] and need a high-speed communications network to provide a high controller bandwidth [23]. Typically, a voltage waveform THD of less than 3% is good enough to synthesize the output voltage waveform of MMCs which can be achieved by 48-pulse staircases waveform. With the scale-up methodology, a set of SMs behaves as an individual SM to generate the desired output voltage waveform with less number of levels. This methodology exploits the MMC modularity to provide more capabilities and possibilities of other controls such as operating under several faulty SMs. Further, the desired AC and DC voltage can be accomplished with less number of voltage level without increasing the voltage stress on switches and SM capacitors. This paper addresses the first step toward the scale-up control of MMC and performance analysis using the Real Time Digital Simulator (RTDS) and MMC support units based FPGAs.

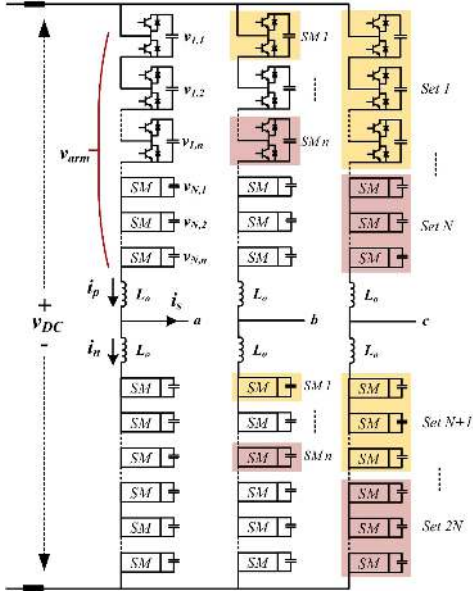


Fig. 1. Three-phase scale-up MMC based HVDC configuration

## II. OPERATING PRINCIPLES OF SCALE-UP METHODOLOGY AND SPECIFICATIONS

### A. Operating Principles

Fig. 1 represents a three-phase scaled-up MMC based HVDC system. The scale-up MMC system consists of six arms where each arm comprises  $N$  sets “groups” cascaded in series and an inductor  $L_o$ . Each set has  $n$  half-bridge SMs cascaded in series. Each SM utilizes two IGBT switches with an antiparallel diode and a floating DC capacitor. Each  $n$  SMs behaves as an individual SM to generate the AC stepped waveform as illustrated in Fig. 2. Although the total number of SMs per phase arm is  $N \times n$ , the arm operates as it has  $N$  SMs which means that the MMC produces an AC voltage with less number of levels. However, the THD of the AC side interface voltage is always maintained to be less than 3% which can be accomplished by a 48-pulse stepped waveform in a cycle.

The operating principle is identical among the three phases, thus; a single phase (e.g. phase-a) of MMC is only considered as an example to elaborate the MMC scale-up approach. The DC bus voltage of the MMC can be defined as follows:

$$v_{DC} = \sum_{i=1}^{2N} \sum_{j=1}^n S_{i,j} v_{i,j} + L_o \frac{d}{dt} (i_p + i_n) \quad S = 0,1 \quad (1)$$

where  $v_{i,j}$  is the SM capacitor voltage  $j$  of set  $i$ ,  $L_o$  is the arm inductor, and  $i_p$  and  $i_n$  are the upper and lower arm currents of a single phase, respectively.  $S$  represents the operation state of SM whether the capacitor voltage is inserted to the system or not. The upper and lower arms of the MMC phase can be defined as follows:

$$v_{arm,u} = \frac{v_{DC}}{2} - v_{ac} - L_o \frac{di_p}{dt} \quad (2.a)$$

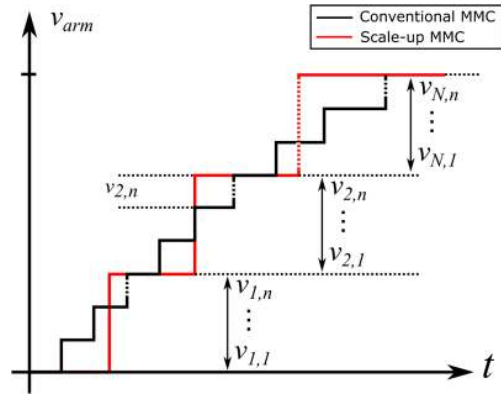


Fig. 2. Output voltage waveform of a single MMC arm based HVDC

$$v_{arm,l} = \frac{v_{DC}}{2} + v_{ac} - L_o \frac{di_n}{dt} \quad (2.b)$$

where  $v_{ac}$  is the single-phase AC output voltage of the MMC, and  $v_{arm,u}$  and  $v_{arm,l}$  are the upper and lower arm voltages.

The output voltage of the MMC  $v_{ac}$  is defined as follows:

$$v_{ac} = \frac{v_{arm,l} - v_{arm,u}}{2} \quad (3)$$

In general, the reference AC output voltage  $v_{ac}$  of a single phase (e.g. phase-a) can be also written as (4). Note that the  $120^\circ$  phase shift should be considered for the other phases (e.g. phase-b and c):

$$v_{ac} = m \frac{v_{DC}}{2} \sin(\omega t) \quad 0 \leq m \leq 1 \quad (4)$$

where  $m$  is the modulation index and characterized as the peak AC-side output voltage of the MMC  $\hat{v}_{ac}$  divided by half of the DC voltage as:

$$m = \frac{2\hat{v}_{ac}}{v_{DC}} \quad (5)$$

Substituting (4) into (2) and ignoring the voltage across the arm inductors  $L_o$ , the upper and lower arm voltages can be expressed as [24]:

$$v_{arm,u} = \frac{v_{DC}}{2} [1 - m \sin(\omega t)] \quad (6.a)$$

$$v_{arm,l} = \frac{v_{DC}}{2} [1 + m \sin(\omega t)] \quad (6.b)$$

The number of implemented sets within the upper arm  $N_{arm,u}$  and lower arm  $N_{arm,l}$  at specific time  $t$  is defined as [25]:

$$N_{arm,u} = \frac{v_{DC}[1 - m \sin(\omega t)]}{2n v_{i,j}} \quad (7.a)$$

$$N_{arm,l} = \frac{v_{DC}[1 + m \sin(\omega t)]}{2n v_{i,j}} \quad (7.b)$$

The values of  $N_{arm,u}$  and  $N_{arm,l}$  are always rounded to the nearest integer number. The maximum number of implemented sets  $N_{max}$  within each arm can be realized as:

$$N_{max} = \frac{v_{DC}[1 + m]}{2n v_{i,j}} \quad (8)$$

The number of output voltage levels produces by the MMC principally depends on the implemented modulation technique to generate the firing pulses (FPs) to the MMC switches. The number of output voltage levels of using the conventional Nearest Level Modulation (NLM) technique is  $(N + 1)$  while the phase-shifted PWM technique generates  $(2N + 1)$ . The maximum number of active sets  $N_{ac,max}$  to the output voltage of MMC can be found as follows:

$$N_{ac,max} = m \frac{v_{DC}}{n v_{i,j}} \quad (9)$$

Each SM capacitor voltage  $j$  of set  $i$  is obtained as follows:

$$v_{i,j} = \frac{v_{DC}}{N \times n} \quad (10)$$

Each set produces an output DC voltage of  $n \times v_{i,j}$ . Thus, the average voltage of each set  $\bar{v}_i$  and phase-leg  $\bar{v}$  are expressed as:

$$\bar{v}_i = \frac{\sum_{j=1}^n v_{i,j}}{n} \quad i = 1, 2, \dots, 2N \quad (11)$$

$$\bar{v} = \frac{\sum_{i=1}^{2N} \bar{v}_i}{2N} \quad (12)$$

### B. Operation with Multiple SM Faults

One of the distinctive features of using scale-up MMC is the operating under several faulty SMs. In the conventional MMC schematic, the converter depends on each SM in the MMC to synthesize the output AC-side voltage and DC bus voltage. Malfunction of any SM results in undesirable waveform and a high THD, or it may lead to unstable operation of the entire MMC. In contrast to the conventional MMC system, the scale-up MMC can satisfactorily operate under multiple faulty SMs. This feature significantly increases the reliability of the MMC operation.

To ensure a stable operation with faulty SMs, each set of the MMC should maintain a constant output voltage of  $n \times v_{i,j}$ . The SM capacitor voltages of any faulty set will increase to regulate the output voltage of the faulty set without disturbing the other set SMs. The new capacitor voltage values of the faulty set  $v_{i,j}^{new}$  can be selected as follows:

$$v_{i,j}^{new} = v_{i,j} + \frac{n_i v_{i,j}}{n - n_i} \quad (13)$$

where  $n_i$  is the number of faulty SMs at set  $i$ .

From (13), the capacitor voltages of the remaining SMs of any faulty set will increase by  $\frac{n_i}{n - n_i}$  % of the nominal capacitor value. Therefore, each SM capacitor voltage under multiple SM faults should be considered when designing the SM components such as the capacitor and semiconductor device ratings.

## III. CONTROL AND MODULATION OF THE SCALE-UP MMC

Typically, MMC control systems are classified into two levels; the primary control and the arms control. The primary control is mainly used to adjust the power and voltage and provides the reference voltage command of each MMC phase. The primary control is also divided into two parts; the inner current control (ICC) and outer control. The decoupled current

control based  $dq$ -reference frame is developing the inner current control in this paper. The outer control is mainly used to provide the current reference commands of the inner current control. However, the arm control implementations, which include the circulating currents and the SM capacitor voltage balancing controls, mainly depend on the modulation technique such as NLM and phase-shifted carrier PWM.

### A. Phase-shifted PWM Based Control

The phase-shifted PWM is one the techniques that have been used to generate the gate signals for switching devices based on using a single reference sinusoidal waveform. This technique requires  $2N \times n$  identical triangular carriers per MMC phase in the conventional MMC with a phase difference between carriers of  $\theta = \frac{360^\circ}{2N \times n}$ . Thus, the phase-shifted PWM technique is difficult and complicated to implement with a high number of SMs because the carriers are quite high and the phase difference between carriers is considerably small. However, the carriers are reduced to  $2N$  identical triangular waveforms, and the phase difference between carrier waveforms increases to  $\theta = \frac{360^\circ}{2N}$  with the scale-up method.

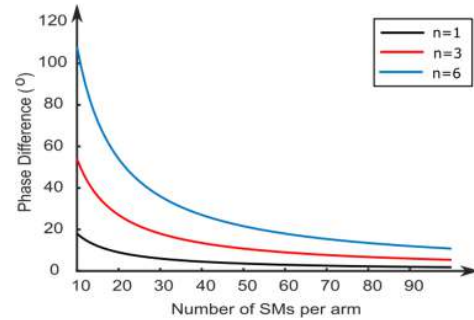


Fig. 5. Carrier waveform phase differences with the conventional ( $n=1$ ) and scale-up ( $n>1$ ) MMC schematic

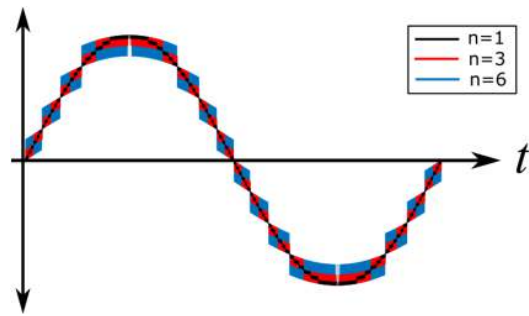


Fig. 6. Typical output voltage with the conventional ( $n=1$ ) and scale-up ( $n>1$ ) MMC schematic

As shown in Fig. 5, the carrier phase difference between the carrier waveforms with the scale-up MMC (e.g.  $n=6$ ) is larger than the conventional MMC where  $n=1$  with the same total number of SMs per arm. Hence, the phase difference between PWMs with scale-up methodology can be much easier to implement especially for a high number of SMs. Note that the THD of the output voltage increases as the number of SM per set  $n$  increases with the same total number of SMs per arm as shown in Fig. 6. Therefore, the output voltage of the MMC

should produce an AC waveform with 48-pulse or more to ensure that the THD is less than 3%.

The arm controls based phase-shifted PWM technique in [26], which include the averaging, arm-balancing, and SM balancing controls, are implemented in this paper.

### B. NLM and Balancing Algorithm Technique

The Nearest Level Modulation (NLM) is a very suitable technique if the number of SMs is quite high because the carrier signals are not necessary. The arm controls, which includes capacitor voltages balancing, circulating current suppression control (CCSC) in [15] and NLM, is used to generate the firing pulses (FPs) for each switching device. Fig. 7 represents the overall block diagram of the MMC control system.

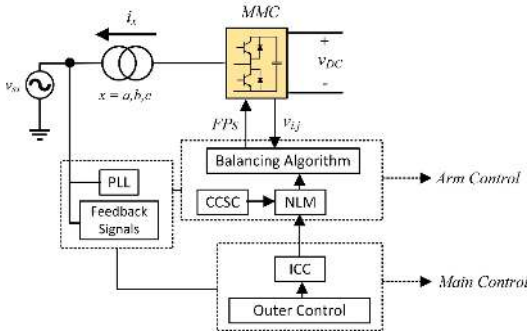


Fig. 7. MMC control system based NLM

The sorting method is widely implemented as a capacitor voltage balancing strategy of MMCs. The fundamental principle of the scale-up MMC approach is mainly developed based on the conventional sorting algorithm as shown in Fig. 8. With the scale-up methodology, a set of SMs behaves as an individual SM. The capacitor voltages are grouped into sets with an equal (or could be unequal) number of SMs per set. When the arm current is positive which charges the capacitors, the sets with the lowest average voltages are inserted into the system. When the arm current is negative which discharges the capacitors, the sets with the highest average voltages are inserted. The required number of inserted sets in the upper and lower arms are derived from (7). This balancing algorithm is implemented for each MMC phase arm.

## IV. SIMULATION RESULTS

### A. Study System

The MMC system shown in Fig. 9 is simulated in the PSCAD software based on the phase-shifted PWM technique to validate the scale-up control methodology under multiple faulty SMs. Table I presents the converter parameters of Fig. 9. The MMC is controlling the active and reactive power at 1 PU and 0 PU, respectively. Although the number of SMs is 24 SMs per arm, the system behaves as it has 6 SMs per arm because the number of SMs in each set is selected to be 4 SMs per set. Thus, the required number of carrier waveforms is 6 carriers in this case. Each SM has a capacitor voltage of  $\frac{48kV}{6 \times 4} = 2kV$ , and each set is required to produce 8kV.

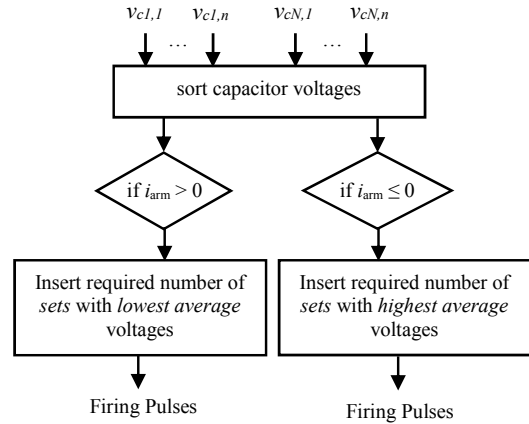


Fig. 8. Capacitor voltage balancing strategy of a single MMC arm

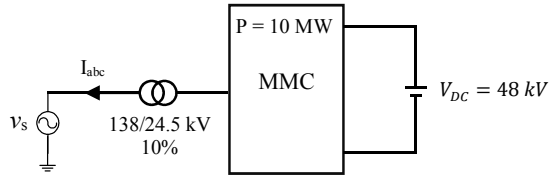


Fig. 9. Single line diagram of the simulated MMC

TABLE I  
MMC SYSTEM PARAMETERS OF FIG. 9

Base MVA ( $P$ )	10 MVA
DC voltage ( $V_{DC}$ )	48 kV
Number of SM per arm ( $N \times n$ )	$6 \times 4 = 24$
Fundamental frequency	60 Hz
Arm inductance ( $L_o$ )	15 mH
Switching frequency	2 kHz

### B. Dynamic Performance of MMC under Multiple SM Faults

Initially, the MMC system operates under the normal condition until  $t=0.5$  s. At  $t=0.5$  s, two SMs (e.g. SM 1 and SM 2) of one set (e.g. set 1) are intentionally failed and removed from the upper arm of phase-a. Consequently, the THDs of the phase-a MMC output voltage and current are increased from 2.87% to 3.16% and 0.09% to 0.69%, respectively. The SM capacitor voltages of the lower arm remain at the nominal value while the SM capacitor voltages of the upper arm are somewhat increased to maintain the average voltage of phase-a SMs to 2 kV. Fig. 10 illustrates the transition of the MMC system from the normal operating condition to the two faulty SM conditions.

The THDs of the output voltage and current can be reduced to the normal operating condition values if the faulty SM voltages are compensated by the other SMs of the same faulty set. In this case, the two remaining SMs of the faulty set (e.g. SM 3 and SM 4) compensate the two faulty SM voltages. Therefore, each SM voltage of the faulty set is increased to a new value based on (13). As seen in Fig. 11, the remaining SM capacitor voltages of the faulty set are increased to a new value at  $t=0.7$  s. Thus, the SM capacitor voltages of the non-faulty sets of either the upper or lower arm are not disturbed by the faulty SMs and maintained at the nominal value, 2 kV.

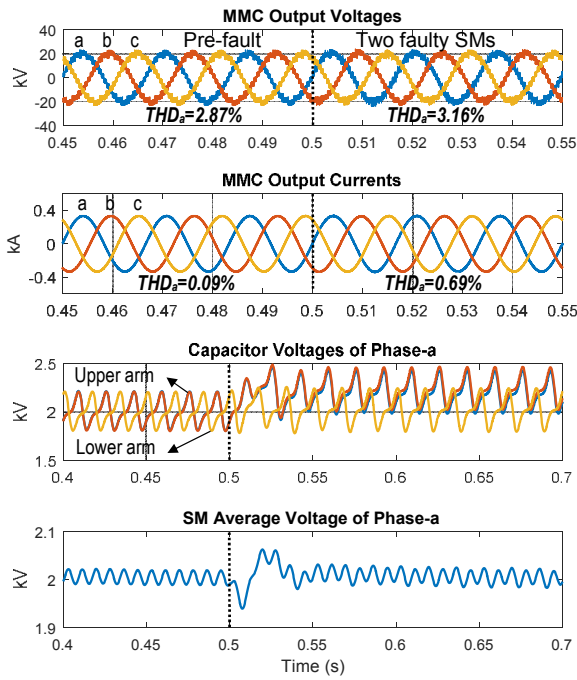


Fig. 10. Dynamic response of the MMC under two faulty SMs

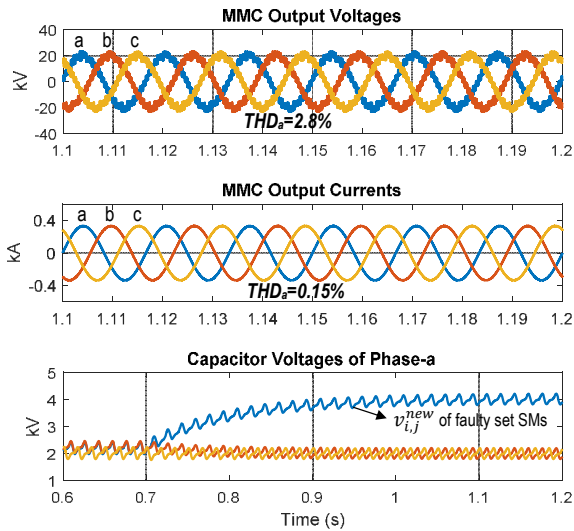


Fig. 11. Performance of the MMC under two faulty SMs with SM voltage compensation

## V. RTDS RESULTS

### A. Study System

The B2B-MMC based HVDC system shown in Fig. 14 is implemented in the RTDS and the MMC Support Units based FPGAs. Table II illustrates the parameters of the B2B-MMC system shown in Fig. 14. The MMC-1 is controlling the active and reactive powers with a power rating of 1000 MVA while the MMC-2 is regulating the DC voltage and reactive power with ratings of 640 kV and 1000 MVA. Each MMC utilizes 128 SMs per arm with an SM DC voltage rating of 5 kV. Each set

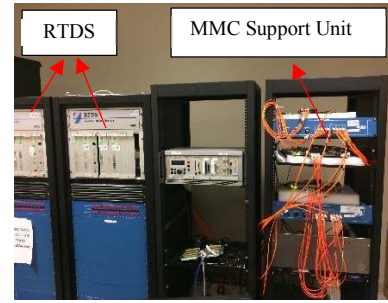


Fig. 12. RTDS and MMC support unit implementations

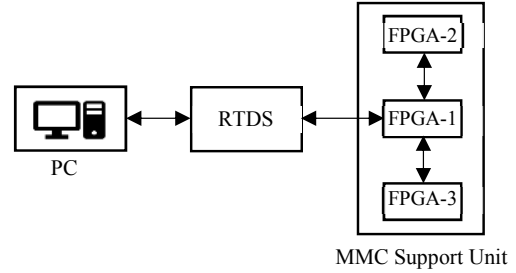


Fig. 13. Overall RTDS and MMC support unit implementation for a single converter

TABLE II  
B2B-MMC BASED HVDC SYSTEM PARAMETERS

Symbol	Description	Value	Unit
$P$	Base MVA	1000	MVA
$V_{DC}$	DC voltage	640	kV
$v_{abc}$	Line-Line AC voltage	400	kV
$T$	Transformer ( $Y_g - \Delta$ )	400/333	kV
$N \times n$	Number of SM per arm	$16 \times 8 = 128$	-
$V_c$	Capacitor Voltage	5	kV
$f$	Fundamental frequency	60	Hz
$L_o$	Arm inductance	15%	PU
$L$	Transformer inductance	18%	PU
$C$	SM capacitance	5	mF

utilizes 8 SMs which behave as a single SM. Therefore, the number of sets per phase-arm  $N$  is 16 sets. The DC bus capacitor size is selected as  $300 \mu\text{F}$ . The high voltage side of the converter transformers is a  $Y$ -connected with a neutral point grounded. The low voltage side of the converter transformer is a  $\Delta$ -connected to eliminate the zero-sequence components under unbalanced grid conditions.

### B. RTDS and MMC Support Unit Implementation

The MMC control system is implemented in RTDS FPGA based MMC supports units for a switching model of MMC based HVDC systems. The RTDS and MMC support units are shown in Fig. 12. The MMC support unit contains a Xilinx Virtex 7 FPGA board (VC707) and two 8 fiber communication daughter boards from Faster Technologies (FM-S18). The

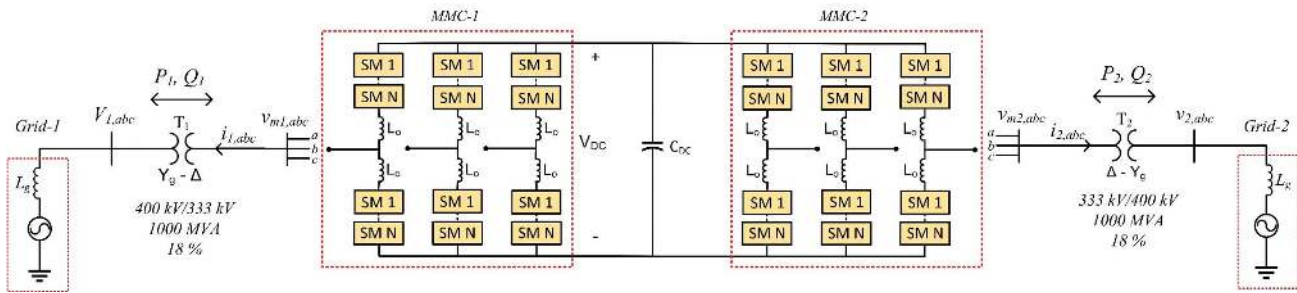


Fig. 14. B2B-MMC System based HVDC

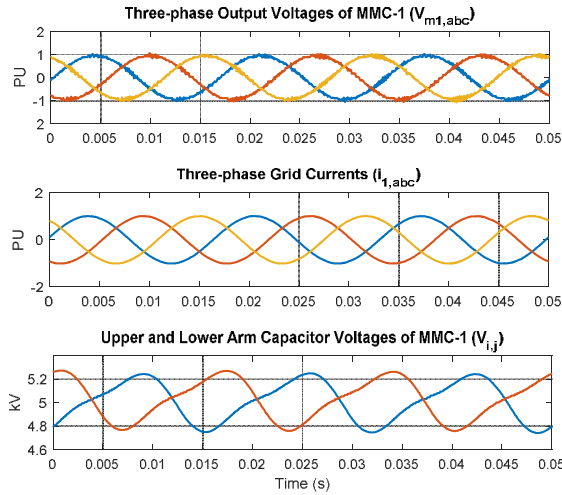


Fig. 15. RTDS results of the MMC-1 under steady states

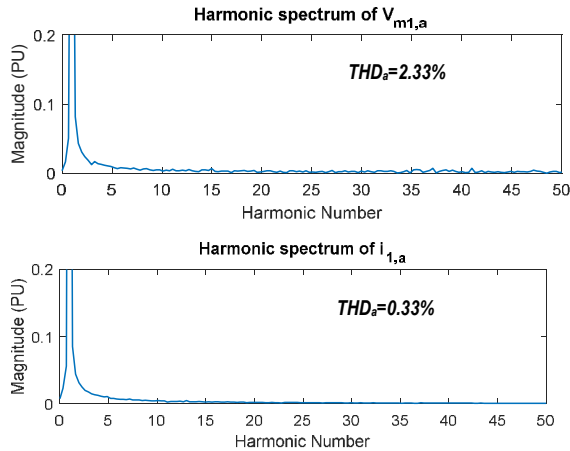


Fig. 16. Voltage and current harmonic spectrums of phase-a MMC-1

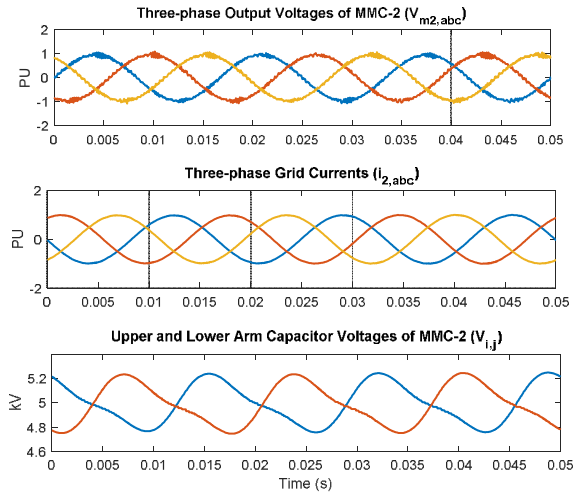


Fig. 17. RTDS results of the MMC-2 under steady states

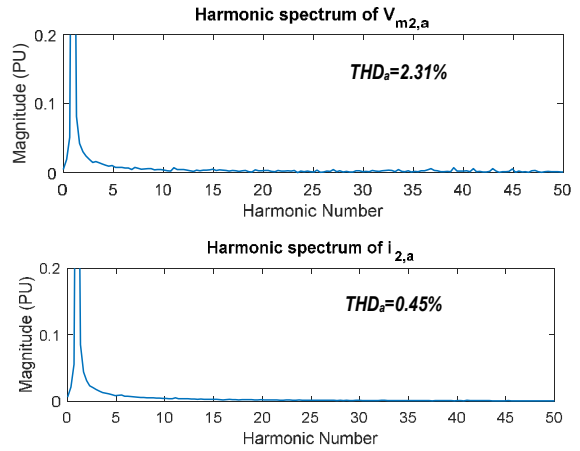


Fig. 18. Voltage and current harmonic spectrums of phase-a MMC-2

VC707 FPGA board provides the ability to support up to six MMC phase arms. With VC707 FPGA boards, three FPGAs are necessary to model a single converter terminal. As illustrated in Fig. 13, FPGA-1 models the six MMC phase arms. FPGA-2 and FPGA-3 are used to model the firing controller for the top and bottom arms of A, B and C phases. The capacitor voltages are sent from FPGA-1 to FPGA-2 and FPGA-3 over fiber connections while the firing pulses (FPs) are sent from FPGA-2 and FPGA-3 to FPGA-1. Six FPGA boards are required to configure the B2B-MMC system.

### C. Performance Evaluation of the Scale-up MMC Under Steady States

The MMC-1 system controls the active and reactive power at 1000 MW and -150 MVAR, respectively. The MMC-2 system is regulating the DC voltage and the reactive power at 640 kV and 150 MVAR, respectively. The active power transfers from Grid-2 to Grid-1. Fig. 15 and Fig. 16 show the RTDS results and the spectral analysis of the output line voltages and grid currents of the MMC-1. The output voltages of MMC-1  $v_{m1,abc}$  have a THD of less than 3% which is

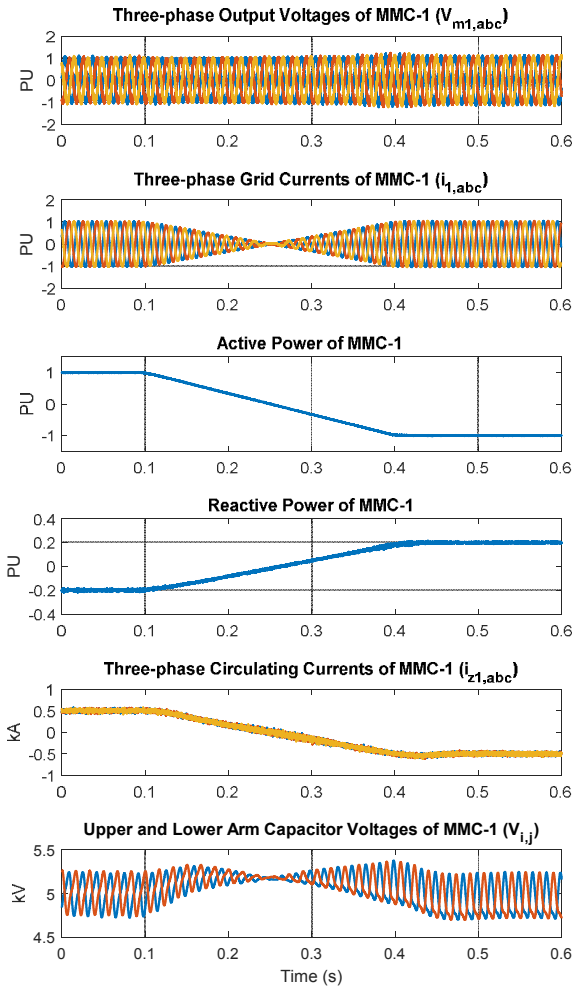


Fig. 19. RTDS results of MMC-1 with active and reactive power variations

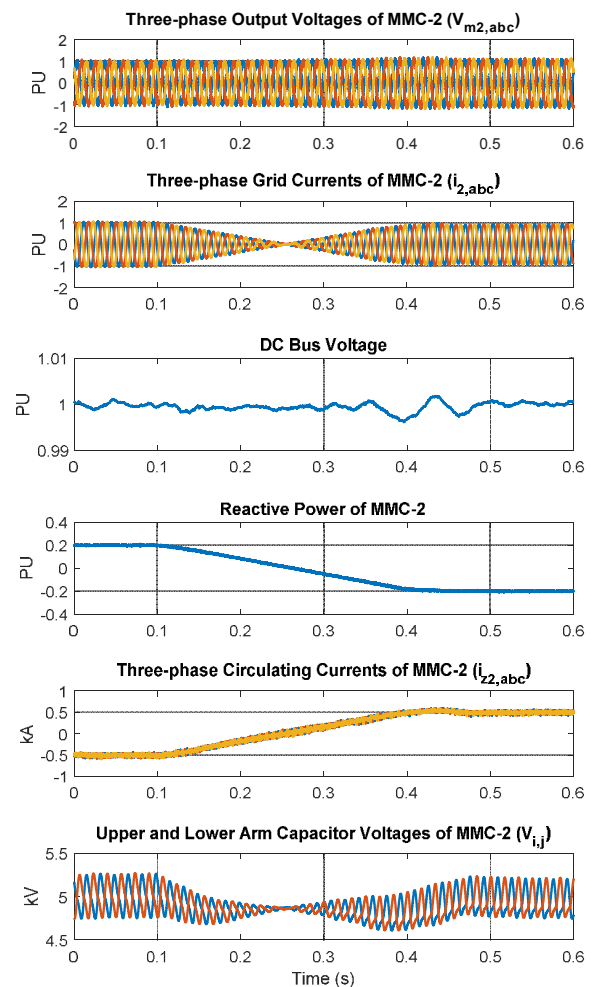


Fig. 20. RTDS results of MMC-2 with active and reactive power variations

satisfactory. The three-phase grid currents  $i_{1,abc}$  look purely sinusoidal due to the low THD ( $<0.4\%$ ). The SM capacitor voltages are controlled at the nominal value of 5 kV with a ripple voltage less than  $\pm 2.8\%$ .

Fig. 17 and Fig. 18 show the RTDS results and the harmonic spectrums of the output line voltages and AC line currents of the MMC-2. The output voltages of MMC-2  $v_{m2,abc}$  have a THD of less than 3%, and the three-phase grid currents  $i_{2,abc}$  are purely sinusoidal because the THD is relatively low ( $<0.5\%$ ). The SM capacitor voltages are maintained at the nominal value with a ripple voltage of  $\pm 2.8\%$ .

#### D. Performance Evaluation of the Scale-up MMC Under Transient States

The B2B scale-up MMC based HVDC system is verified with active and reactive power variations. The MMC-2 system is regulating the DC voltage and the reactive power at 640 kV and 200 MVAR, respectively. The MMC-1 system initially controls the active and reactive power at 1000 MW and -200 MVAR, respectively.

Fig. 19 and 20 show the dynamic responses of MMC-1 and MMC-2 with the active and reactive power variations, respectively. At  $t=0.1$  s, the active power of MMC-1 is ramped to -1000 MW and the reactive power of MMC-1 and MMC-2 are ramped to 200 MVAR and -200 MVAR, respectively. Obviously, the active and reactive power of MMC-1 and MMC-2 are precisely able to track their reference commands. Further, the three-phase circulating currents of MMC-1  $i_{z1,abc}$  and MMC-2  $i_{z2,abc}$  are significantly suppressed due to the implemented CCSC. The DC bus voltage  $v_{DC}$  is regulated at its rated value of 640 kV. The capacitor voltages of the upper and lower arms of MMC-1 and MMC-2 are maintained at the nominal value with a ripple voltage of  $\pm 5.1\%$ .

#### I. CONCLUSIONS

This paper addresses the first step towards scale-up control and performance analysis such that the behavior of a large number of SMs can be predicted by a cumulative set of a smaller number of SMs. The scale-up MMC method is more efficient for MV and HVDC where a large number of SMs is

required. Although the scale-up MMC system has a THD higher than the conventional MMC, the THD of the scale-up MMC system of less than 3% is good enough to synthesize the output voltages of the MMC. Further, this methodology adds more features to the MMC system such as operating under multiple SM faults and easier PWM implementation for a high number of SMs. The scale-up model of MMC system has been presented and analyzed for a B2B MMC-HVDC system in the RTDS and MMC support unit based FPGAs.

#### REFERENCES

- [1] N. Flourentzou, V. G. Agelidis and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," in *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 592-602, March 2009.
- [2] Lie Xu, B. R. Andersen and P. Cartwright, "VSC transmission operating under unbalanced AC conditions - analysis and control design," in *IEEE Transactions on Power Delivery*, vol. 20, no. 1, pp. 427-434, Jan. 2005.
- [3] L. Zhang, L. Harnefors and H. P. Nee, "Power-Synchronization Control of Grid-Connected Voltage-Source Converters," in *IEEE Transactions on Power Systems*, vol. 25, no. 2, pp. 809-820, May 2010.
- [4] S. Cole, J. Beerten and R. Belmans, "Generalized Dynamic VSC MTDC Model for Power System Stability Studies," in *IEEE Transactions on Power Systems*, vol. 25, no. 3, pp. 1655-1662, Aug. 2010.
- [5] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey," in *IEEE Transactions on Industrial Electronics*, vol. 45, no. 5, pp. 691-703, Oct 1998.
- [6] T. Bruckner, S. Bernet and H. Guldner, "The active NPC converter and its loss-balancing control," in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 855-868, June 2005.
- [7] A. Nami, J. Liang, F. Dijkhuizen and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18-36, Jan. 2015.
- [8] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, Aug 2002.
- [9] Jih-Sheng Lai and Fang Zheng Peng, "Multilevel converters-a new breed of power converters," in *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509-517, May/June 1996.
- [10] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist and H. P. Nee, "Dynamic Analysis of Modular Multilevel Converters," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2526-2537, July 2013.
- [11] R. C. Portillo et al., "Modeling Strategy for Back-to-Back Three-Level Converters Applied to High-Power Wind Turbines," in *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1483-1491, Oct. 2006.
- [12] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie and Zhong Du, "Control of a multilevel converter using resultant theory," in *IEEE Transactions on Control Systems Technology*, vol. 11, no. 3, pp. 345-354, May 2003.
- [13] H. Peng, R. Xie, K. Wang, Y. Deng, X. He and R. Zhao, "A Capacitor Voltage Balancing Method With Fundamental Sorting Frequency for Modular Multilevel Converters Under Staircase Modulation," in *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7809-7822, Nov. 2016.
- [14] J. Mei et al., "Balancing Control Schemes for Modular Multilevel Converters Using Virtual Loop Mapping With Fault Tolerance Capabilities," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 38-48, Jan. 2016.
- [15] Q. Tu, Z. Xu and L. Xu, "Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters," in *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 2009-2017, July 2011.
- [16] F. Deng and Z. Chen, "A Control Method for Voltage Balancing in Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 66-76, Jan. 2014.
- [17] W. Li, L. A. Grégoire and J. Bélanger, "A Modular Multilevel Converter Pulse Generation and Capacitor Voltage Balance Method Optimized for FPGA Implementation," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2859-2867, May 2015.
- [18] P. M. Meshram and V. B. Borghate, "A Simplified Nearest Level Control (NLC) Voltage Balancing Method for Modular Multilevel Converter (MMC)," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 450-462, Jan. 2015.
- [19] Z. Li et al., "Power Module Capacitor Voltage Balancing Method for a  $\pm 350$ -kV/1000-MW Modular Multilevel Converter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 3977-3984, June 2016.
- [20] J. Qin and M. Saedifard, "Reduced Switching-Frequency Voltage-Balancing Strategies for Modular Multilevel HVDC Converters," in *IEEE Transactions on Power Delivery*, vol. 28, no. 4, pp. 2403-2410, Oct. 2013.
- [21] F. Deng and Z. Chen, "Voltage-Balancing Method for Modular Multilevel Converters Switched at Grid Frequency," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2835-2847, May 2015.
- [22] M. Eremia, C.-C. Liu, and A.-A. Edris, *Advanced Solutions in Power Systems: HVDC, FACTS, and Artificial Intelligence*. Hoboken, NJ, USA: Wiley, 2016.
- [23] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4-17, Jan. 2015.
- [24] P. Hu and D. Jiang, "A Level-Increased Nearest Level Modulation Method for Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1836-1842, April 2015.
- [25] M. Alharbi, M. Mobarrez and S. Bhattacharya, "Control and performance analysis methodology for scale-up of MMC submodules for back-to-back HVDC applications," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 440-447.
- [26] N. Thitichaiworakorn, M. Hagiwara and H. Akagi, "Experimental Verification of a Modular Multilevel Cascade Inverter Based on Double-Star Bridge Cells," in *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 509-519, Jan.-Feb. 2014.