Design of a Medium Voltage Mobile Utilities Support Equipment based Solid State Transformer (MUSE-SST) with 10 kV SiC MOSFETs for Grid Interconnection

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***Abstract*—A conventional transformer can withstand multiple electrical, mechanical and thermal faults which enables it to have a long lifetime. However, its inability to control the power flow through it has led researchers to look for alternate options such as the solid-state transformers. With the Silicon Carbide (SiC) semiconductor devices, it is now possible to go to high switching frequencies in medium voltage applications, which helps in reducing the overall size and weight of the transformer. The advent of medium voltage (MV) SiC devices has enabled the use of simple two-level and three-level topologies for medium voltage power transfer. This paper discusses a basic power topology for a medium voltage mobile utilities support equipment based solid state transformer (MUSE-SST) with the new 10 kV SiC MOSFETs. A design of the MUSE-SST is presented followed by some of the practical considerations that needs to be taken, including gate driver design and heat sink configurations. Simulation results for a 100 kW, MV MUSE SST system is presented. Experimental results are provided validating the operation of these 10 kV devices in double pulse tests, buck and boost operation. This research helps in providing an overview regarding the usage of the 10 kV SiC devices in grid-interconnection and also discusses various challenges that comes along with it.**

Keywords*—*10 kV SiC devices, gate driver, grid interconnection, medium voltage, solid-state transformer, XHV-6 modules

I. Introduction

Typically, in a distribution system, the conventional transformer takes in thousands of volts and converts them to lower voltage levels that can be safely delivered to consumers [1]. The downside of the conventional transformers stems from the fact that they are bulky, often oil-cooled, and that they are not designed for rapidly changing loads. Moreover, power flow controllability is also an issue in case of these transformers. Medium voltage solid-state transformers (MV-SSTs) have the potential to replace the conventional transformers on account of the multitude of advantages in brings along with it [2], [3]. In addition to having a better power density as compared to conventional transformers, the SST offers a multitude of advantages which includes

- Controlling the power flow between different grid connections
- Limiting the fault currents
- Integration with energy storage units
- Provide voltage regulation and communication capabilities

Fig. 1 illustrates the differences between the conventional low frequency (LF) transformers and the new medium frequency (MF) solid state transformers. The power electronics converter stages in the SST enables control over its full range.

The increased penetration of renewable energy sources (PV and wind) has catalyzed the need to modernize the conventional power distribution system [4]. Moreover, the SSTs are of interest in traction applications due to its light weight and medium frequency isolation [3], [5]. Traditionally, for distribution grids (up to 13.8 kV and 60 Hz), higher order multilevel converters (more than three level) were mandatory. Availability of high voltage blocking SiC devices have enabled power converters without the use of complicated multilevel converters [2], [6]–[8].

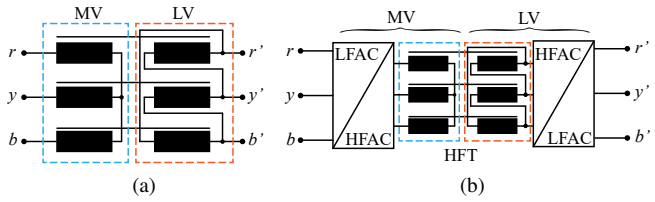

Fig. 1: Schematic of (a) a typical star-delta connected conventional line frequency transformer, and (b) a solid-state transformer. The galvanic isolation in the solid state transformer is provided by the high frequency transformer (HFT).

This paper describes a power topology for a MV MUSE-SST used for grid inter connection. The filter design for the LCL filters with $R_d - C_d$ damping and the control strategy which is used for controlling the power flow between the grids are also described. In addition, practical considerations, that needs to be taken care of while designing the MUSE-SST, including gate driver design, thermal management, and high frequency magnetics design considerations has also been provided. The working of the 10 kV SiC MOSFETs have been validated using double pulse tests, buck and boost operation.

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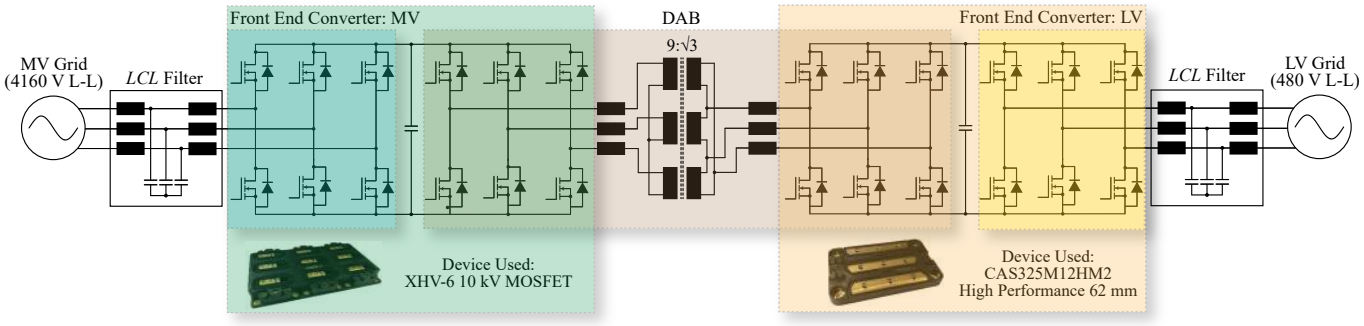


Fig. 2: Schematic of the hardware implementation of the overall system architecture. The MUSE-SST consists of three parts: MV AFEC, DAB and LV AFEC. In the actual system, the LCL filter has an additional $R_d - C_d$ damping.

II. Operational Overview

The MUSE-SST provides a concept for the replacement of a conventional 4.16 kV to 480 V distribution transformer. Several factors should be taken into account for comparing the conventional transformers with SSTs. Inherently, the size of the SST becomes smaller than that of the conventional low frequency transformers on account of having a high frequency transformer isolation stage. The exact study on the size ratio of the transformers is beyond the scope of the paper.

A. Efficiency

It should be noted that the efficiency of both the transformers have not been elaborately compared here on account of the fact that the losses in the high frequency transformer in MUSE-SST is difficult to predict. Simulation studies assuming losses in just the power electronic converters shows the efficiency of the SST to be around 98.5% as compared to an efficiency of 99% in conventional transformers of similar ratings [9]. The efficiency of the MUSE-SST is calculated assuming the rated power transfer. It should be noted that the efficiency of the MUSE-SST can be further improved by using better heatsinks (maintaining lower junction temperature). However, this compromises the power density and also leads to under-utilization of the SiC MOSFETs.

B. Reactive Power Capability

A generalized comparison is drawn for the reactive power capability of both the transformers. It is assumed that a 1 p.u VA load is connected to the system with a real power of 0.8 p.u and reactive power of 0.6 p.u. In this case, the conventional transformer supplies the same amount of load and draws the same amount of real power from the MV grid. It might result in a voltage dip and an increased line loss at the MV grid. In contrast, the MUSE SST is capable of handling the load at the LV feeder without drawing any reactive power from the MV grid. It draws 0.8 p.u real power from the MV grid and injects the 0.6 p.u. reactive power from the LV grid and hence decrease the line loss and support the voltage sag. Fig. 3 shows the reactive power capability of the MUSE-SST when compared to the conventional transformer.

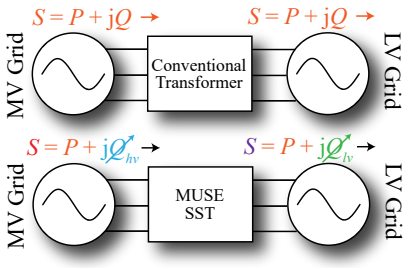


Fig. 3: Power flow direction of a conventional transformer and MUSE-SST. The conventional transformer draws both the active and reactive power from the MV grid where as the MUSE-SST is capable of supplying reactive power locally.

III. System Architecture of MUSE-SST

A schematic of the hardware implementation of the overall system architecture is provided in Fig. 2. In this system, an interconnection between a 4.16 kV - 60 Hz grid to a 480 V - 60 Hz is studied. The system consists of LCL with $R_d - C_d$ filters on either grid-connections. The voltage transformation is handled by the three-stages (Front-End Converter: MV, Dual Active Bridge and the Front-End Converter: LV).

A. Topology

In this topology, the 3-phase 4.16 kV grid voltage is rectified by a 3-phase 2-level inverter, followed by the DAB (which acts as a dc-dc stage) and a LV dc-ac inverter. The MV stage is isolated from the LV stage using a high frequency medium voltage transformer. This topology is enabled by Wolfspeed 10 kV, 75 A XHV-6 modules on the primary side and CAS325M12HM2 High performance Wolfspeed modules on the low voltage (LV) side [10].

B. Control Implementation

The control strategy for the MV and LV inverter is aimed at maintaining the corresponding dc-link voltages at 7.2 kV and 800 V respectively. A space-vector modulation scheme is adopted to avoid overmodulation. Fig. 4 gives the control strategy of the entire system. A synchronous-PLL is used to calculate the voltage angle. The dc-link voltage controller

generates the d-axis reference (i^*_{sd}) and the q-axis reference is fed by the user depending on the amount of VAR that needs to be injected. A PI current controller is used as an inner current control loop for maintain the current.

The control of DAB is done in a straightforward manner. Since, the dc-link voltage is maintained on either side of the DAB, only a phase angle control is implemented for the DAB. This method is simple and easy to implement. However, there are issues associated with in respect to transformer saturation. In order to avoid the transformer saturation, a rate limiter is implemented at the phase angle output which does not allow the phase angle to change abruptly. This makes the control slower as compared to other techniques. However, this helps in avoiding current sensing for the DAB currents and consequently, does not require any fast analog-to-digital conversion systems (ADCs).

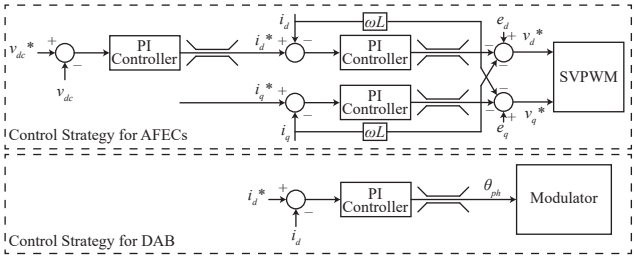


Fig. 4: Control block implemented for MUSE-SST. The MV and the LV AFEC use a similar control technique where a conventional PI controller is used to maintain the dc-link voltage on the MV and the LV side.

IV. System Design of MUSE-SST

The design of the converter system mainly includes the filter design for the LCL filters with $R_d - C_d$ and the high frequency transformer. The topology selection is also one of the major design challenges. However, with the use of 10 kV SiC MOSFETs, the system is kept simple and compact (2-level inverter) for this application which requires a 7.2 kV dc-bus. In the literature, three level topologies have been proposed [3]. However, even if three-level topologies bring in some advantages, it leads to additional complications both in terms of control and physical implementation. The design is therefore reduced down to the selection of the filters and the high frequency transformer. A LCL filter design with a $R_d - C_d$ is chosen for this system due to its better attenuation properties at higher frequencies as compared to L or LC filters [11].

A. Active Front End Converters

For the MV side, the voltage rating of 4.16 kV, requires a phase voltage of 3.4 kV peak. With the two-level active front end converter (Fig. 2), the dc bus voltage requirement is approximately 7.2 kV, considering 5% drop in the AC side filter. Similarly, the voltage rating of the LV side can be found to be 800 V dc-link voltage. Each switch is subjected to a stress of the total dc-link voltage. If snubberless circuit is used, then the peak voltage stress is dependent on the stray inductance in the switching loop when the current turns off. It is necessary that the busbars are designed for minimal stray inductance. The stray inductance forms a resonant tank circuit with the DC bus capacitance, which results in ringing during switching. Depending on the resonant frequency of this stray inductance and DC bus capacitance, the switching frequency ripple rating of the DC bus capacitor is determined.

A LCL filter with $R_d - C_d$ damping is chosen for filtering the grid current harmonics on both the sides as shown in Fig. 5 [11], [12]. The design procedure is exactly the same for both the filters (MV and LV side). A total inductor drop at fundamental frequency is considered to be 5% p.u. The filter capacitor current is assumed to be 10% p.u.

$$C_f + C_d = \frac{0.1}{2 \times \pi \times 60 \times Z_{p.u.}} \tag{1}$$

$$L_g + L_s = \frac{0.05 \times Z_{p.u.}}{2 \times \pi \times 60} \tag{2}$$

A preliminary value of resonance frequency (ω_{res}) is chosen which should be more than five times away from 420 Hz (seventh harmonic) and lower than one-fifth of the switching frequency of 10 kHz (for AFEC: MV) and 20 kHz (for AFEC: LV).

$$\omega_{\text{res}} = \sqrt{\frac{L_\text{s} + L_\text{g}}{L_\text{s} \times L_\text{g} \times (C_\text{f} + C_\text{d})}} \tag{3}$$

Solving (1) and (2), the inductor values are calculated.

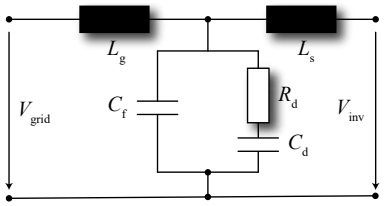


Fig. 5: Filters used in MUSE-SST. This filter is preferred to conventional LCL filters due to reduced losses in the damping resistor.

B. Dual Active Bridge Converter

The dual active bridge converter, in this topology, is a three-phase converter. A three-phase 2-level converter supplies the primary side of the AC high frequency transformer in a star configuration. The secondary side of this high frequency transformer is connected to the three-phase two level converter employing low voltage (1200V) SiC MOSFET switches in delta configuration. The effective leakage inductance is calculated using the power flow equations.

$$P = \frac{3(V_1/n)V_2 \sin(\phi)}{L_{12}\omega} \tag{4}$$

$$Q = \frac{-3(V_1/n)V_2 \cos(\phi) + V_2^2}{L_{12}\omega} \tag{5}$$

where P and Q represent the active and reactive power processed by the DAB, ϕ gives the phase shift angle between the primary and the secondary sides of the transformer. The

TABLE I: Summary of the key design results for MUSE-SST

MV side Front End Converter			Dual Active Bridge			LV side Front End Converter		
	Parameter	*Value*		*Parameter*	*Value*		*Parameter*	*Value*
	Power	100 kW		Turns Ratio	$9/\sqrt{3}$		Power	100 kW
	DC-bus voltage	7200 V		RMS AC Voltage Rating	3395 V/ 656 V		DC-bus voltage	800 V
	AC-voltage (L-L)	4160 V		Peak AC Voltage Rating	4800 V/ 805 V		AC-voltage (L-L)	480 V
	AC side current	14 A		RMS AC Current Rating	22 A/ 55.24 A		AC side current	120 A
	Semiconductor Device			Peak AC Current Rating	30 A/ 83 A		Semiconductor Device	
	Device Rated Voltage	10000 V		Nominal Frequency	20 kHz		Device Rated Voltage	1200 V
	Device Rated Current	75 A		Leakage Inductance (HV)	1.8 mH		Device Rated Current	325 A
	Switching Frequency	10 kHz		Mag. Inductance	656 mH		Switching Frequency	20 kHz
	LCL Filter			Max. Step Voltage (MV)	4800 V		LCL Filter	
	Grid Side Inductor	7.7 mH		Max. Step Voltage (LV)	800 V		Grid Side Inductor	0.1 mH
	Conv. Side Inductor	15.3 mH		Insulation Design	20 kV		Conv. Side Inductor	0.2 mH
	Filter Capacitance	1.5 uF					Filter Capacitance	21 uF
	Damping Resistance	20 Ω					Damping Resistance	3.7 Ω
	Corner Frequency	1800 Hz					Corner Frequency	3000 Hz

voltages are referred to the secondary side of the transformer. It should be noted that the phase shift angle should not be kept very high (leads to increased reactive power flow) or very low (hampers controllability). This design considers a rated phase shift angle of 45^o for a real power transfer of 100 kW. Fig. 6 gives the active and reactive power transfer capability according to the phase shift angle.

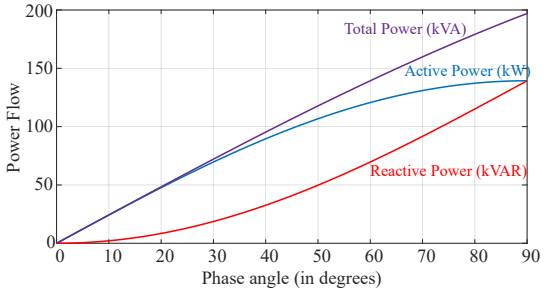


Fig. 6: Relation of phase angle with the power processed by the DAB. The operating point is generally taken at the middle (45° for the rated condition.

C. High Frequency Transformer

A star-delta configuration is chosen for the 3-phase connection on the primary and the secondary side of the transformer [13]. The star-delta configuration is chosen to minimize the turns ratio. The turns ratio is chosen in the same ratio as the dc-link voltages to ensure ZVS for the maximum voltage range. The leakage inductance is not a major factor that is taken into consideration since additional inductors are put in series in order to have better controllability over the effective leakage inductance. The magnetizing inductance is calculated to be 300 mH using a 5% of full load current. The most important criteria while designing a MV high frequency transformer is its insulation ratings. The insulation rating should adhere to the BIL ratings for a working voltage of 7.2 kV [14]. The electrical design parameters for MUSE-SST is summarized in Table I.

V. Practical Design Considerations

A number of things should be taken care of, while implementing the MUSE-SST in practice. Gate drivers need to be designed for both the MV and the LV systems. In addition, the heatsink design has to be made to remove the heat from the devices. In addition to the auxiliary supplies, the practical designs of the filter inductors and the transformers is very essential. The major problem which is seen in MV devices is the high dv/dt experienced by the system. This high dv/dt makes it necessary to design the high frequency transformer, filter inductors and gate drivers with very less parasitic capacitances. The magnitude of the common mode (CM) current (I_{cm}) is directly affected by the dv/dt and isolation/ parasitic capacitance (C_p)

$$i_{cm} = C_p \frac{dv}{dt} \tag{6}$$

A. Gate drivers

The gate driver design is one of the most important criteria for driving MV SiC MOSFETs. The gate driver should be designed considering three main parameters

- High isolation voltage between primary and secondary
- Low coupling capacitance between primary and secondary
- Small, optimized footprint while maintaining the insulation standards

In practice, a trade-off is made between the size of the gate driver and the coupling capacitance. Fig. 7 shows the designed gate-driver for MUSE-SST. The gate driver transformer is designed to have a minimized parasitic capacitance for driving the SiC MOSFETs with such high dv/dt. The isolation capacitance of the designed gate driver is around 0.25 pF. Fig. 8(a) and Fig. 8(b) validate the operation of the gate driver by double pulse tests at 7.2 kV and 7.5 kV dc-link voltage, respectively. The common mode current is observed and the isolation capacitance can also be deduced from the same (by measuring the dv/dt of the voltage). The same gate driver is used for the continuous operation of the MV devices.

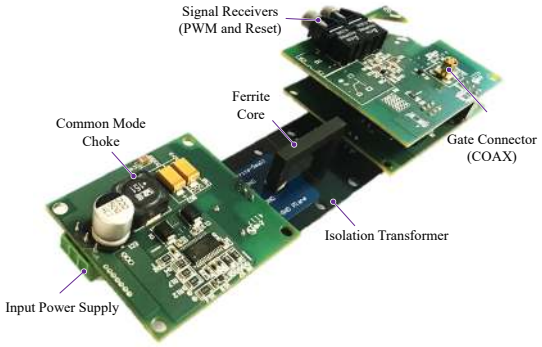


Fig. 7: Designed gate driver for driving 10 kV SiC MOSFETs in the high voltage side of MUSE SST. The overall dimensions are 6 in $\times$ 2 in $\times$ 1.5 in.

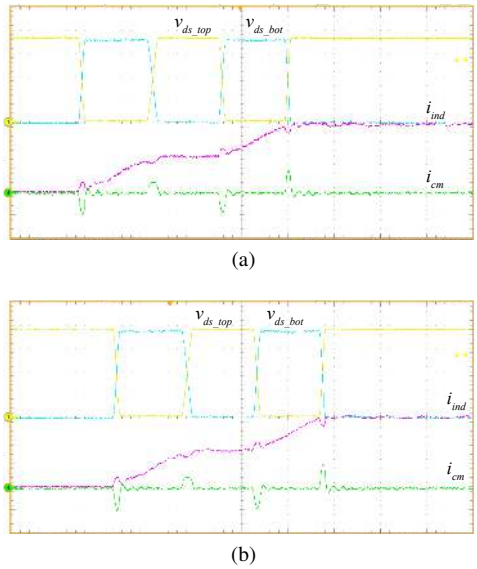


Fig. 8: Double pulse tests to validate the gate driver operation at (a) 7.2 kV, and (b) 7.5 kV dc-link bus voltages. The common mode currents through the gate driver can be observed. (Scale:- Ch1 (v_{ds_top}): 2 kV/div; Ch2 (v_{ds_bot}): 2 kV/div; Ch3 (i_{ind}): 2 A/div; Ch4 (i_{cm}): 90 mA/div; Time: 2 µs/div).

The fabricated LV gate driver is shown in Fig. 9. The routing is conducted carefully such that the high-speed signals have differential path to increase the noise immunity. The gate driver is built with two isolated channels on the same printed circuit board (PCB), which can drive two devices on one CAS325M12HM2 independently. Gate power is isolated through galvanic isolation of a transformer and the gate signal is isolated through optical isolator. The interface between the gate driver and control board is solely through optical cables which has better common mode performance.

B. Thermal Solutions

Conventional heatsink designs include naturally cooled or forced air cooled fin-type heatsinks. MUSE-SST employs a more efficient thermal solution which uses a thermosyphoon based product manufactured by Advanced Cooling Technolo-

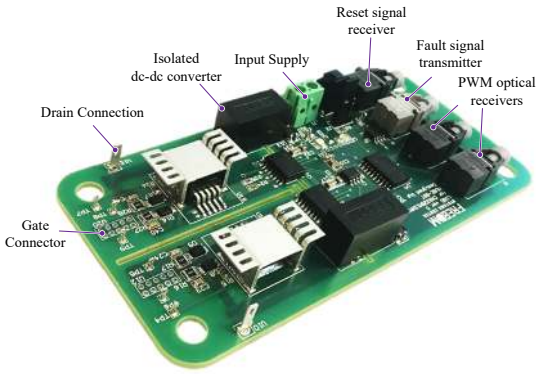


Fig. 9: Designed gate driver for driving CAS325M12HM2 in the low voltage side of MUSE SST. The overall dimensions are given by 5 in $\times$ 2.5 in $\times$ 0.75 in.

gies (ACT) [15]. Heat generated by the power semiconductor devices causes liquid inside the evaporator to change its phase. This expansion of the liquid in the evaporator combined with the condensation of liquid in the condenser, generates a gravitational pressure imbalance which maintains fluid circulation between the condenser and evaporator [15]. Fig 10(a) and Fig. 10(b) shows the thermal solutions for both the MV and the LV side assembly, respectively. The heatsinks are designed

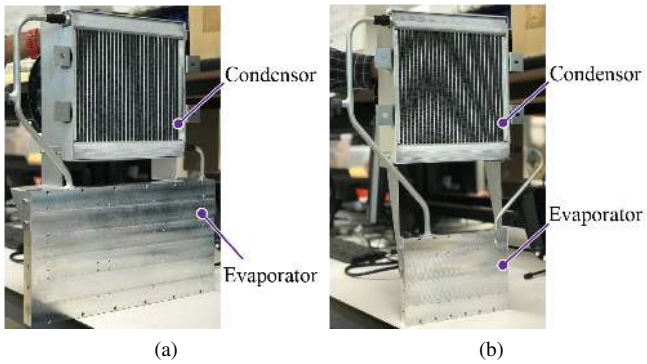
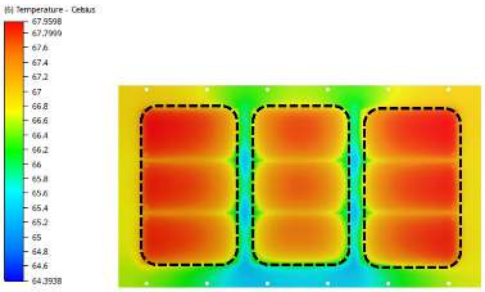
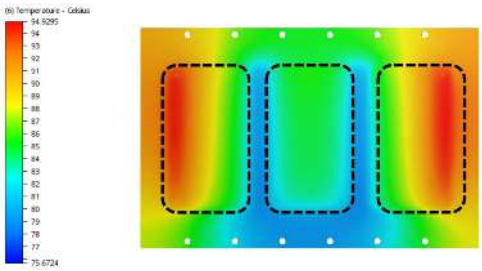


Fig. 10: Loop thermosyphoon used for cooling the power semiconductor devices for (a) MV power devices, and (b) LV power devices.

to handle up to 2 kW of power losses for a temperature rise of 70°C. The heatsink is over designed for MUSE-SST application in order to maintain a significantly lower junction temperature since the 10 kV SiC MOSFETs is not a matured technology yet. Thermal simulation results showing the temperature distribution of the evaporator assembly for both the MV and the LV side is shown in Fig. 11a and Fig. 11b, respectively. A maximum power dissipation of 2 kW is taken for both the evaporators. The maximum cold plate temperature of the MV evaporator reaches around 68°C. A similar analysis on the LV evaporator shows the maximum coldplate temperature to be around 95°C. Combining these results with the thermal resistance of the module, the junction temperature is found to be maximum 85°C for the MV power devices and 112°C for the LV power devices. These are well within the specified limits.



(a)



(b)

Fig. 11: Thermal simulation results for the loop thermosyphoon used for cooling the power semiconductor devices for (a) MV power devices, and (b) LV power devices. A maximum power dissipation of 2 kW is taken for both the evaporators.

C. High Frequency Magnetics Design

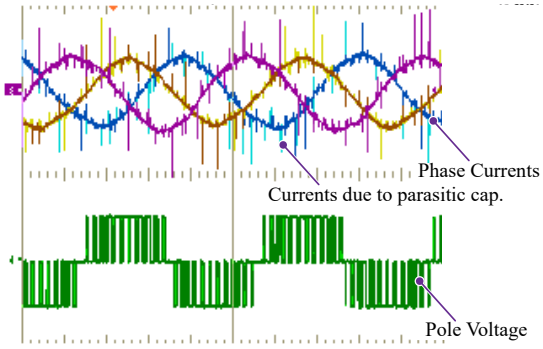
The practical design of the high frequency magnetics is very important for MV SiC MOSFETs due to the high dv/dt associated with these devices. The parasitic capacitances across the filter inductors and the high frequency transformer leads to an additional common mode current. The paths for the common mode current is shown in Fig. 13. The common mode current flows through the devices and cause additional switching and conduction losses. This current spikes can lead to device failure also, if an abundant safety margin is not considered. Fig. 12(a) and 12(b) shows the effect of the parasitic capacitors on the current waveform for the front-end converter and the dual active bridge respectively.

VI. Simulation and Experimental Results

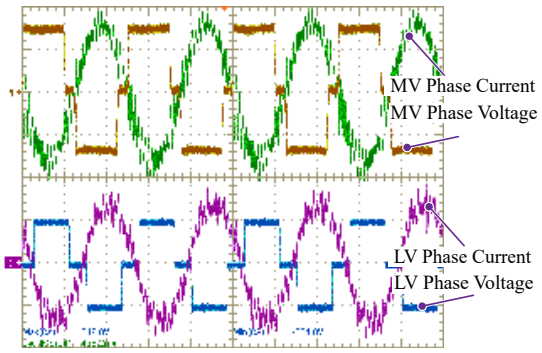
They key parameters used in the simulation is summarized in Table I. The parasitic elements in the filter inductors or the high frequency transformer has not been considered for the system simulation.

A. Simulation Results

Fig. 14(a) shows the grid current, inverter current, filter capacitor voltage and the dc-bus voltage for the MV front end converter. Initially, it is assumed that the grid is disconnected. The grid connection is turned on at 0.2s. Similarly, the simulation results for the LV side converter is shown. Here, the power reference is changed at 0.1s and the system behavior is observed. Both the converters side grid current exhibit a THD within 5%, which validates the filter designs. The simulation results for the DAB is shown in Fig. 14(c) and Fig. 14(d).



(a)



(b)

Fig. 12: Experimental waveforms illustrating the effect of parasitic capacitances across the (a) filter inductors in the front end converter (Scale: Pole Voltage 1 kV/div and Phase Currents 2 A/div), and (b) primary and secondary side of the dual active bridge (Scale: MV Phase Voltage 1 kV/div, LV Phase Voltage 200 V/div, MV Phase Current 1 A/div and LV Phase Current 10 A/div). It should be noted that these tests are conducted on 15 kV SiC IGBTs [2].

B. Experimental Validation of 10 kV SiC MOSFETs

The basic building block for the MV side converters is the 10 kV SiC MOSFET. The packaging of the dies into a module is done in a compact way while maintaining the clearance and creepage requirements. Since, the 10 kV SiC MOSFETs have not yet been a mature technology, there are a lot of challenges involved in its design and operation. The realization of MUSE-SST system in a hardware setup needs to be done after figuring out the issues associated with the continuous operation of 10 kV SIC MOSFETs. The design of the gate driver and initial double pulse tests has already been discussed. The next step involves a testing of the 10 kV SiC MOSFETs in a continuous operating mode. Initially, the device is switched at no load (half-bridge configuration with no inductors or resistors connected to the midpoint) as shown in Fig. 15(a). The top and the bottom power devices are switched alternately to make sure that the gate driver can handle the no load dv/dt and to figure out any issues with the common mode currents through the ground. The device is tested upto 6.5 kV in this case. Fig. 15(b) shows the synchronous buck operation at no load of the XHV-6 module with an input voltage of 2.8 kV and a peak current of 10 A. The common mode current is measured at the input to the gate driver of the top-side device.

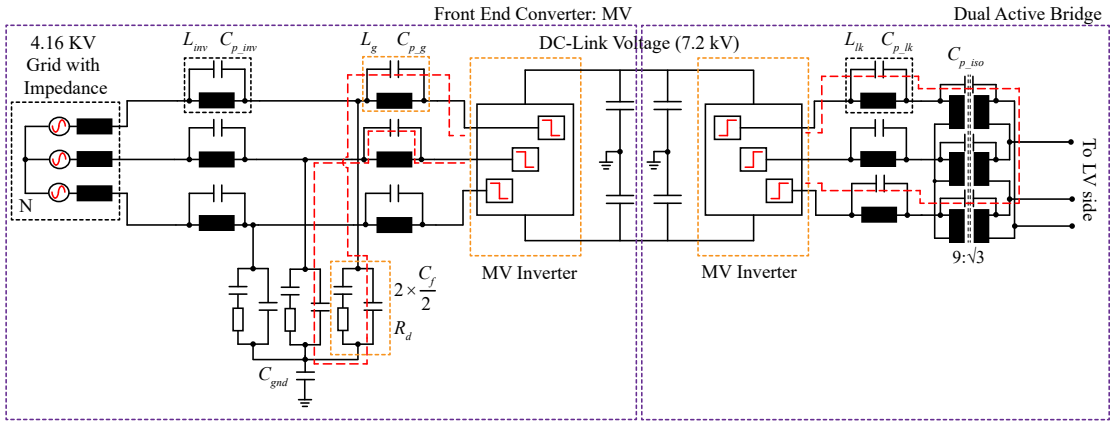


Fig. 13: Path for the common mode currents which arise due to the parasitic capacitances across various components and the high dv/dt associated with the device switching. These currents are mainly seen in the MV side converter since the dv/dt of the switches are comparatively higher than those of the LV devices.

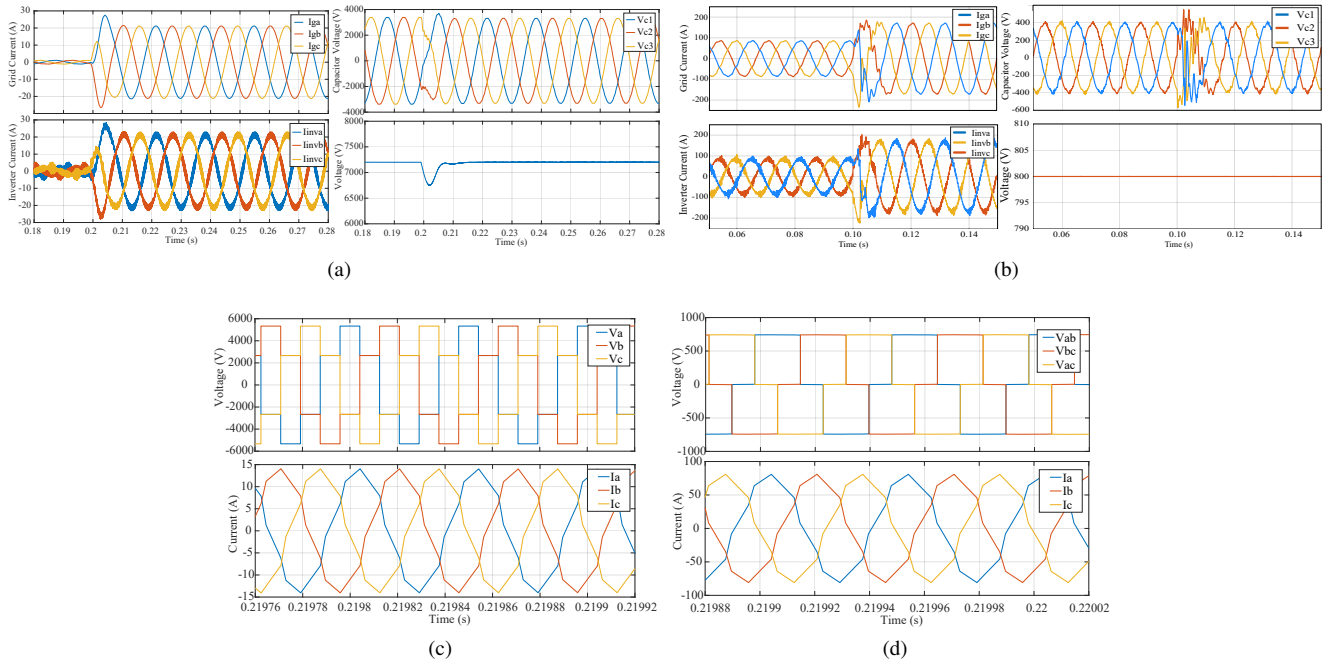


Fig. 14: Simulation results for the (a) AFEC: MV (Top left: Grid Current; Bottom Left: Inverter Current; Top Right: Capacitor Voltage and Bottom Right: DC-bus voltage. The control starts at 0.2 s.) and (b) AFEC: LV (Current Reference is changed from 85 A to 170 A at 0.1 s) (c) Voltage and Current waveforms for the DAB MV Side (d) Voltage and Current waveforms for the DAB LV Side.

The common-mode current is found to be very less and well within limits. This can be attributed to the design of the gate driver transformer. The synchronous buck operation at no load validates the soft switching operation of the converter. The XHV-6 module as well as the gate driver is tested for hard switching in a synchronous buck operation with a resistive load as shown in Fig. 15(c). The final validation of the XHV-6 module is carried out by its use in a boost converter where the voltage is boosted from 2100 V to 5.5 kV as shown in Fig 15(d). It should be noted that the tests are down up to 6 kV in continuous mode operation since the voltage protection is kept at 6.2 kV in order to avoid any catastrophic failures.

VII. Conclusions

In this paper, the design and control of a MUSE-SST is presented along with some practical considerations needed to implement it. The MUSE-SST is expected to be an attractive alternate solution for the distribution transformer in terms of providing ancillary services and power density. The aim of this paper is to provide and overview and design procedure for building and testing MUSE-SST. A brief idea regarding the gate driver, the thermal solutions and the effect of the magnetics parasitics on the entire system is discussed. The 10 kV SiC MOSFETs' operation is validated using double pulse

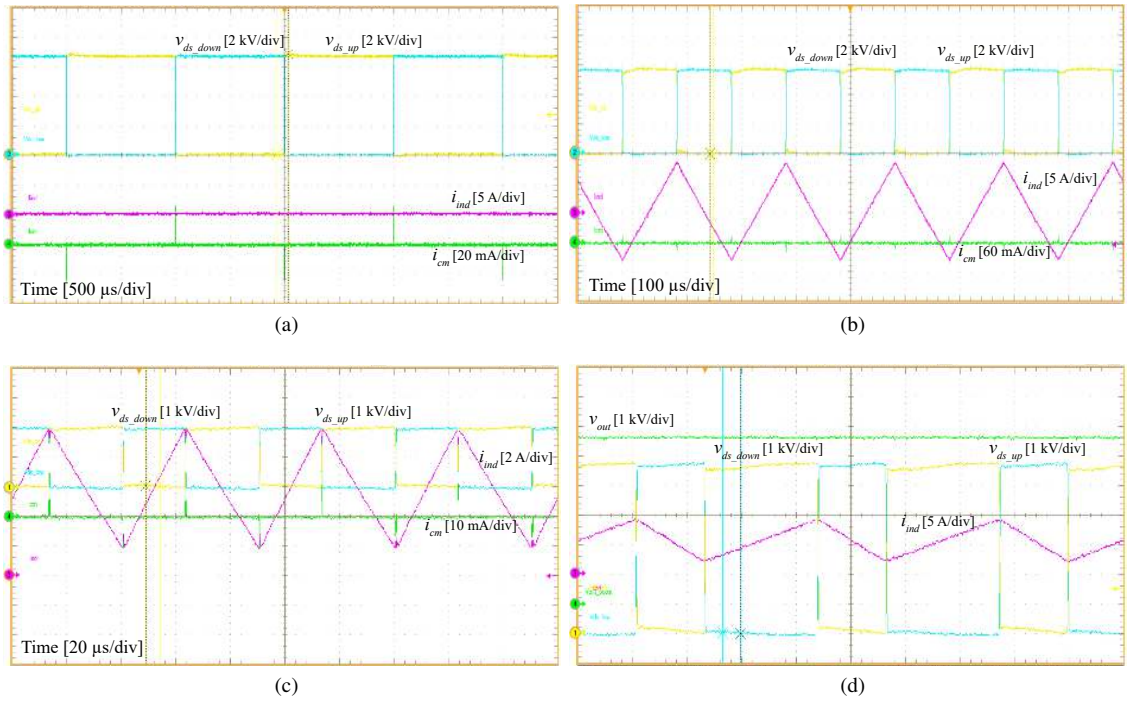


Fig. 15: Experimental results for validating the operation of the 10 kV MOSFET in the XHV-6 packaging. (a) Operation at no load and a dc-input of 6.5 kV at 500 Hz. The high voltage supply is limited in its current output capability which prevents the tests at higher voltage levels (b) Operation at a synchronous buck mode at no load. (c) Operation at synchronous buck mode with a resistive load (d) Boost mode of operation where the boost duty cycle is taken to be 0.65. The reference scales and time divisions are provided in the respective figures.

and continuous tests at different voltage and current levels to ensure its proper operation when connected to the MUSE-SST system. This research aims at at being a building block for implementing and testing the MUSE-SST system.

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