Practical Design Considerations for MV LCL Filter Under High dv/dt Conditions Considering the Effects of Parasitic Elements

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***Abstract*—For high power medium voltage (MV) grid connected applications LCL filter proves to be an attractive solution to filter out the current harmonics when compared to L or LC filters. The inductance requirement reduces drastically to meet the same Total Harmonic Distortion (THD) standards for grid connections for LCL filters compared to L filter which makes the system dynamics much faster. The increasing use of Silicon Carbide (SiC) based power devices for MV applications has made the effects of the parasitic elements in the filter more prominent, due to the high dv/dt experienced by the passive filter elements during device switching transients. This paper addresses the issues associated with the high dv/dt experienced by the LCL filters for SiC-based MV applications. In order to study these effects, the parasitic elements of the inductor are modeled and analyzed. A suitable solution is proposed to improve the overall system performance. The effect of high dv/dt on the filter and the effectiveness of the proposed solution are validated using simulation. Experimental data is also provided to validate the proposed concept.**

***Keywords*—10 kV SiC devices, gate driver, grid interconnection, LCL filters, medium voltage, inductor parasitics, solid-state transformer, XHV-6 modules**

I. Introduction

Medium voltage (MV) SiC-based semiconductor power devices have paved way for a new class of MV converters where it is possible to use a two level three phase inverter topology to connect directly to the MV (4.8 KV) grid [1]. This eliminates the need of complicated multi-level topologies which relies on the circuit level solutions to go to higher voltage levels where many number of converter blocks are connected in series [2].

Fast switching capability, low losses, and higher thermal capacity make SiC based power devices potentially great for any MV applications [3]. A MV converter may be used as an active rectifier, with the advantages of full control of both dc-link voltage and power factor, and its bidirectional power handling ability [4]. Furthermore, in higher voltage levels, the current rating of the system comes down drastically which helps in reducing the size of the conductors and hence minimizes the copper usage. However, lower current levels of these converters leads to requirement of higher value of the filter inductance to meet the total harmonic distortion (THD) standards for grid connection and hence the inductor design needs higher number of turns for the same core cross sectional area. Also the higher voltage level calls for higher insulation levels between the core and the winding. All these issues results in higher parasitic capacitance between the magnetic core and the inductor winding. A high value of input inductor can be used as a filter element. However, for applications above several kilowatts, it becomes expensive to realize these filter reactors [5]. Moreover, the system dynamic response becomes poorer. An alternative solution is to use an LCL filter (or an LCL filter with damping as shown in Fig. 1b and Fig. 1c [6], [7]. With this solution, optimum results can be obtained in the range of power levels up to hundreds of KVAs while using small values of inductors and capacitors [8].

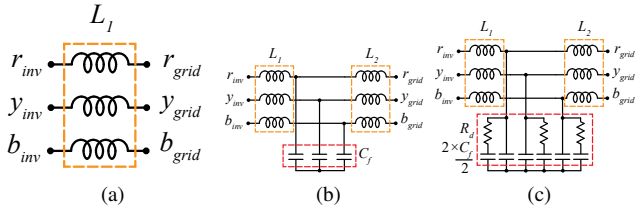

Fig. 1: (a) L filter (b) LCL filter, and (c) LCL filter with $Rf - C_f$ damping.

For SiC based solutions, very fast switching transients pose several challenges in a converter system design. The parasitic in the circuit layout becomes much more prominent. It is therefore necessary to minimize the effect of parasitic elements of all the filtering components. When an inductor is used as a filter element, measures have to be taken to minimize the parasitic capacitance since during SiC-MOSFET switching transients the voltage gradient can reach as high as 100 kV/µs [9]. The additional currents ($I_{cap,ind}$) flows through the parasitic capacitor of the inductor and also through the SiC devices causing additional losses in the system. This is given by

$$I_{cap,ind} = C_{p,eq}\frac{dv}{dt} \tag{1}$$

where $C_{p,eq}$ is the equivalent capacitance in the capacitive current path.

For a two-level inverter in grid-connection mode, typically L or LCL filters with passive damping are used as shown in Fig. 1. For LCL filters, the inductance requirement re-

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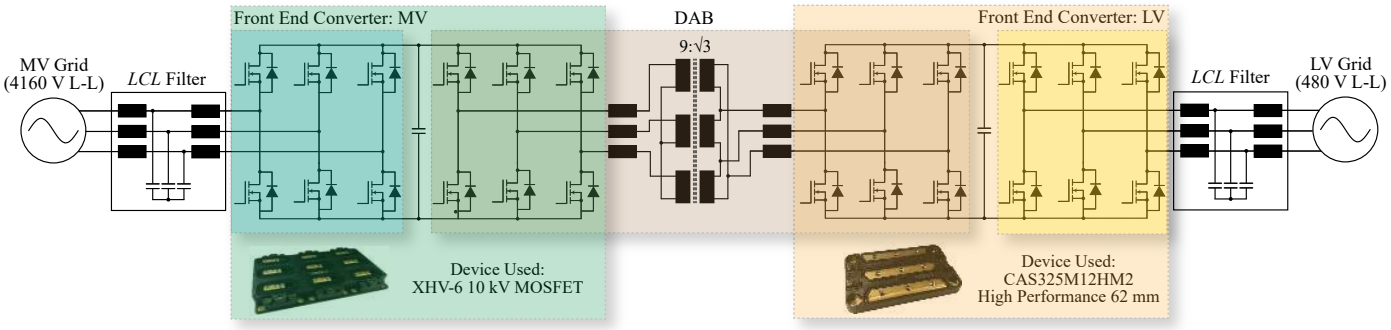


Fig. 2: Hardware Schematic of the SST topology with a power rating of 100 kW and integrating a 4180 V - 60 Hz grid with a 480 V -60 Hz grid. The analyzed system uses an additional $R_d - C_d$ branch along with the conventional LCL filters.

duces drastically as compared to L filters which makes the system dynamics much faster. However, the current through the parasitic capacitor is more pronounced in LCL filters as compared to L filters as explained later in the paper. This paper addresses the issues associated with high switching dv/dt, and consequently the additional currents experienced by the filters due to the parasitic capacitance for SiC-based MV applications. A LCL filter with passive damping, connected with a two-level inverter with a dc-bus voltage of 7.2 kV is considered for analysis. A suitable solution is proposed for minimizing these additional capacitive currents, and thus improving the system performance.

II. Converter Architecture of a MV-Solid State Transformer (SST) Topology

Fig. 2 depicts the schematic of the hardware implementation of a MV converter system architecture. This system interconnects between a 4.16 kV - 60 Hz grid to a 480 V - 60 Hz. The system consists of LCL filters with $R_f - C_f$ damping on both MV and LV grid-connections. The power conversion stage is divided into three stages (Front-End Converter: MV, Dual Active Bridge and the Front-End Converter: LV).

In this topology, the 3-phase 4.16 kV grid voltage is rectified by a 2-level inverter, followed by the DAB (which acts as a dc-dc stage with high frequency isolation) and a LV dc-ac inverter. The MV stage is isolated from the LV stage using a high frequency medium voltage transformer. The aimed power rating of the system is 100 KVA. This topology is enabled by Wolfspeed 10 kV, 75 A XHV-6 modules on the MV side and CAS325M12HM2 Wolfspeed modules on the low voltage (LV) side [10].

A. MV side LCL filter design

Compared to a first order L filer, the LCL filter can meet the grid interconnection standards with significantly smaller size and cost, particularly for application above several kilowatts. However, it can also trigger a resonance between inverter and the grid if proper damping is not ensured [8]. In the literature, several active or passive damping methods have been discussed to avoid this issue [11]. If the grid impedance does not change widely, passive damping method should be preferred

TABLE I: Designed LCL parameter with passive damping

Parameter	*Designed Values*
KVA Rating	100 kVA
AC line-line voltage (V_g (rms))	4160 V
DC bus voltage (V_{dc})	7200
Switching frequency (f_{sw})	10 kHz
Resonance frequency (ω_r)	1.8 kHz
Grid side inductor (L_g)	7.7 mH
Converter side inductor (L_{inv})	15.3 mH
Filter capacitor (C_f)	1.5 μ F
Damping resistance (R_d)	120 Ω

owing to its simpleness and low cost. In the passive damping method, a resistor is inserted in series with the filter capacitor. The damping resistor weakens the high frequency harmonic attenuation ability of the LCL filter and also increases extra power loss in the system. To counter these issues, an additional $R_d - C_f/2$ branch in parallel with $C_f/2$ is inserted as shown in Fig. 1(c). The damping resistor is optimized to get the maximum damping with minimum power loss [12].

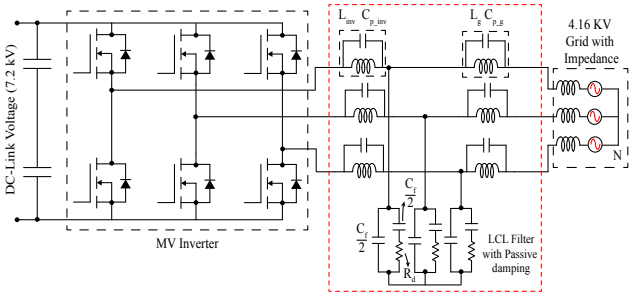


Fig. 3: LCL Filter with passive damping resistor

The switching frequency of the MV converter is designed to be at 10 kHz. The resonance frequency (ω_{res}) of the LCL filter is placed at 1800 Hz (by design) which is more than five times away from 420 Hz (7^{th} harmonic) and lower than one-fifth of switching frequency. The inductors are designed considering 5% drop and the filter capacitor is calculated assuming 2.5% ripple current capability. Considering these constraints, the filter elements are designed and the values are tabulated in Table. I.

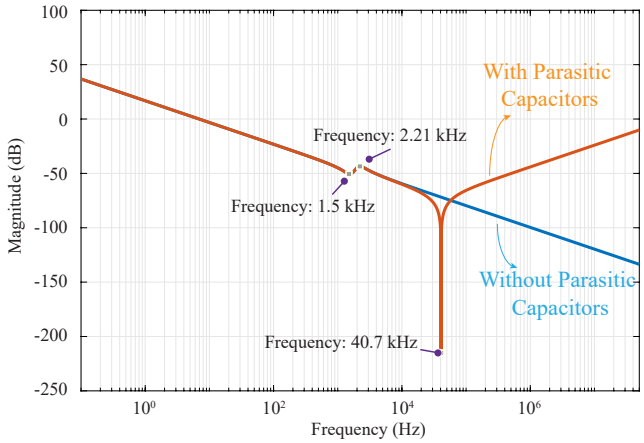


Fig. 4: Bode plot between inverter current and inverter voltage ($G(s) = I_{inv}/V_{inv}$) with and without parasitic capacitance of the inductors. This plot shows the admittance seen by the inverter.

B. Parasitic elements in the filter inductance

The MV side converter interfaces 4.16 kV grid with 7.2 kV DC bus voltage. At these voltages the filter inductors have to be designed with 60 kV insulation class [13]. Moreover, since the inductance value is in the milli-henries range, the number of turns for each of the inductors is high. This results in a high value of winding to winding as well as layer to layer capacitance. Hence, the parasitic capacitance of the inductor is expected to be high and considering a practical design case, the parasitic capacitance value can go in the nano-farad range. The inverter side inductor and the grid side inductor capacitances are represented as C_{p_inv} and C_g respectively in Fig. 3. The inverter current response depends on the LCL parameters. The bode plot of the transfer function between inverter current and the inverter output voltage is shown in Fig. 4. The figure overlays two transfer functions: one without the inductor parasitic capacitances and the other one with parasitic capacitances.

It should be noted that the parasitic capacitance of the grid side inductor (L_g) has very little influence on the bode plots since this capacitance effectively comes in parallel with the main filter capacitance and since the main filter capacitance value is much higher than the parasitic capacitances, the grid side inductor's parasitic capacitor has minimal influence.

TABLE II: Parasitic capacitances of the inductors

Inductor	*Parasitic capacitance*
Grid side inductor (L_g = 7.7 mH)	C_{p_g} = 503 pF
Converter side inductor (L_{inv} = 15.3 mH)	C_{p_inv} = 1000 pF

Fig. 4 indicates that the parasitic capacitance associated with L_{inv} introduces complex conjugate zeros which is located at the resonance due to L_{inv} and C_{p_inv}. The parasitic components are tabulated in Table. II. From the bode plots it is clear that at higher frequencies the inverter sees a capacitive impedance. The per phase equivalent circuit shown in Fig. 5. At higher frequencies clearly the capacitances provide the least impedance path shown in the figure.

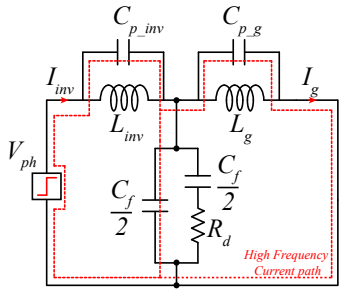


Fig. 5: Per phase equivalent circuit of the LCL Filter

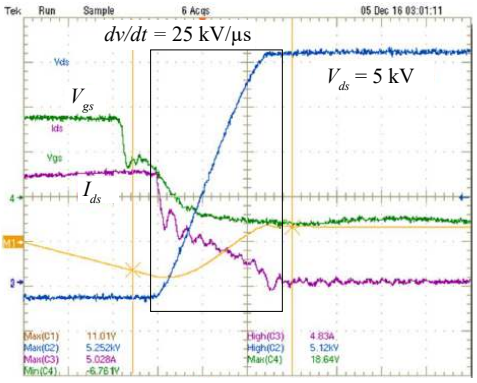
C. Turn ON and OFF dv/dt of Medium Voltage SiC-MOSFET

The presented converter is designed with the state of the art 10 kV SiC-MOSFET based XHV-6 module from Wolfspeed [10]. These devices can work at very higher switching frequencies at MV level because of the fact that the switches have a very low switching and conduction loss performance. This helps in improving the converter efficiency. However, the turn ON and OFF dv/dt is very high for these devices. At the intended operating voltage and currents, the switching transitions can experience a dv/dt as high as 100 kV/µs (worst case scenario). Fig. 6b shows one of the experimental cases where a dv/dt of 65 kV/µs is observed. It can be pointed out from Fig. 6a and 6b that the turn ON experiences much higher dv/dt than turn OFF because of the fact that the turn ON process involves turning OFF of the body diode of the complementary device.

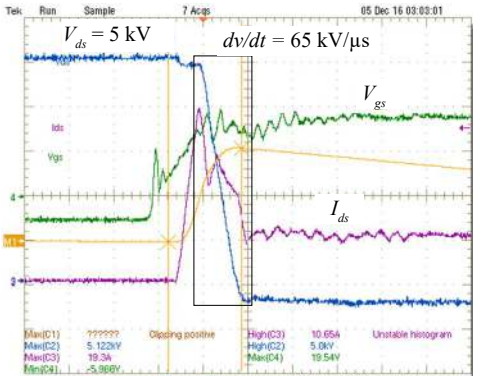
III. Path for dv/dt currents and Proposed Filtering Technique

The high dv/dt of the SiC-devices calls for careful design of the system parasitics. At these high dv/dt, the parasitic capacitance of the inverter side inductor along with the filter capacitance provides a significantly low impedance path at higher frequencies and hence it is expected that for the LCL filter case, the inverter side current I_{inv} will have current spikes at every switching transients of the SiC-MOSFET switch. All these current spikes flows through the SiC-devices which is detrimental to the device, as in many cases the current spikes may exceeds the rated device current and damage it over a period of time.

If an inductive filter is used, the total capacitive current path is decided by the parasitic capacitance of the filter inductance along with the grid impedance as shown in Fig. 7. In this case, the parasitic capacitance of the inductor comes in series with the grid impedance. Since the grid impedance is distributed in nature the effective capacitance becomes very small. However, when a LCL filter is used, the filter capacitor decouples the grid impedance and the filter inductance. In this case, the capacitive current which originates due to the dv/dt experienced by the filter has a defined path to flow (through the filter capacitors) as shown in Fig. 8. This current is differential in nature and flows through the semiconductor devices. In practice there will also be path for the common mode (CM) current along with this which worsens the current waveforms. This is shown in Fig. 9 at 3 kV dc bus voltage and 2 kW in the standalone inverter mode of operation. The presence of 2 A



(a)



(b)

Fig. 6: (a) Turn-off and (b) turn-on waveforms for a third-generation 10 kV XPM3-10000-0350-B7 SiC MOSFETs (building die of the XHV-6 module). The dv/dt for these tests is seen to be as high as 65 kV/μs. Testing is done for 5 kV, 5A for a gate resistance of 4.7 Ω. (Ch2: V_{ds} = 1 kV/div; Ch3: I_{ds} = 5 A/div; Ch4: V_{ds} = 10 V/div)

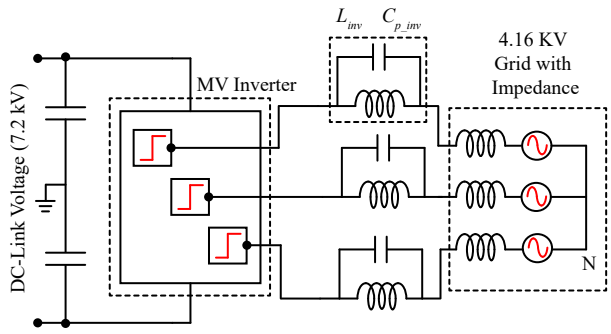


Fig. 7: Path for the current which flows due to the high dv/dt experienced by the L filter due to the fast switching transients

current spikes is due to the 9 kV/μs dv/dt (at 1.5 kV blocking voltage) and the parasitic capacitance across the filter inductor. This effect becomes severe with higher voltages (which leads to higher dv/dt) which leads to EMI issues. In addition. this results in a significant increase in the switching losses.

To reduce this current spike, it is proposed to split the required inverter side inductor into two parts. One part makes the majority of the inductance required. This inductor can have bigger amount of parasitic capacitance. The second one

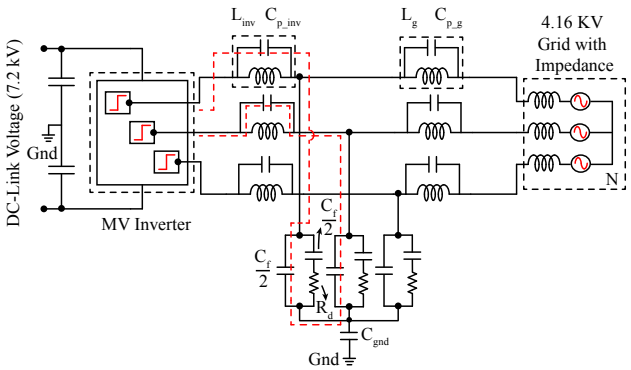


Fig. 8: Path for the current which flows due to the high dv/dt experienced by the LCL filter due to the fast switching transients

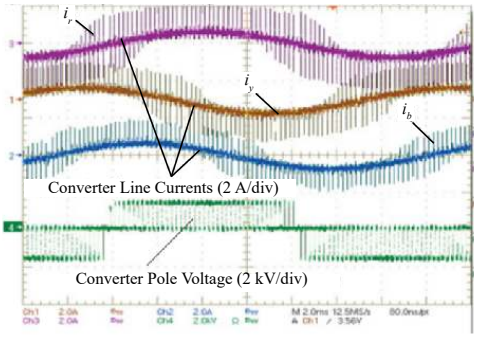


Fig. 9: Three phase converter currents in a stand-alone inverter system. This result has been obtained using 15 kV SiC IGBTs at 3 kV dc bus voltage and 2 kW in the inverter mode [1]. (Scale - Ch1: 2 A/div, Ch2: 2 A/div, Ch3: 2 A/div) and pole voltage (Ch4: 2 kV/div).

forms a small amount of inductance with minimized parasitic capacitance. The division of the inductance is shown in Fig. 10. In series, the effective capacitance is decided by the smaller parasitic capacitance.

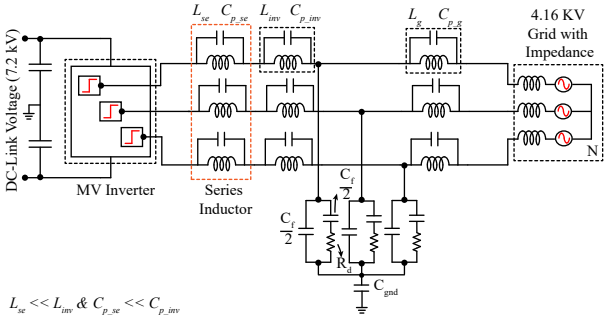


Fig. 10: Distribution of Inductance in LCL filter ($L_{dist} << L_{inv}$; $C_{p_dist} << C_{p_inv}$)

As mentioned, the problem with the additional current due to the dv/dt experienced by the filter can be reduced by reducing the effective parasitic capacitance. The power quality is mainly a concern at higher voltage and lower current levels in non-cascaded structure. Fig. 11 shows the bode plot of the transfer function between inverter current and the inverter voltage when

TABLE III: Series Inductor with damping resistor

Element	*Value*
Series inductor (L_{se})	200μH
Parasitic Capacitance (C_{p_se})	100 pF
Series Damping Resistor (R_{se})	5000 Ω

the inverter side inductor is split into two parts (shown in Fig. 10) and connected in series. As indicated in the figure,

$$\begin{aligned} L_{se} &<< L_{inv} \\ C_{p\_se} &<< C_{p\_inv} \end{aligned} \tag{2}$$

This relation indicate that the small inductor L_{se} can be designed with tight regulation on its parasitic capacitance. Furthermore, this inductor will have a very small voltage drop at rated current compared to the main inductor L_{inv}. The series connection effectively reduces the equivalent capacitance. This is supported by the bode plot shown in Fig. 11 where it is shown that the magnitude of the admittance as seen by the inverter at higher frequencies is less than the single inductor case. It is expected to have a reduced value of peak current spike during every switching instants. However, this also introduces a resonance point at higher frequency which gives rise to sustained oscillations in the inverter current which can not be damped by the damping resistor. This affects the system performance adversely in spite of reducing the current spike. The oscillating current flows through the inverter side inductors as well as through the SiC-devices which causes additional losses. The series inductive elements value is tabulated in Table. III. However, it can be observed that the resonance point is at 342 kHz. At this frequency, it is expected that the current carrying conductors will provide higher AC resistance than at the grid frequency. This will help to damp the inductor current.

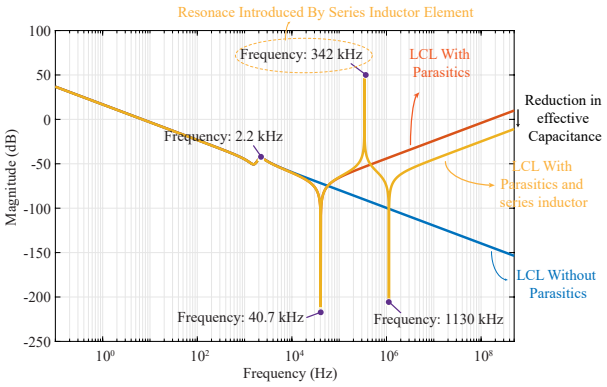


Fig. 11: Bode plot of transfer function between inverter current and voltage ($G(s) = I_{inv}/V_{inv}$) with series connected inductors on the inverter side.

One way to suppress the oscillation caused by this resonance, is to connect a resistor R_{se_d} in parallel with the small series inductor L_{se} as shown in Fig. 12. It might be intuitive that this additional resistor will introduce extra losses in the converter system. However, the loss in this resistor is not too high as the resistor R_{se} only will see the small drop across the small series inductor L_{se}. With the tabulated parameters the bode plot of the transfer function between inverter current and voltage is plotted in Fig. 13. The bode plot clearly suggests that the parallel resistor provides effective damping at the resonance point.

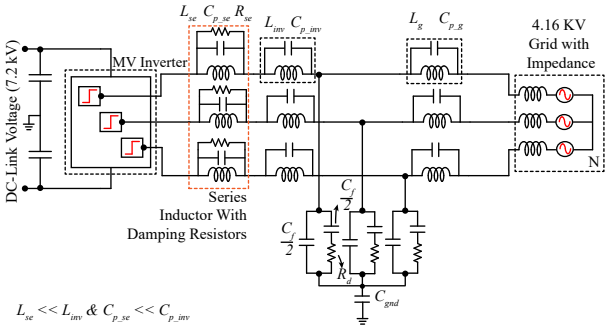


Fig. 12: Schematic of the system showing the introduction of a series inductor with a parallel resistive damping.

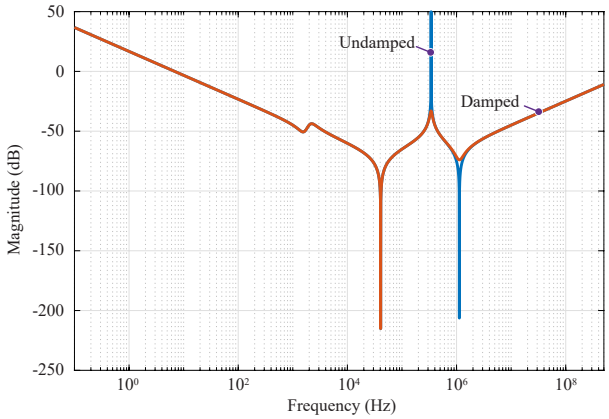
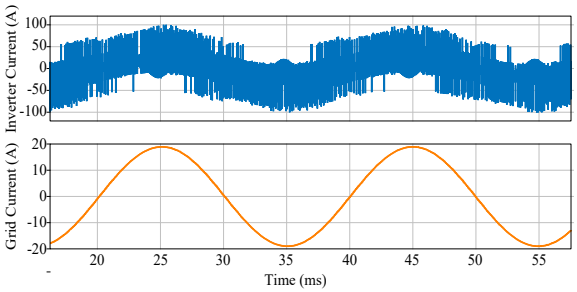


Fig. 13: Bode plot of transfer function between inverter current and voltage ($G(s) = I_{inv}/V_{inv}$) with series connected inductors with and without parallel damping resistance

IV. Simulation Results

With all the tabulated parameters the system is simulated in PLECS [14] to validate the proposed method and the simulation results are provided in this section. Fig. 14a shows the inverter current and grid current when the converter is running at rated conditions with SiC device dv/dt of 100 kV/µs (considering the extreme case). As can be seen the inverter side current does have the current spikes at every switching instant. These current spikes can be as high as 100 A. This causes additional losses in the SiC devices and leads to an increased junction temperature, thus reducing the device lifetime.

The introduction of the additional series inductor is simulated and the current waveforms are shown in Fig. 14b. It is clear that the series inductor helps to reduce the current spikes significantly. A magnified waveform during a switching transient is presented in Fig. 15 which shows the effect of the series inductor. It shows the reduction in peak current due to the high dv/dt experienced by the inductor. It should be noted that the low frequency component (60 Hz) has been



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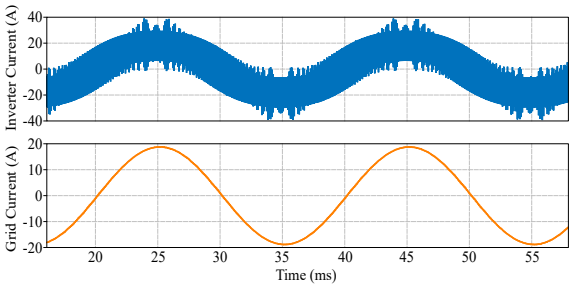

(b)

Fig. 14: Simulation results for inverter Current and grid current at 100 KVA with dv/dt of 100 kV/μS (a) without the additional series inductor (b) with the additional series inductor

filtered to effectively show the difference between both the cases. To demonstrate the damping effect of the R_{se_d}, the inverter current oscillations with the variation in the R_{se_d} in the inverter current is plotted in Fig. 16 (after removing the fundamental grid frequency component). The plot suggests that the lesser the value of the resistance, better is the damping effect. The choice of the value of the resistor can be made by comparing the power loss in all cases. Furthermore, the dv/dt, experienced by the devices also plays a part in the peak current spikes in the inverter current. The effect of variation in dv/dt is depicted in Fig. 17 which shows that with reduction in dv/dt the inverter current peak reduces.

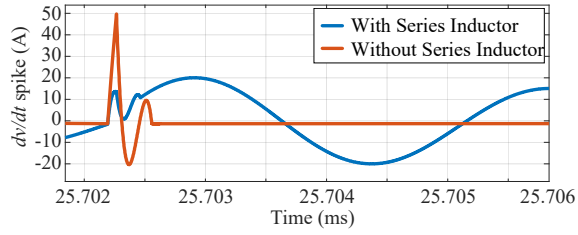

Fig. 15: Current spike during a switching transient with 100 kV/μs dv/dt with and without series inductor with R_{se_d} = 5 kΩ

It is established that the introduction of a parallel resistor with the small series inductor helps in reducing the peak spike in inverter current however at the cost of increased system loss. Therefore, it is important to minimize this resistance loss. The power loss in the resistor is plotted with variation in dv/dt in Fig. 18. It can be seen that the power loss does reduce with the reduction in dv/dt. Furthermore, the loss in not too significant

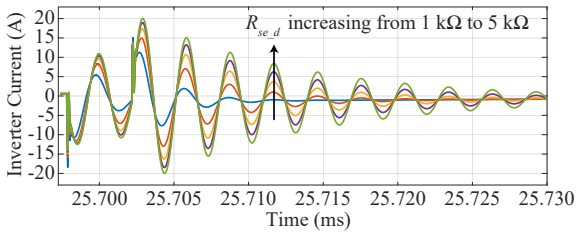

Fig. 16: Increasing damping effect with decrease in R_{se_d} at dv/dt = 100 kV/μSec

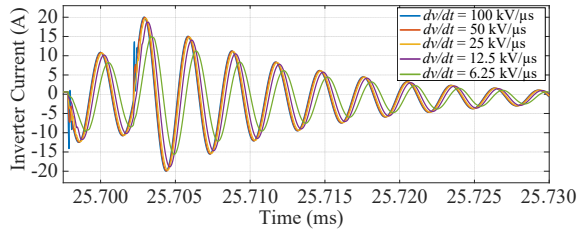

Fig. 17: Peak current variation with dv/dt with R_{se_d} = 5 k Ω

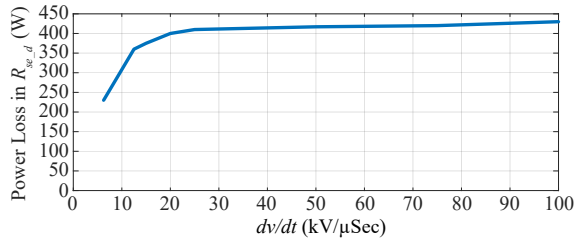

Fig. 18: Power Loss in the series damping resistor with dv/dt with R_{se_d} = 5 kΩ

as the the capacitor voltage does not increase much owing to the small value of the series inductor.

V. Experimental Results

The proposed solution is implemented on hardware for validation. A synchronous buck converter topology is used to validate the concept. A half-bridge 10 kV SiC MOSFET module in XHV-6 package is used as the device and the diode of the buck converter. The buck converter is operated at a 2 kV input voltage and the device is switched at a dv/dt of 10 kV/µs. In order to validate the concept, an additional capacitor is placed in parallel with the main inductor for both the operating modes (with and without the series inductor). Fig. 19 presents the experimental waveforms for both the cases, where inductor currents are captured during SiC-MOSFET turn ON and OFF transients with and without series inductors. The series inductor used for the experiment are toroidal ferrite cores with an external diameter of around 2 inches with five turns wound around it. It can be seen that the introduction of the series inductor reduces the peak current values when the device is switched on. This leads to a reduced turn-on switching loss in the device. It is interesting to note that the peak current during the turn-off transition is also reduced. This reduces the turn-off switching losses in the SiC MOSFET. However, since the turn-on switching losses are much more dominant over the

turn-off switching loss, the overall losses in the SiC MOSFETs can be brought down. Furthermore, in this practical case no oscillations due to the resonance point introduced by the series inductor is observed. This is due to the fact that the resonance point is at very high frequency and at that frequency, the wires used in the system provide high AC resistance to damp the system response.

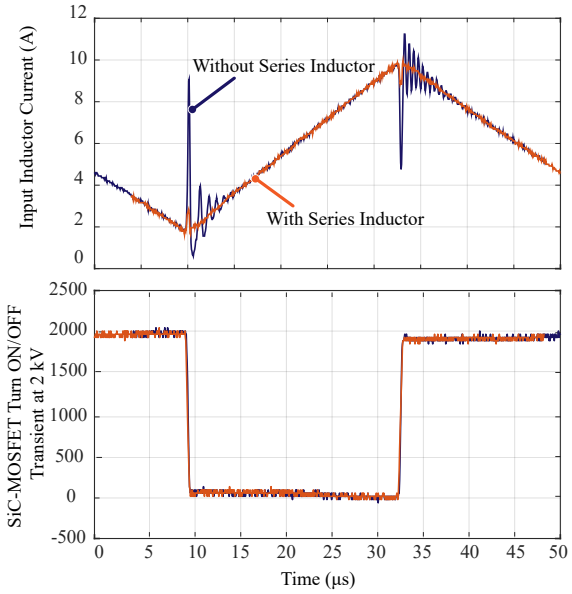

Fig. 19: Experimental inductor currents and SiC-MOSFET Turn ON/OFF Transients at 2 kV dc-link voltage with and without series inductor

VI. Conclusion and Future Work

In this paper, the effect of parasitic capacitance of the filter inductor with high dv/dt occurs in the SiC-power device turn-on and off transients. It is concluded that, compared to L filter, the effects of dv/dt currents in an LCL filter is more pronounced. A suitable method is proposed to increase the impedance offered to the capacitive dv/dt current. An analsysis of the effect of these parasitic capacitance on the SiC MOSFET is also provided. The effectiveness of the proposed method is validated through simulation and experiements. The future work includes optimizing the series inductor and its parasitic capacitance, along with the damping resistor to obtain reduced peak current and lower losses. This method can be helpful for MV converter systems, where the magnetics design can be based on other parameters such as efficiency or power density and the effect of the parasitic capacitance can be taken care of by the additional series inductor.

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