2.8 Gen4 Medium Voltage SST Development

Year 10 Projects and Participants			
Project Number	**Project Title**	**Participants**	**Institution**
Y10ET3	Gen4 Medium Voltage SST Development	Yu, Husain	NCSU

2.8.1 Intellectual Merit and Impact

The overall objective of this project is to furtherly develop a reliable, efficient, cost-effective, compact, and fully functional the fourth generation Solid State Transformers (Gen4 SST) with the bidirectional power flow controllability between 7.2kV MV AC and 400V DC /240 VAC, based on lessons learned from three generations of SSTs developed at FREEDM System Center. As shown in Fig.1, the main challenges for Gen-1 SST are: 1) the system efficiency is unacceptably low (only 88%) because of three-stage power conversion and large switching loss of Silicon IGBT operating at hard-switching. 2) MV AC is only half of the rated voltage (3.6 kV, not 7.2 kV) due to the limited isolation level (only 6 kV) of commercially available auxiliary power supply. By using 10 kV SiC power devices, Gen-2 SST improves the system efficiency to 96%. But Gen-2 SST cannot control the bidirectional power flow because the HV silicon diode is used as rectifier. And Gen-2 SST cannot support 7.2 kV MV AC due to the limited availability of 10 kV SiC devices if the multi-level topology is adopted. In order to realize 7.2 kV AC voltage rating, 15 kV SiC devices are implemented in Gen-3 SST. The system efficiency of Gen-3 SST is improved to 97.5% because the front-end AC-DC PFC rectifier and back-end DC-AC inverter both are eliminated. However, Gen-3 SST has no capability to control the power factor of MV AC grid, and there is no 400 V DC. Moreover, 240 V AC is not controlled in Gen-3 SST because of the fixed frequency operation of the resonant converter.

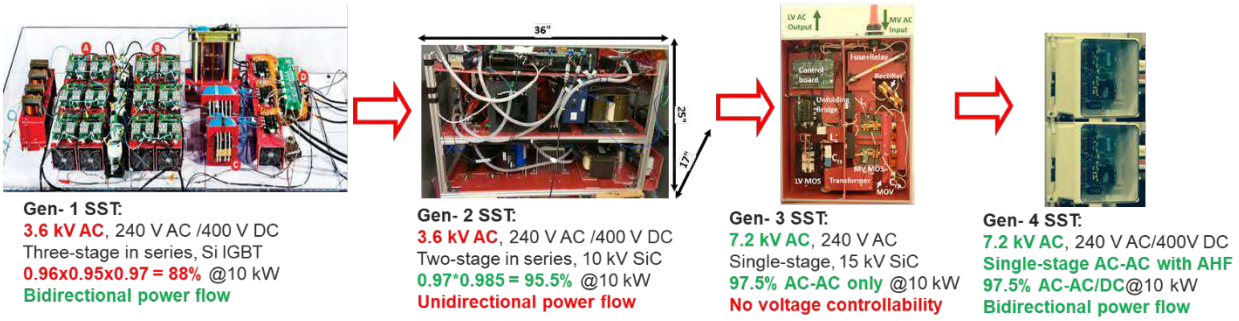


Fig. 1. Four generations of Solid State Transformers at FREEDM System Center.

According to the strategic research roadmap and the lessons learned from the previous nine years, the specific objectives of the Gen- 4 SST project is to reach the rated input voltage 7.2 kV level with the full controllability of MV AC power factor, 400 V DC voltage and 240 V AC voltage regulations, and > 97.5% system level efficiency at the same time. As a key enabling technology, the Gen-4 SST will be delivered as revolutionary energy router between the existing 7.2kV AC distribution system and commonly available 240V AC grid and the future 400V DC microgrid for distributed renewable energy sources (DERE), distributed energy storage devices (DESD) and smart loads. Gen-4 SST will serve as a key node to effectively validate the multi-layer hybrid control robustness and overall system operation reliability of FREEDM System. Moreover, the project of Gen-4 SST is keeping the FREEDM SST to be at the forefront of the global existing development activities.

2.8.2 Technical Approach

2.8.3 Scientific Breakthroughs:

In this project, a methodology of mapping system-level functionalities with architecture of SST is proposed to explore the critical impact of system-level functionalities on the architecture of Gen-4 SST. Fig. 2 shows that the system-level functionalities of SST include fault management, power management and energy management between medium voltage grid and renewables, distributed energy storage, EV, and DC or AC loads. SST can manage and optimize bi-directional power/energy flow with local autonomous control and / or distributed intelligence through communications. As a result, a modular direct AC-AC topology in parallel with an active filter is identified as the optimized system architecture for Gen-4 SST to effectively address the key challenges of high efficiency, modularized design, high voltage isolation, reliability, protection, grounding, packing and cooling.

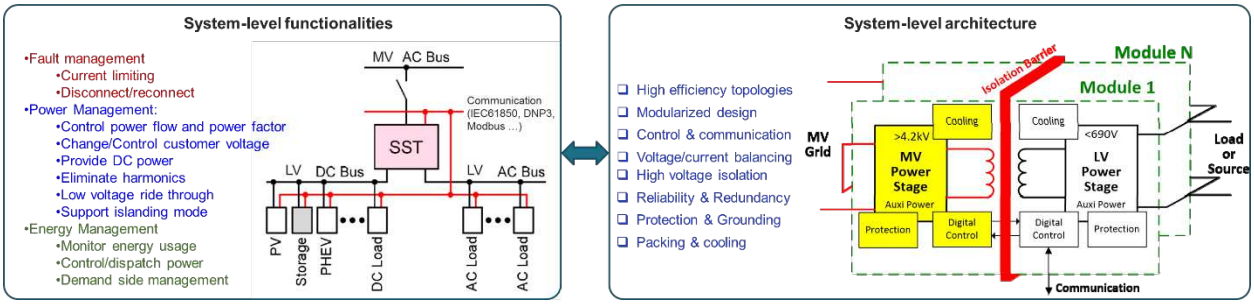
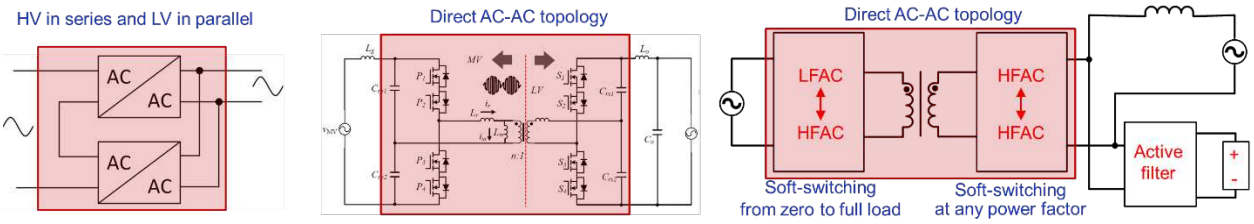


Fig. 2. Proposed methodology of mapping system-level functionalities with system-level architecture of SST.

2.8.4 Technology Innovations:

2.8.4.1 Direct AC-AC and active harmonic filter based Gen-4 SST system architecture:

Modularized design is adopted in Gen-4 SST system architecture to use the commercially available HV power semiconductor by connecting multiple AC-AC cells at HV-side in series and LV-side in parallel, as shown in Fig. 3. Novel modulation method is verified to realize the full-range of soft-switching from zero to full load and under any power factor conditions. The designed AC-AC topology is capable of controlling the voltage of the low voltage AC port. Instead of employing a direct bidirectional switches, it is also possible to first place a folding/unfolding stage to eliminate the commutation risk of the bidirectional switches. The active harmonic filter not only eliminates the second and higher order harmonics injecting to grid, but also controls the bidirectional power flow and regulate the voltage of the low voltage DC port.

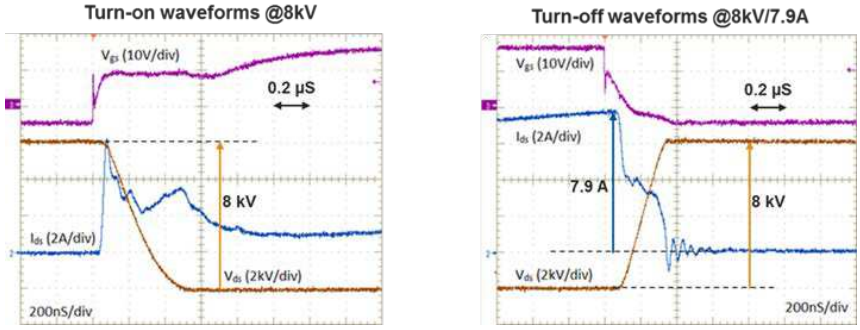


(a) (b) (c)

Fig. 3. Gen-4 SST system architecture. (a) Modular cells connected at HV side in series and LV side in parallel. (b) Direct AC-AC topology using the bidirectional switches. (c) Integration of soft-switching direct AC-AC topology with active harmonic filter.

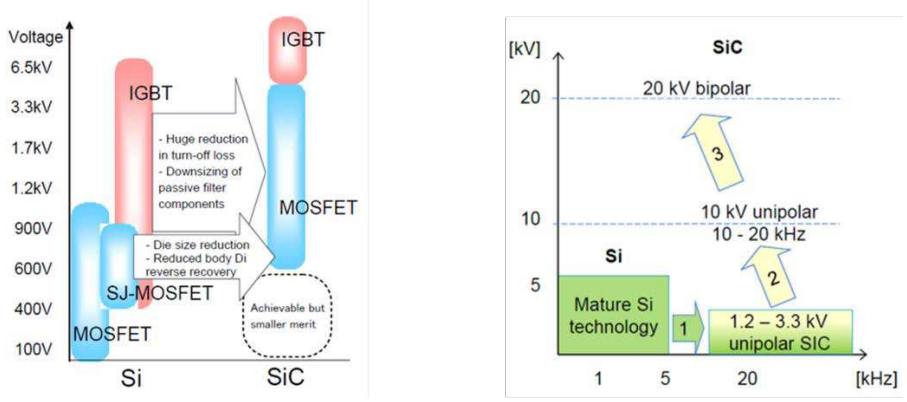
2.8.4.2 HV power semiconductor under different operating conditions:

Fig. 4 shows detailed switching waveforms of 10 kV SiC MOSFET operates at high voltage (8 kV). The rising is 0.8µs and the falling time is 0.3 µs. It verified that SiC 10 kV MOSFET can operate under high voltage at hard-switching and high switching frequency conditions. Based on the experimental results shown in Fig. 4, the switching losses can be evaluated by sweeping gate resistance, DC link voltage and semiconductor current, Fig.5 illustrates the HV power semiconductor voltage rating and associated switching frequency of Silicon and SiC MOSFETs, Silicon and SiC IGBT semiconductors under the normal hard-switching operation. In this project, HV silicon IGBT operating under the full range of soft-switching conditions will be also included as one of the suitable candidates for power semiconductors in Gen-4 SST.



(a) (b)

Fig. 4. Detailed switching waveforms of 10 kV SiC MOSFET operates at high voltage (8 kV) and hard-switching. (a) Turn on transition and (b) turn off transition of gate voltage (purple), drain-to-source voltage (yellow), and device current (blue).

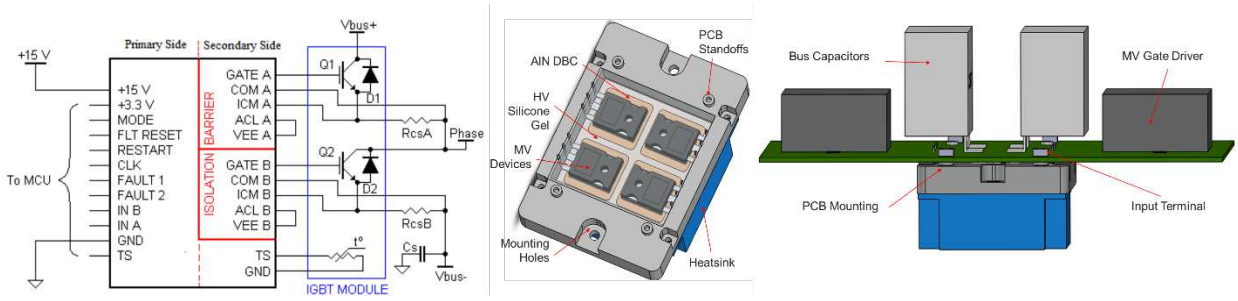


(a) (b)

Fig. 5. HV power semiconductor selection of Gen-4 SST. (a) Voltage rating of Silicon and SiC power devices. (b) Voltage rating and the associated switching frequency at normal hard-switching frequency.

2.8.4.3 Customized MV power module with robust short-circuit protection:

The ruggedness is the most important design consideration of the customized MV power module. The module is fabricated using 40mil AIN Direct Bonded Copper (DBC) as the substrate of the module for heat transfer and high voltage isolation. TO 247 MV devices are soldered using Sn63/Pb37 solder paste. Case is 3D printed using polylactic acid (PLA). The module is encapsulated with SEMICOSIL 915HT high temperature silicone gel to provide high voltage isolation at high temperature.

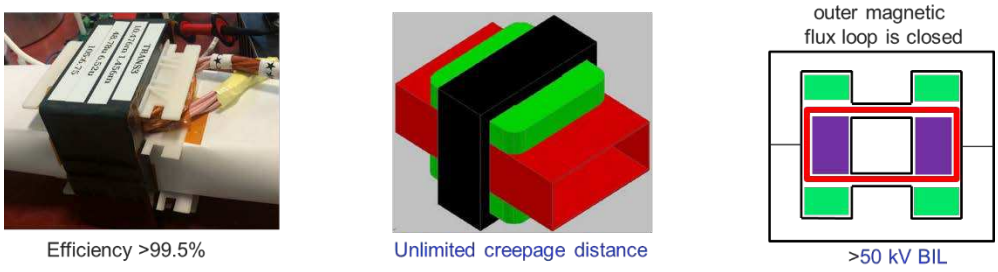


(a) (b) (c)

Fig. 6. Customized MV power module with robust short-circuit protection. (a) Gate driver with isolated local robust overcurrent protection using shunt resistors. (b) MV devices with high voltage isolation using AlN DBC and high temperature silicone gel. (c) MV power module mounted with bus capacitors, MV gate drivers and heatsink.

2.8.4.4 High-voltage isolated transformer integrating wireless power transfer with closed magnetic loop

Designing a compact and high efficiency transformer is very critical while realizing >50 kV basic insulation level (BIL) high voltage isolation. As shown in Fig.7, the proposed transformer has a prefabricated isolation box which breaks through the center branch of the magnetic core. This innovative technology significantly improves the state of the art in how to achieve the high-voltage isolation and greatly simplify the manufacturing process. From isolation point of view, the proposed approach achieves 50 kV basic insulation level because of wireless power transfer. From energy efficiency point view, it demonstrated >99.5% transformer efficiency at 40kHz or higher operation frequency thanks to better window area utilization of magnetic core while eliminating EMI issue because that the outer magnetic flux loop is closed.



(a) (b) (c)

Fig. 7. Innovative transformer integrating wireless power transfer with closed magnetic loop. (a) Photo of the proposed high efficiency and high isolation voltage transformer prototype. (b) Three-dimension drawing with unlimited creepage distance. (c) Cross-section drawing with the closed outer magnetic flux loop.

2.8.4.5 High speed control of active harmonic filter:

The active harmonic filter (AHF) includes commercially available SiC power module, heatsink, grid-side inductor, DC-link capacitor, bus bar, gate driver, sensor and FPGA-based digital controller, which is holistically integrated in the mechanical, thermal, electrical, and electronic multi-physics perspectives to meet the efficiency, power density, and control bandwidth requirements. Fig. 8 describes the control block diagram of active harmonic filter with enhanced control bandwidth by the interleaved SiC power stage and FPGA-based PI plus repetitive compensator in d-q frame.

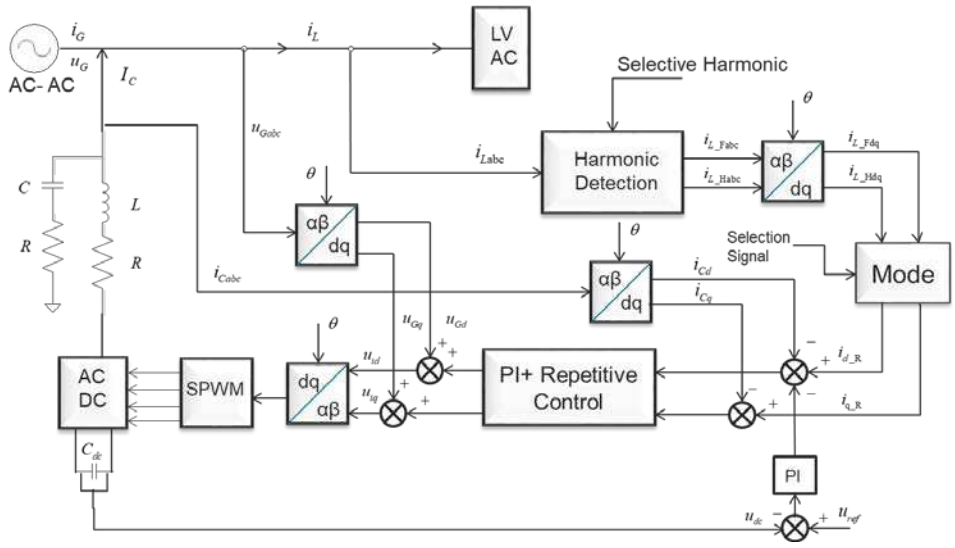


Fig. 8. Control block diagram of active harmonic filter with enhanced control bandwidth by the interleaved SiC power stage and FPGA-based PI plus repetitive compensator in d-q frame.

The harmonics detection for active harmonic filter using Recursive Discrete Fourier Transform (RDFT) and its implementation in z-domain is presented in Fig. 9.

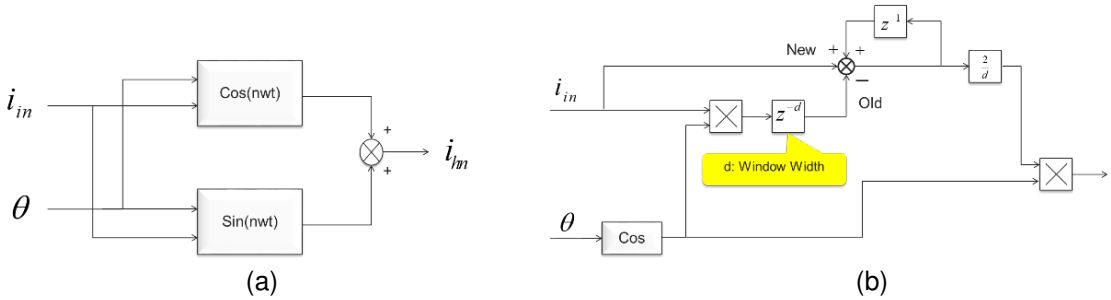


Fig. 9. The harmonics detection for active harmonic filter. (a) Control block diagram of recursive discrete Fourier transform. (b) z-domain implementation of recursive discrete Fourier transform.