Estimation and Minimization of Power Loop Inductance in 135 kW SiC Traction Inverter

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***Abstract*—The paper discusses the estimation and minimization of commutation loop inductance for a printed circuit board (PCB) busbar based 135 kW SiC inverter with a 1 kV DC link using finite element analysis (FEA) simulations. For the inductance estimation of the power module (Wolfspeed: HT-3231-R), PCB busbar, and customized interconnects constituting the commutation loop have been modelled accurately in Ansys Q3D Extractor. Based on the simulation results, subsequent modification to the original PCB busbar design has been proposed to lower the loop inductance. FEA simulation results have resulted in an optimized PCB busbar with lower commutation loop inductance, thereby limiting the device voltage spike well below its rated value. Loop inductance results from the Q3D simulation have been validated through double pulse tests (DPT) and the performance improvements achieved therefore have been highlighted.**

Keywords—SiC inverter; commutation loop inductance; FEA simulations; parasitic inductances; PCB busbar; busbar design.

I. INTRODUCTION

With increasing penetration of wide band-gap devices, the research focus on high power density power electronics is to ensure high performance and reliability in traction applications [1]. To realize high power density, wide band-gap devices are generally operated at higher frequencies [2]. Under fast switching conditions, the impact of high di/dt on the parasitic inductances cannot be ignored, especially in multichip high-power modules (MCPM) [3, 4]. The commutation loop parasitic inductance in inverters determine the voltage spike across the devices. Higher loop inductance leads to large voltage spikes during turn-off and may lead to device breakdown [5]. An accurate estimate of the commutation loop inductance is thereby vital to improve the switching performance and ensure safe and reliable operation. Taking this into account, this paper discusses the extraction of the parasitic commutation loop inductances of a 135 kW PCB busbar based SiC traction inverter.

Traditionally, copper-based laminated busbars have been the go-to solution to ensure high efficiency and safe operation [6] in traction applications and the operating frequency was generally limited to 10-20 kHz. With an increased operating frequency, busbar design is crucial since the system performance, safety, efficiency, and electromagnetic emissions etc. are heavily influenced by the busbar architecture and parasitic components [7-9]. With increase in demand for high power density power converters, busbar form-factor and interconnection with power modules play significant roles in the overall system-level design. Printed circuit board (PCB)-based busbars are better alternatives to copper-based laminated busbars owing to ease of design, manufacturability, and simplified system assembly [9].

This paper illustrates the modelling of the various components that constitute the commutation loop in an inverter using finite element analysis (FEA) [10]. Thus, the MCPM, PCB busbar and the module to PCB interconnect have been modelled in Ansys Q3D Extractor to obtain a lumped commutation loop inductance value. The busbar design is centered around the Wolfspeed 1.7 kV, 7.5 mΩ high performance SiC half-bridge power module (SKU: HT-3231-R). The designed PCB busbar encompasses the interconnection of the power modules, as well as the capacitors and the power connectors.

The organization of the paper is as follows: In Section II, the stray inductance model of the MCPM, interconnects and an initial PCB busbar design, henceforth called busbar-A, have been derived followed by the extraction of the commutation loop inductance of the inverter using busbar-A. Section III discusses improvements that can be made to busbar-A for commutation loop inductance reduction. Section IV presents double pulse test results highlighting the reduction in voltage overshoot that can be obtained with busbar-A and the improved version busbar-B. Finally, in Section V, the developed 135 kW EV inverter is compared to 81.8 kW Wolfspeed traction inverter to highlight the high-power density achieved by the former without compromising on the high frequency performance.

II. STRAY INDUCTANCE MODEL OF THE VARIOUS COMPONENTS OF POWER LOOP

This Section discusses the extraction of stray inductance of the different components that constitute the commutation loop in the inverter. The commutation loop inductance in an inverter includes the inductance of the 1.7 kV SiC module, inductance contributed by the PCB busbar between the DC+ and and DC- terminals and the inductance of the module to PCB interconnect. These inductances have been extracted

The first two authors contributed equally to this work. * denotes the equal contribution made by the authors.

using FEA and a simple model of each component has been provided.

A. Modelling of the SiC Module

The 1.7 kV module (HT-3231-R) shares the same low inductance package as that of the 1.2 kV version (CAS325M12HM2). The latter was opened to expose the internal architecture and parameters such as dimensions and spacing of the direct bonded copper (DBC), dimensions of the terminals, etc. were extracted from the exposed 1.2 kV module shown in Fig. 1. The die positions in the 1.7 kV module, wire bond dimensions, etc. were obtained through micro-CT. With these details, the 1.7 kV module was modelled in Ansys Q3D extractor for the estimation of the stray inductances. Distribution of 150 A in the commercially available 1.2 kV module is shown in Fig. 2. The Q3D model and the current distribution in the 1.7 kV module is similar to that of the 1.2 kV module in Fig. 2.

The inductance and resistance values extracted from Ansys Q3D Extractor are tabulated in Table I. The correpsonding equivalent circuit of the commutation loop is shown in Fig. 3. The inductance offered by the module between the DC+ and the DC- terminals can be estimated using (1). The estimated module inductance (L_{module}) between the DC+ and the DC- terminals is 10.48 nH at 10 MHz.

$$L_{module} = L_1 + L_2 + L_3 + 2\times\left(M_{12} + M_{23} + M_{13}\right) \quad (1)$$

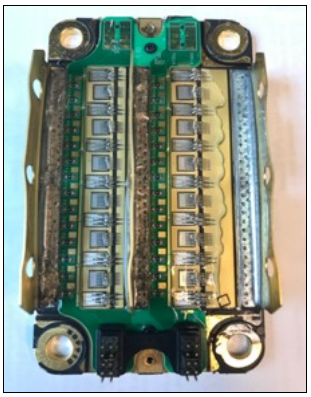


Fig. 1. Internal layout of the 1.2 kV module.

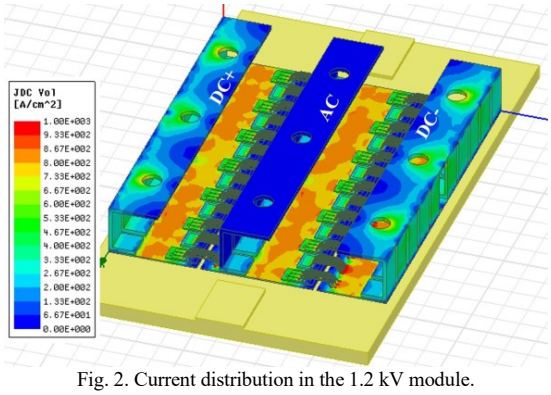


Fig. 2. Current distribution in the 1.2 kV module.

B. Modelling of the PCB Busbar-A and the Interconnects

The design of the busbar PCB is centered around the 1.7 kV module which shares the same package as that of the 1.2 kV SiC module. In these modules, the AC terminal lies between the DC+ and DC- terminals. This geometry poses difficulties in realizing low commutation loop inductance busbar design while maintaining the required voltage isolation between terminals.

To utilize the low inductance module effectively, and to minimize the commutation loop inductance, customized heavy duty connectors with current handling capability of 150 A, shown in Fig. 4, were designed using Solidworks and later fabricated. The interconnects allow the power module to be electrically and mechanically connected to the high voltage busbar with minimal added parasitic inductance to the commutation loop. Additionally, these interconnects offset the busbar several millimeters from the top of the module, allowing an extra set of small ceramic capacitors to be placed on the bottom side of the busbar.

The PCB busbars designed for the 135 kW SiC inverter with a 1 kV DC link is shown in Fig. 5, has two stages of capacitors for enhanced high-frequency performance. The two capacitor stages result in two parallel loops between the DC+ and the DC- terminal in the busbar as shown in Fig. 5. The two stages of capacitors are described below:

1st-stage - Bulk DC-link capacitors for energy buffer or voltage stabilization. Two 27 µF capacitors were distributed for each module (ESL = 15 nH, resonant frequency = 250 kHz). The DC-link capacitors constitute the current path named busbar-A1 in Fig. 5.

TABLE I. ESTIMATED STRAY INDUCTANCES OF THE MODULE

	DC inductance		*Inductance and resistance at 10 MHz*	
	L_{dc} (nH)	R_{dc} (mΩ)	L_{ac} (nH)	R_{ac} (mΩ)
L_1, R_1	2.22	0.019	1.77	1.77
L_2, R_2	3.68	0.025	3.03	0.39
L_3, R_3	1.51	0.017	1.21	0.31
M_{12}, R_{12}	1.24	0	0.91	0.91
M_{23}, R_{23}	0.93	0	0.69	0.07
M_{13}, R_{13}	0.25	0	0.18	0.18

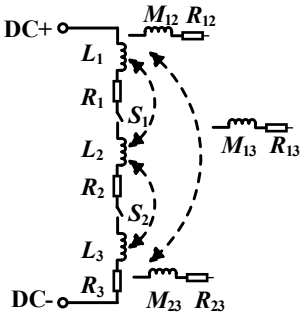
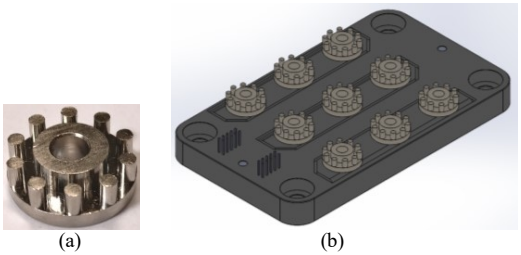


Fig. 3. Equiavelnt circuit representing the stray inductances in the module between the DC+ and DC- terminal.



(a) (b)

Fig. 4. Module to busbar interconnect and (b) the connectors on the module.

2nd stage - Ceramic capacitors were distributed near the power modules on both sides of the board to reduce the device's voltage overshoot. These snubber capacitors constitute the current path busbar-A2 and result in a localized commutation loop in the inverter as evident from Fig. 5.

Efficacy of the snubber capacitors in reducing voltage overshoot is dependent on their placement with respect to the DC+ and DC- terminals of the module. The initial busbar design has capacitors placed around the module as shown in Fig. 5(a). Busbar-A and the interconnects were modelled and analyzed in Q3D Extractor. The inductances extracted from busbar-A and the equivalent circuit of the busbar with the stray inductances is shown in Fig. 5(a) and 5(b) respectively. In Fig. 5(b), L_{cable} denotes the inductances of the power cables used to connect the terminals of the busbar to the DC voltage source.

From Fig. 5, it is evident that $L_{busbar\text{-}A1}$ is made up of L_3, L_5 and the ESL of the DC link capacitors. As shown in Table-II, the addition of the distributed ceramic capacitors resulted in the localized current path-2 with $L_{busbar\text{-}A2} < L_{busbar\text{-}A1}$. Reduction in the stray inductance contributed by the busbar to the commutation loop inductance significantly reduces the overshoot voltage across the devices. The current distribution in the two loops is shown in Fig. 6.

C. *Commutation Loop Inductance of the Inverter with Busbar-A*

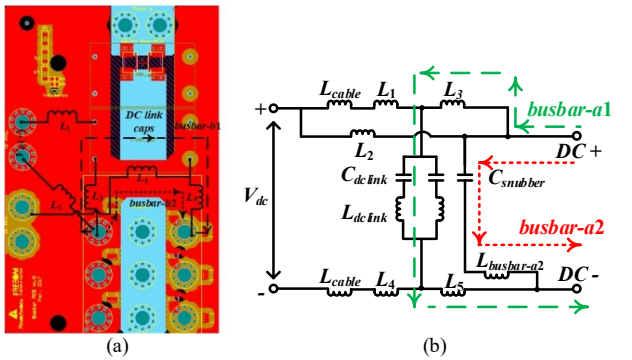
Distributed snubber capacitors were placed around the PCB with the intention of reducing the localized parasitic loop inductance. Additionally, the current path in busbar-A causes mutual inductance cancellation between the busbar and module. The bridge, shown in Fig. 7, connects the DC+ and the DC- terminals in the busbar also acts as the return path for the current. Though the bridge in the busbar-A does not completely overlap with the module as seen in Fig. 7, the opposing currents in the bridge and the module lead to flux cancellation, thereby reducing the inverter's localized commutation loop inductance. The inductance of the localized commutation loop formed by the ceramic capacitors is therefore given by (2):

$$L_{CCL-A} = L_{module} + L_{busbar-A2} - 2M_A \tag{2}$$

where M_A is the mutual inductance between the module and the PCB busbar-A. This cancellation effect is negligible with the DC-link capacitors due to their distance from the module. The inductance matrix computed from Q3D at 10 MHz is given by (3):

$$\begin{bmatrix} L_{module} & M_A \\ M_A & L_{busbar-A2} \end{bmatrix} = \begin{bmatrix} 10.46nH & 2.25nH \\ 2.25nH & 19.93nH \end{bmatrix} \tag{3}$$

With mutual inductance cancellation, the inductance of the localized commutation loop i.e., $L_{CCL\text{-}A}$ was estimated to be 25.84 nH at 10 MHz. The curernt distribution in the localized commutation loop of the 135 kW inverter with busbar-A is shown in Fig. 8. Mutual inductance cancellation has been approximated in simulation by subtracting the $L_{busbar\text{-}A2}$ of the PCB busbar with the mutual indutance estimate such that the overall inductance of the commutation loop remains the same as $L_{CCL\text{-}A}$.



(a) (b)

Fig. 5. (a) PCB busbar-A of the 135 kW SiC inverter with 1 kV DC-link and (b) equivalent circuit of the PCB busbar-A.

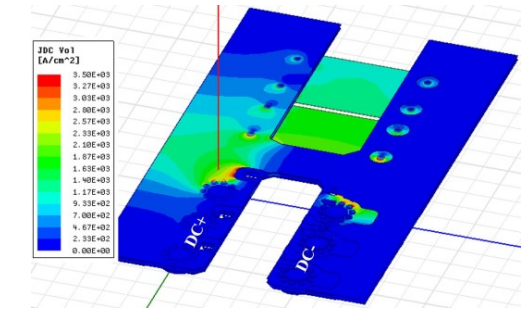
TABLE II. ESTIMATED STRAY INDUCTANCES OF THE BUSBAR-A

	DC inductance		*Inductance and resistance at 10 MHz*	
	L_{dc} (nH)	R_{dc} (mΩ)	L_{ac} (nH)	R_{ac} (mΩ)
L_1, R_1	5.76	0.03	4.05	2.42
L_2, R_2	18.40	0.14	12.50	5.79
L_3, R_3	16.20	0.09	7.44	7.45
L_4, R_4	42.06	0.46	29.43	7.36
L_5, R_5	14.57	0.10	9.85	4.02
$L_{busbar\text{-}A1}$, $R_{busbar\text{-}A1}$	48.05	0.31	20.93	13.10
$L_{busbar\text{-}A2}$, $R_{busbar\text{-}A2}$	35.49	0.15	19.93	8.60

III. OPTIMIZATION OF BUSBAR DESIGN FOR MINIMIZING COMMUTATION LOOP INDUCTANCE

A. *Modelling of the PCB Busbar-B*

The customized heavy duty connectors used to connect the module to the PCB busbar provide an opportunity to further reduce the localized commutation loop inductance. Because each connector can safely conduct 150 A and the power modules will draw less than 150 A at maximum power output, the connectors in the middle can be removed. As shown in Fig. 9, the additional space was bridged in the new design, "busbar-B", to reduce the length of the conduction path. The localized snubber capacitors were distributed on either side of the aforementioned bridge.



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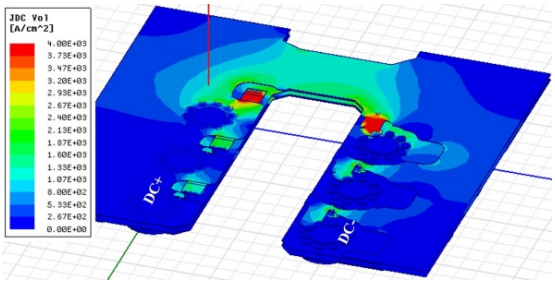


(b)

Fig. 6. (a) Current distribution in path involving the DC link capacitors (*path*-1) in the busbar PCB and (c) current distribution path involving the snubbers capacitors (*path*-2) in busbar PCB.

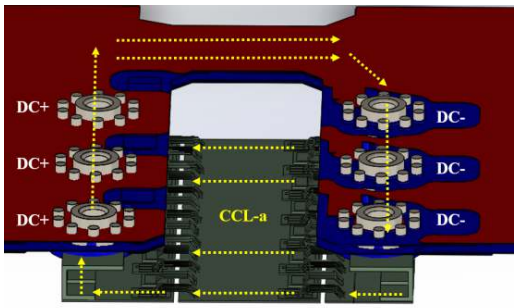


Fig. 7. 3D model of showing the commutation loop (CCL-A) with busbar-A.

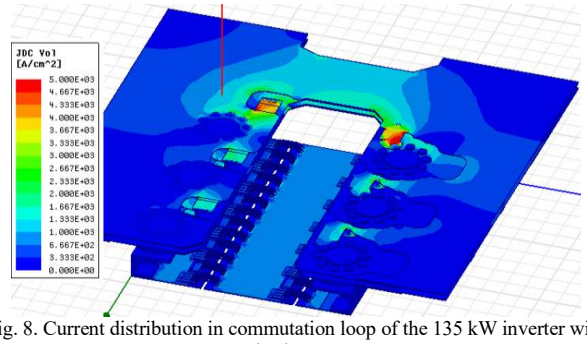


Fig. 8. Current distribution in commutation loop of the 135 kW inverter with busbar-A.

Busbar-B with its stray inductances and corresponding equivalent circuit is shown in Fig. 9. Because modifications were made only to the placement of the snubber capacitors and the bridged area, the equivalent circuit of busbar-B and the current path for the DC-link capacitors are similar to busbar-A. It is to be noted that, $L_{busbar\text{-}B2} < L_{busbar\text{-}A2}$, due to a decrease in length of the current path owing to change in snubber capacitor placement. $L_{busbar\text{-}B2}$ was estimated to be 10.2 nH at 10 MHz from Q3D simulations. The current distribution in busbar-B is shown in Fig. 11 and it is clear the majority of the current flows through the modified bridge area. It can be observed from Fig. 11 the current distribution between the ceramic capacitors is more uniform with busbar-B than busbar-A. With a uniform current distribution, capacitor failure becomes less probable leading to a more reliable design.

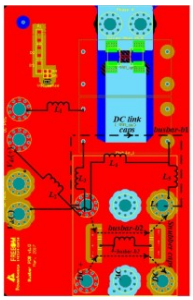
B. Commutation Loop Inductance of the Inverter with Busbar-B

It can be seen from Fig. 10 the mutual inductance cancellation becomes significant as the current path in the busbar-B now exactly overlaps with the current path in the module. By utilizing the mutual inductance cancellation and uniform current sharing between module terminals, more than 50% reduction in commutation loop can be easily achieved.

When compared to CCL-A in Fig. 7, there is significantly more overlap in current paths leading to increased mutual flux cancellation. The commutation loop inductance in this case is given as:

$$L_{CCL-B} = L_{module} + L_{busbar-B2} - 2M_B \tag{4}$$

where M_B is the mutual inductance between the module and the busbar-B.



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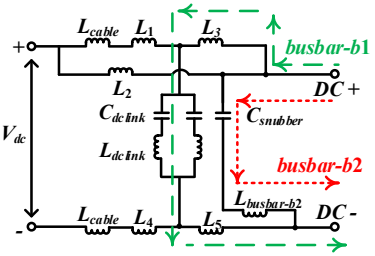


(b)

Fig. 9. (a) PCB busbar-B of the 135 kW SiC inverter with 1 kV DC-link and (b) equivalent circuit of the PCB busbar-B.

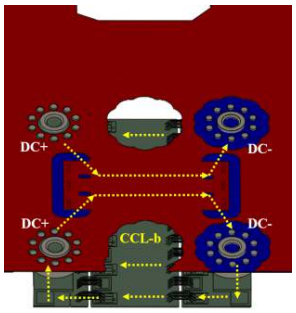


Fig. 10. 3D model of showing the commutation loop (CCL-B) with busbar-B with increased mutual inductance cancellation.

The inductance matrix computed from Q3D at 10 MHz is given by (5)

$$\begin{bmatrix} L_{module} & M_B \\ M_B & L_{busbar-B2} \end{bmatrix} = \begin{bmatrix} 10.46nH & 3.63nH \\ 3.63nH & 7.00nH \end{bmatrix} \tag{5}$$

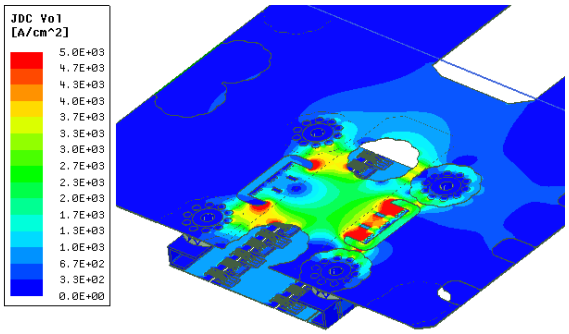


Fig. 11. Current distribution of in the commutation loop with busbar-B.

TABLE III. COMPARISON OF LOOP INDUCTANCE WITH SNUBBER CAPACITORS

Inductance	Busbar-A	Busbar-B
CCL	25.84 nH	10.2 nH
Busbar	19.93 nH	7.00 nH
Mutual, *M*	2.25 nH	3.63 nH

With mutual inductance cancellation, the inductance of the localized commutation loop i.e., $L_{CCL\text{-}B}$ was estimated to be 10.2 nH at 10 MHz. Comparison between the matrices in (3) and (5) shows that significant improvements in the parasitic loop inductance was achieved by reducing the commutation path length, and increasing mutual inductance cancellation.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To characterize the switching behaviour of the SiC inverter and measure the overvoltage seen by the devices, a standard double pulse test (DPT) was performed at 240 A peak current (worst case scenario). The test-setup included the 1.7 kV SiC modules and the PCB busbar-A is shown in Fig. 12. The overvoltage seen by the low side device of the half bridge SiC module was estimated using DPT.

The DPT results obtained with turn-on and turn-off R_g of 1.2 Ω and 1.2 Ω are shown in Fig. 13. From Fig. 13, it is evident at the end of the first pulse, the inductor current reaches a peak of 240 A and the turn-off switching characteristics are obtained by measuring the waveforms. After the device has been turned-off, the inductor current free-wheels through the anti-parallel diode of the high side switch. The second pulse is then used to characterize the turn-on behavior of the switching devices in the SiC inverter. The di/dt was measured to be 8 kA/µs.

The DPT validates the high-frequency behavior owing to the addition of the localized ceramic capacitor in busbar-A. Without the ceramic capacitors, the commutation loop inductance is higher leading to 26% overvoltage across the low-side device as seen in Fig. 13(a). With addition of the ceramic capacitors, the device overshoot is reduced to 19% as shown in Fig. 13(b). This can be attributed to the localized commutation loop with reduced parasitic inductances. Table IV summarizes these results. The approximate voltage overshoot to be expected from busbar-B can be computed using (6).

$$\Delta V_{ds} = L_{CCL-B}\frac{\Delta i_d}{\Delta t} \tag{6}$$

With $\Delta i_d/\Delta t$ of 8 kA/µs, the voltage overshoot of the improved busbar-B design can be estimated to be 104 V, potentially a 45% reduction in overvoltage spike compared to busbar-A.

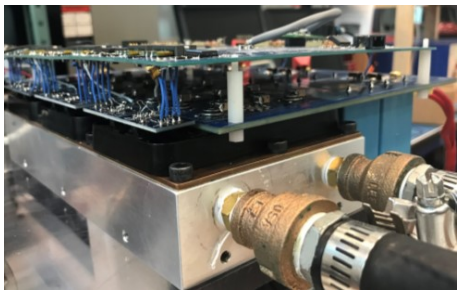
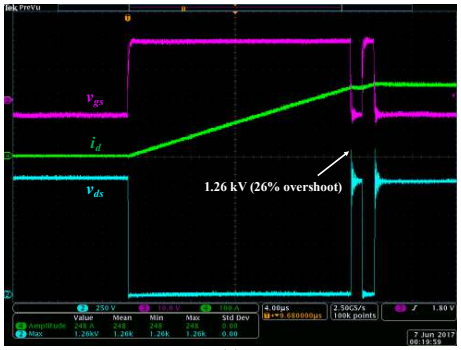


Fig. 12. Double pulse test setup.



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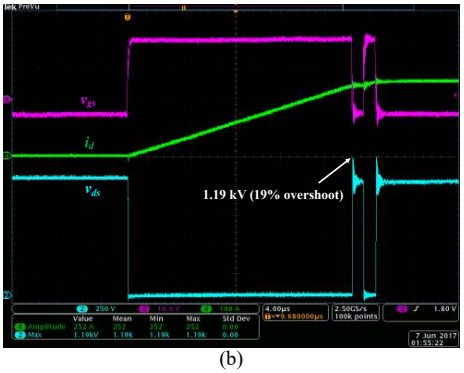


(b)

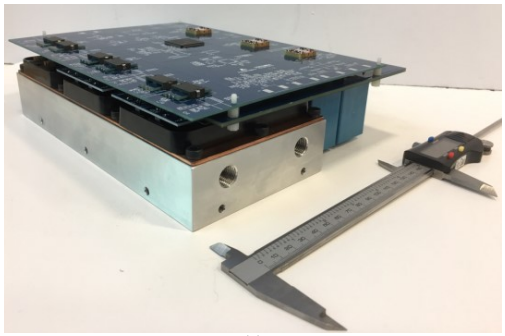
Fig. 13. (a) DPT results with only DC-link capacitors with 240 A peak current and (b) DPT results with localized capacitors with 240 A peak current

TABLE IV. COMPARISON OF LOOP INDUCTANCE WITH SNUBBER CAPACITORS

Parameter	DC-link capacitor	Snubber capacitor
Overshoot (%)	26	19
Falling edge (ns, kV/µs)	32.0 24.4	34.0 23.5
Rising edge (ns, KV/µs)	21.2 37.7	21.0 38.1

V. INVERTER COMPARISON

The 135 kW SiC inverter shown in Fig. 14(a) is compared with the 81.8 kW Wolfspeed traction inverter [11] as they employ modules with the same package. The Wolfspeed inverter in Fig. 14(b) utilizes the 1.2 kV CAS325MHI12 modules, a laminated Cu-busbar structure for power interconnects, and DC-link capacitors while multiple PCB's are used for the gate driver and local snubber capacitor mounting. Thus, the overall busbar and associated capacitors have a segmented architecture, yielding a power density of 18.6 kW/L. In case of the 135 kW SiC inverter using the 1.7 kV HT-3231-R SiC modules, the customized heavy-duty connectors facilitated in realizing a high power density inverter by permitting a stacked architecture. The proposed PCB-based busbar offers a streamlined solution for all the power interconnects and capacitors while promising a low commutation loop inductance. A power density of 35 kW/L was achieved using the 135 kW SiC inverter and planarized busbar design.



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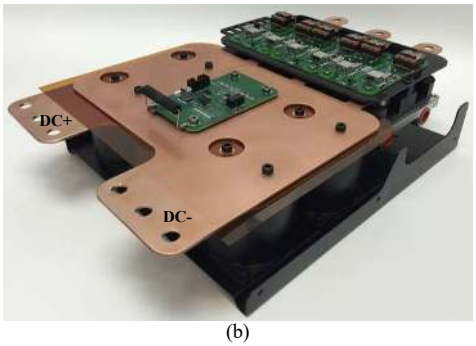

(b)

Fig. 14. (a) Prototype of the 135 kW SiC traction inverter and (b) Prototype of the 81.8 kW Wolfspeed SiC traction inverter [12].

VI. CONCLUSION

The design of a 135 kW SiC inverter with low parasitic inductance profile using PCB-based busbar and customized heavy duty connectors has been discussed in this paper. The inductance contributed by the module, busbar, and interconnects to the commutation loop has been studied in depth as it is designed to be operated at high switching frequencies. Based on the analysis, an improved PCB design with very low commutation loop inductance has also been proposed by removing three pieces of connectors in the middle of the SiC power module. Minimizing the parasitic loop inductance of the PCB busbar leads to lower overvoltage spikes due to large di/dt. The switching behavior of the inverter with the estimated inductances has been validated through simulation and experimentation. The performance benefits obtained from the 135 kW inverter with its small loop inductance due to the PCB busbar has been highlighted. The solution is compared with the Wolfspeed prototype for constructional complexity.

ACKNOWLEDGMENTS

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