PCB Busbar Optimization for a 135 kW SiC Inverter

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Overview

- Develop a framework for analytical, simulation-based, and experimental evaluation of parasitic loop inductance in a PCB busbar for a 135 kW SiC EV inverter.
- Use Ansys Q3D to extract parasitic inductance to evaluate busbar design
- Use impedance analyzer and DPT to directly measure loop inductance to validate design and show improvement in system operation.

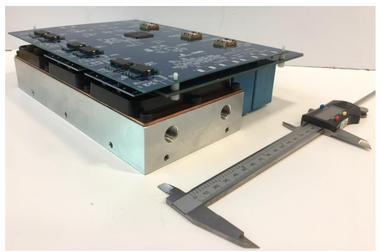


Fig. 1: 135 kW EV Inverter with PCB Busbar

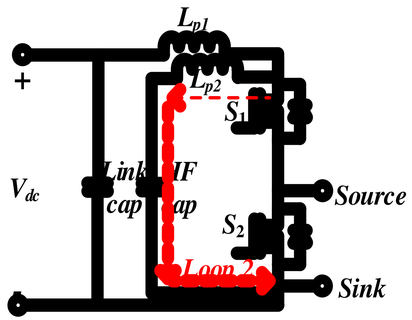
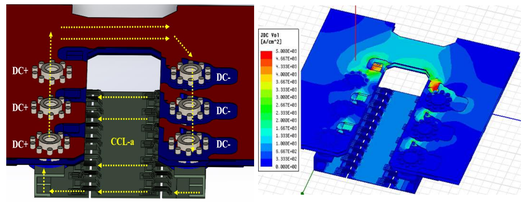


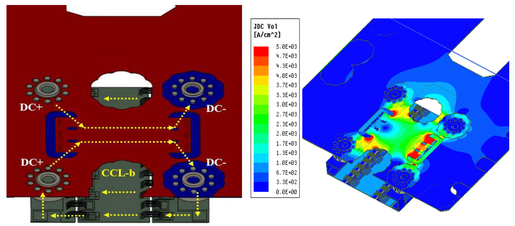
Fig. 2: Current commutation loop

Method



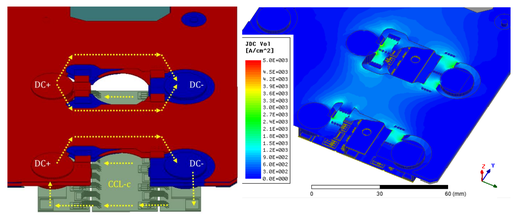
(a) **(b)**

Fig. 3. (a) 3D model of the current commutation loop with busbar - A and (b) current distribution in busbar – A.



(a) **(b)**

Fig. 4. (a) 3D model of the current commutation loop with busbar - B and (b) current distribution in busbar – B.



(a) **(b)**

Fig. 5. (a) 3D model of the current commutation loop with busbar - C and (b) current distribution in busbar – C.

Results

$$L_{CCL} = L_{busbar} + L_{module} - 2M$$

	Busbar A	Busbar B	Busbar C
Total Loop Inductance	12.8 nH	7.00 nH	**7.4 nH**
Busbar Self-Inductance	10.4 nH	5.4 nH	**5.6 nH**
Mutual Inductance	4.0 nH	4.4 nH	**4.3 nH**
DPT Voltage Spike @ 440 A	183 V	-	**163 V**

Fig. 6: Comparison of PCB busbar designs

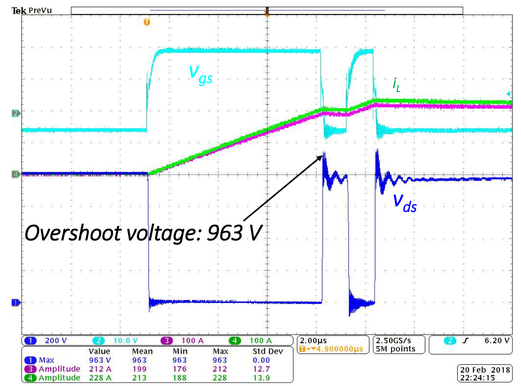


Fig. 7: Busbar-C DPT Results @ 800 V, 440 A

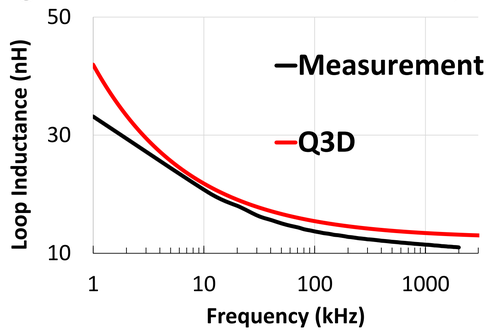
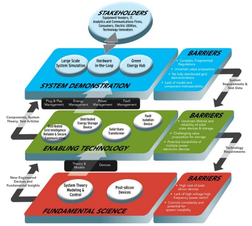


Fig. 8: Initial impedance measurement results for Busbar-A

Conclusions & Future Work

- Decoupling capacitor placement is critical in minimizing loop inductance, resulting in lower turn-off voltage spike and higher reliability.
- Busbar-C is will result in a more reliable system than Busbar-A with lower voltage spikes and more uniform decoupling capacitor current distribution.
- Analysis approach can be used to inform decisions in future busbar designs.



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