Gate Driver Design for a High Power Density EV/HEV Traction Drive Using Silicon Carbide MOSFET Six-Pack Power Modules

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***Abstract*—Targeting the development of a silicon carbide (SiC) inverter for electric vehicle/hybrid electric vehicle (EV/HEV) applications, the design considerations of the gate driver for the adopted SiC metal-oxide-semiconductor field-transistor (MOSFET) power modules are presented. Given the system power density requirement, the gate driver design challenges for the commercial off-the-shelf (COTS) SiC modules are identified, analyzed, and tackled with proposed solutions. To accomplish such design with the constraint of limited layout space, a single chip MAX 13256 (3 mm×3 mm) enabled high frequency link based isolated bias supply structure is proposed for each six-pack module. Moreover, the gate driver design guidelines for module phase-leg parallel operation are introduced with a comparison study confirming the printed circuit board (PCB) layout effectiveness for electromagnetic interference (EMI) mitigation. Experimental validation is conducted on the traction inverter prototype.**

***Keywords*—Gate Driver, EV/HEV traction drive, SiC MOSFET power module, parallel operation.**

I. Introduction

Nowadays, SiC devices are being increasingly considered for efficient power conversion over their Silicon (Si) counterparts in view of higher blocking voltage capability, faster switching speed, better thermal conductivity, and lower conduction resistance [1]. Some exemplary investigations reported are 15 kV SiC MOSFET based solid-state transformer [2], [3], several-megahertz switching frequency based dc/dc converter [4], [5], and converter operation at over 200 °C junction temperature [6]. A promising application area is the transportation electrification. As the EV/HEV market rapidly expands in the automotive industry, the SiC devices can provide an effective solution for the high power density drivetrain requirement, high temperature environment, and high efficiency merit [7]–[11]. However, the penalties come with the fast switching transient di/dt, which induces overshoots and ringing due to parasitic inductances as well as the EMI emissions. Besides, the higher dv/dt coupling through the parasitic capacitances might result in high frequency circulating current deteriorating the controller functions. This makes the SiC devices gate driving circuit design more challenging compared with the conventional converter systems. Meanwhile, overall size limitation further enhances the design difficulty when automotive application is targeted.

On the other hand, the SiC devices can be paralleled to reach high current ratings. Three solutions can be found in the literature: paralleling the single-chip discrete devices, building a multi-chip module, or directly paralleling of the power modules. The first solution, indicating a higher flexibility for converter system structure, is usually easily affected by the uneven distribution of various parasitic parameters [12]. For the multi-chip modules, the external circuit layout becomes less significant if the chips are symmetrically distributed; however, such fabrication process has to depend on specific equipment and suffers from a lower yield rate. The parallel connection of COTS SiC power modules is recently reported for railway traction converter system [13]. Few papers investigate another possibility to achieve high current ratings through configuring the six-pack power modules into a half-bridge structure. The module characterization and comparison study is conducted in [14], [15]; however, the gate driver design and application performance are not evaluated. Hence, targeting a traction drive application, this paper investigates the gate driver design considerations and layout optimizations for COTS SiC MOSFET six-pack power modules from Wolfspeed (SKU: CCS050M12CM2) that are paralleled in a half-bridge configuration.

Section II describes the system overall layout and design requirement. Section III analyzes the gate driver design methodology and layout considerations where a comparison study is carried to verify its correctness. Experimental results are presented in Section IV. Section V draws the conclusion.

II. System description

The targeted 55 kW (30 kW continuous) traction drive system consists of a boost stage and a voltage source inverter (VSI) stage. The system topology is shown in Fig. 1, where the interleaved dc/dc scheme is adopted to reduce the current ripple and support the adaptive dc bus regulation. The VSI stage is implemented with three power modules where each six-pack module is configured into a half-bridge structure. The overall system packaging is demonstrated in Fig. 2, where the power modules, cold plate and the boost inductors are stacked in a compact planar configuration [11]. The featured double-sided cooling cold plate structure greatly improves the space utilization and system thermal performance. Assessing

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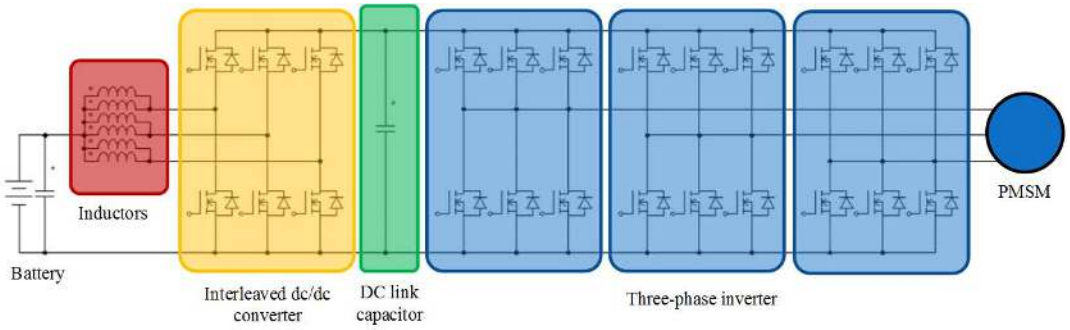


Fig. 1: Traction drive system under consideration.

the gate driver requirement from overall system perspective, the benchmark COTS gate driver (SKU: CGD15FB45P1) will not fulfill the system power density objective, since the overall board dimension is too large (168.61 mm×152.40 mm×38.15 mm). The size comparison with a power module side by side is shown in Fig. 3. Another challenge comes from the module layout structure where each top switch crosses over with the bottom switch as indicated in Fig. 4. Thus, special design consideration needs to be taken for the half-bridge configuration.

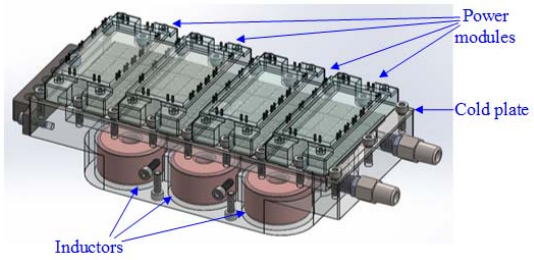


Fig. 2: Traction drive system layout.

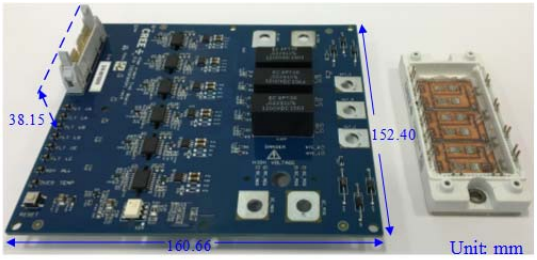


Fig. 3: Benchmark gate driver board (one module) and the SiC MOSFET power module.

III. Gate Driver Design Methodology

A. Driver IC Selection

In this design, an isolated gate driver is considered for each active switch/switch set for noise attenuation. Compared with the Si counterparts, not many COTS driver ICs tailored for SiC MOSFETs are available in the market [16]. The capacitive

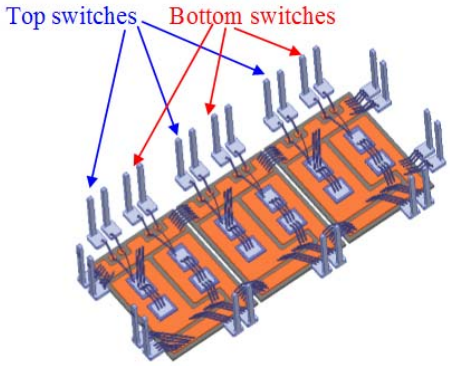


Fig. 4: SiC module decomposition.

isolated driver IC ISO5852S, which is released recently from Texas Instrument, is selected. The critical function comparison with the state-of-the-art INFINEON 1ED020I12, which is adopted in the benchmark gate driver board, are listed in Table I. It is observed that the ISO5852S has higher common-mode transient immunity, short propagation delay time, and soft turn-off compared with 1ED020I12. This comparison clearly indicates its advantages for SiC MOSFETs driving. It is acknowledged that the source/sink short circuit current for the selected driver output is 2.5/5 A, which might limit the SiC MOSFET switching speed with such driver current capability. Thus, an external current booster (IXDN609SI) is specified for each switch, which increases the peak source/sink current to 9 A.

TABLE I: Function Comparison of gate driver IC

Item	1ED020I12	ISO5852S
Common-mode transient immunity	50 kV/μs	100 kV/μs
Propagation delay	165 ns	76 ns
Output voltage range	(-12V, +20V)	(-17.5V, +35V)
Desaturation protection	Yes	Yes
Soft turn-off	No	Yes

B. Isolated Bias Supply Solution

The other critical element for the isolated gate driver is the bias supply. The simple solution is directly acquiring essential

COTS dc/dc modules since they are widely available in various voltage/power range. However, the penalty is the bulky driver board volume when each switch needs an isolated bias rail, and it becomes even worse when multiple modules are actually used. In addition, the COTS dc/dc modules usually come with a relatively large coupling capacitances (over 10 pF), which may fail the system where a high dv/dt switching is essentially required. In this design, a single chip enabled high frequency link based isolated bias supply solution is provided for an entire module. The supply structure is shown in Fig. 5 where the H-bridge converter is switching at roughly 500 kHz with close to 50% duty ratio. With this structure, either a single multi-winding transformer or a multiple-transformer layout is possible. Since the primary current lags the input voltage, it can naturally achieve zero voltage soft-switching (ZVS) on the primary side H-bridge circuit without voltage spike even if the leakage inductance of transformer is not very small. This structure makes it possible to minimize the parasitic capacitance between all the isolation barriers with low-profile and high efficiency. The design procedure, analysis and experiment validation are presented in [17] and are not repeated here.

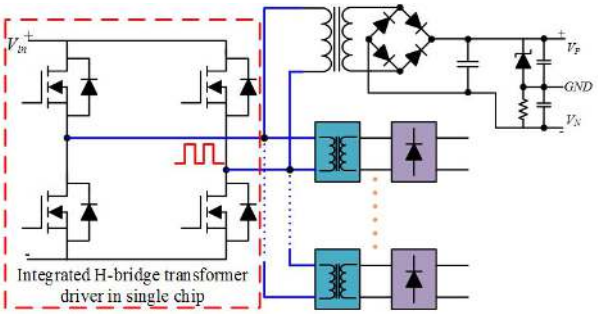


Fig. 5: High frequency link enabled bias supply structure.

C. Parallel Layout Considerations

Considering the crossover layout for the adopted power module in Fig. 4, the gate driver PCB layout principle is elaborated since special attention shall be made to achieve the proposed parallel operation. First, to reduce the gate loop parasitic inductance, the gate peripheral components are placed in close proximity to the switch pins. The direct solder connection is thus favored over the wire/socket interface to fulfill such requirement. Second, functional isolation clearance needs to be maintained, which includes the primary ground plane with respect to all the secondary ground planes and in between of each isolated ground planes. Third, high-frequency PWM signal traces are shielded with ground planes placed in adjacent layers to reduce potential EMI emissions. Last but not the least, the overlap of top and bottom switch ground planes shall be strictly avoided, considering the floating potential might easily cause a common circulating current through the parasitic capacitance. It is true that doing so might cause extra layout area; however, the design reliability and correctness will not be compromised.

On the other hand, gating signal synchronization for parallel devices are of significant importance. Although the positive temperature coefficient for power MOSFET can automatically balance the thermal distribution at steady state, a symmetrical layout is still critical for the device switching dynamic synchronization and thus the overall lifetime for the paralleled devices. For the given system requirements, two layout strategies are evaluated. The first one, shown in Fig. 6, features a low-cost, fewer components solution, which considers a central current booster IC for each top/bottom parallel device sets. A 30 A source/sink current booster IC (IXDN630YI) is selected without limiting the device switching speed. However, the first penalty that comes with such layout is the crosstalk between the top and bottom switch gating loops which is unavoidable. This is clearly indicated with the loop interference shown in Fig. 6. The recorded results indicate that such crosstalk interference might lead to the false trigger of the driver protection mechanism, which assumes a short circuit condition for the top and bottom switch, and thereby causing an erroneous operation. Fig. 8a shows the inverter test results with static RL load, where the dc link voltage and three-phase currents waveforms become distorted when the input voltage is increasing towards 100 V. An unbalanced operating condition is clearly observed, where only Phase-A and Phase-C are remaining functional and Phase-B is lost. Further investigation shows that Phase-B drivers are falsely shut off at certain instant when higher dv/dt is seen, which causes such unbalanced system operation at the output side. Fig. 8b records the distorted gating signals from device side, which also validates that a serious crosstalk noise is coupled into normal gating signals. The second penalty comes with the gate signals synchronization. Such layout scheme unavoidably results in different gating loop sizes, which brings in switching delays for the paralleled switches. A clear time delay can be observed comparing the sync situation for the PWM gate signal sets. It is worthwhile to note that specifying various gate resistor R_G value can help attenuate the difference thus improving the sync. As seen in Fig. 7, R_G is tuned and set as 1.5 Ω, 2.5 Ω, 3.5 Ω for the top switches #5, #1, and #3, respectively. Similar conditions apply to the bottom switch sets. The values are chosen empirically following the switch distance to the current booster location. The results show an improvement for the sync; however, it is still observed up to 2 ns time delay in-between.

Both the crosstalk EMI and switching synchronization issues point to new solutions. The second layout configuration is shown in Fig. 9. Compared with the first solution, this one adopts a symmetrically distributed current booster for each single switch. First, this layout contributes to smaller gate loops since the distributed current booster can guarantee the same gate loop area from the device perspective. Each local current booster only needs to supply one individual switch. Second, the PWM signal traces are routed following the shown arrow directions, which are completely isolated from the gate loop crossing. The compromise is that additional layout area is required, and the total component count has to increase. The parallel sync is validated experimentally with a double pulse test (DPT) as shown in Fig. 10, where Fig. 10a and Fig. 10b present the turn-on and turn-off transients, respectively. It is seen that the three parallel gating signals can achieve the same rising and falling edge without any delay, which fulfills the design requirement. It is noted that in the test, the same values of R_G can be set accordingly where the turn-on

resistance is 4.5 Ω and the turn-off resistance is 2.25 Ω. The observed spikes and ringing in the waveforms highly depend on the DPT setup, testing points, probe parasitics. It may not exactly represent the real switching scenarios. However, the signal synchronization shall not be affected, which verifies the correctness of the proposed solution.

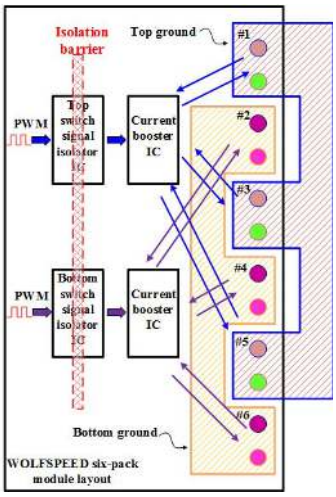
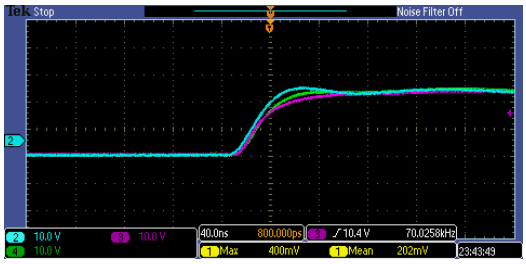
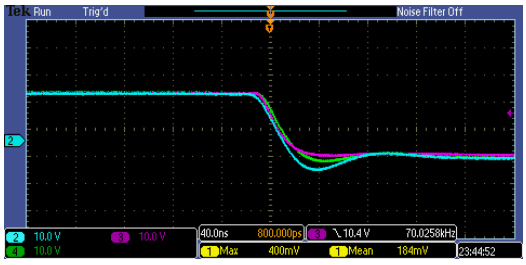


Fig. 6: PCB layout method I.

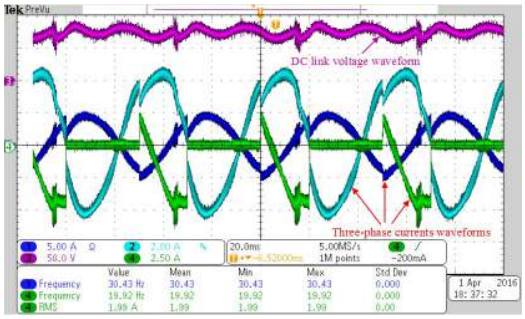


(a) Turn-on Gate synchronization.

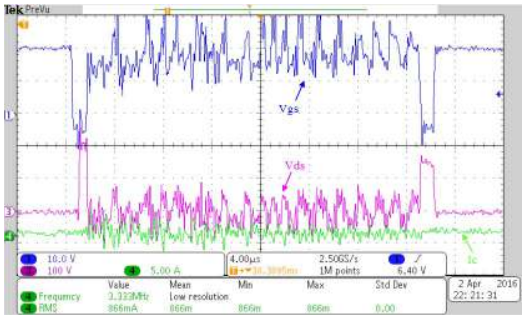


(b) Turn-off Gate synchronization.

Fig. 7: Gating signal synchronization with a central current booster.



(a) Distorted three phase currents and dc link voltage.



(b) Phase-C bottom switch V_{GS}, V_{DS}, and phase current.

Fig. 8: Electromagnetic interference due to crosstalk.

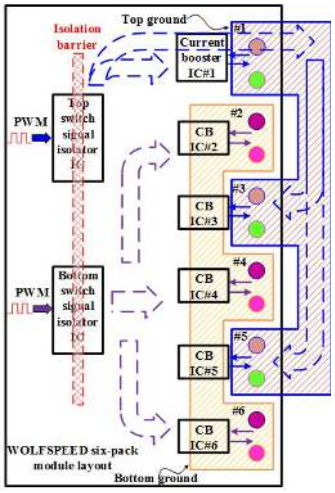
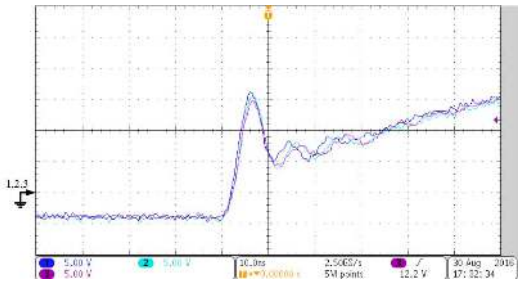


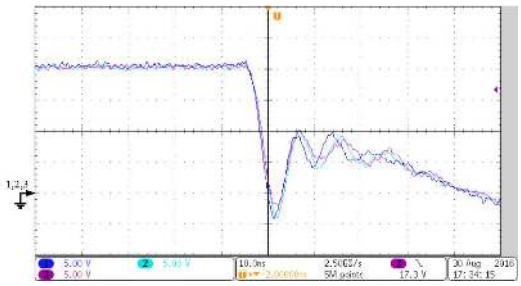
Fig. 9: PCB layout method II.

IV. Experiment Results

The picture of fabricated hardware prototype (240 mm × 129 mm × 6 mm) is shown in Fig. 11 which accommodates four power modules and achieves over 10× volume reduction compared with the benchmark gate driver board (168.61 mm×152.40 mm×38.15 mm×4). The customized eight-layer gate driver board fulfills the driving, isolation, protection and sensing functions within the size constraint. One PCB layer snapshot is shown in Fig. 12, where the four module accommodation can be identified. The leftmost module, distinguishing itself with six independent isolated supply, is the interleaved dc/dc stage. While the rest of modules work as the three-phase legs of dc/ac stage where the parallel configuration can be clearly observed. It is noted that some pins of the module are intentionally omitted during the footprint design so that more room is available for the gate driver board component. Besides, such scheme contributes to reduce the design complexity



(a) Turn-on Gate synchronization.



(b) Turn-off Gate synchronization.

Fig. 10: Gating signal synchronization record with distributed current boosters.

mixing both control and power circuit signals. For example, all the switching middle points of each paralleled module are short-circuited through the bottom busbar PCB, not penetrating the gate driver board, except for one single switching point left for desaturation detection. Fig. 14 demonstrates system test results during continuous operation with three-phase RL load, and the switching frequency is set at 35 kHz with 600 V dc link for a 20 kW output. The waveform presents the drain-source voltage (Vds) of the Phase-C bottom switches. It is noted that the voltage spike is maintained as low as 3% and almost no ringing or oscillations can be observed. The inverter three-phase current waveforms with 650 V dc link and 28 kW output power are presented in Fig. 15, which further proves the design novelty. The proposed gate driver design and layout scheme enables efficient usage of the SiC devices, which contributes to the optimized system overall performance. It is noted that the power loop parasitic optimization also contributes for such performance, which involves both distributed dc link capacitor banks and optimization of the integrated PCB based busbar structure.

V. Conclusion

In this paper, the gate driver design methodology for the COTS SiC power module is introduced which is targeted for the development of a 55 kW traction inverter system. The design challenges are identified and tackled with proposed solution. Specifically, the gate driver IC selection, bias supply design, and the layout considerations for adopted sixpack modules are explained. Experimental results are provided to verify the design novelty. The quantified discussions and double pulse test results for the synchronized switching validate the correctness of the phase-leg operation for high current

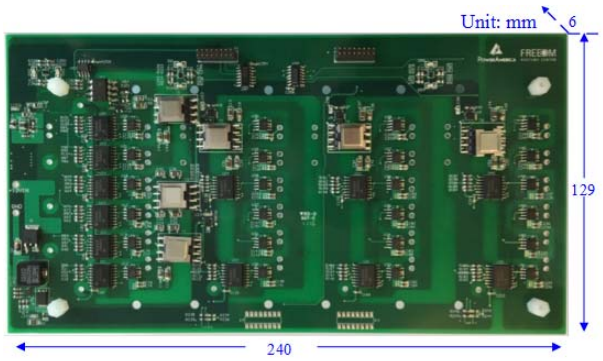


Fig. 11: Picture of hardware prototype.

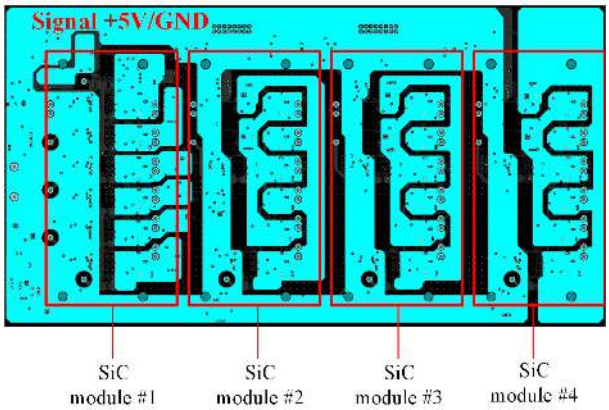


Fig. 12: PCB layout of the gate driver board.

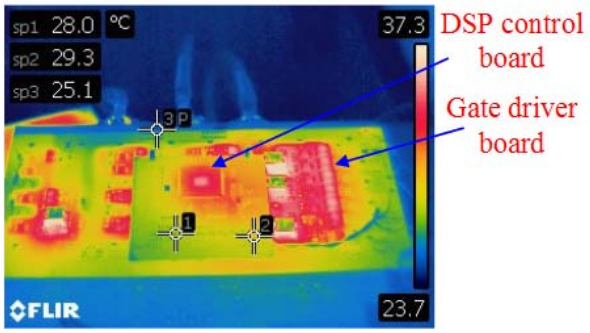


Fig. 13: System thermal performance (Natural air convection under 20 kW operation).

operation.

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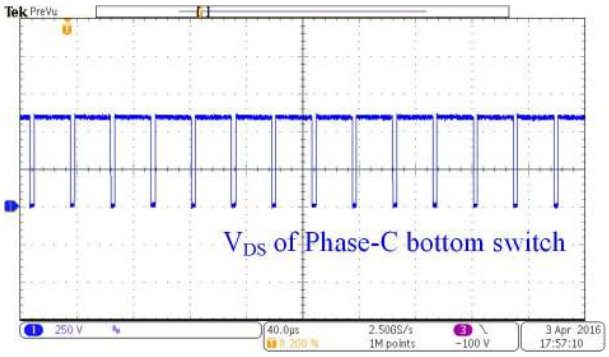

Fig. 14: Bottom switch V_{DS} waveform.

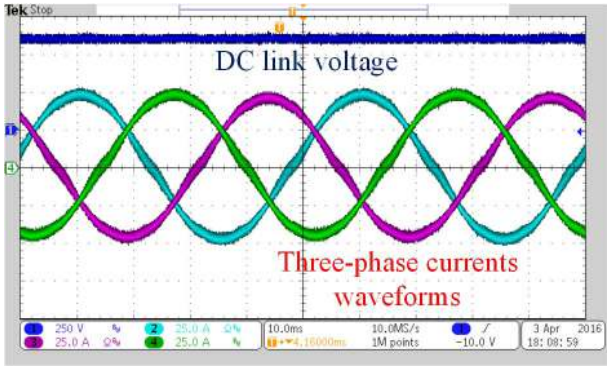

Fig. 15: System continuous operation waveforms.

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