Decentralized Synchronization of AC-Stacked Voltage Source Converters

M A Awal, Hui Yu, Iqbal Husain, Wensong Yu, Srdjan Lukic
FREEDM Systems Center
North Carolina State University
Raleigh, USA
Email: mawal@ncsu.edu

***Abstract*— A decentralized control method is proposed for a system of multiple voltage source converters (VSC) stacked in series on the AC side. Using the proposed method, a group of low-voltage rated VSC modules can be utilized to implement converters for medium/high voltage grid-tied applications. Each converter module can maintain synchronization using only its local measurements without any communication or any form of centralized synchronization signal. A mathematical model of such a system consisting of *N* number of VSC modules employing the proposed control scheme is presented and a linearized model is developed for small signal stability assessment. The proposed method is robust against grid frequency variation and can naturally correct power sharing errors among modules caused by sensor inaccuracies or reference mismatches. Real time simulation results are presented to validate the proposed controller.**

Keywords—AC-stacked inverter; series stacked AC; communicationless synchronization;

I. INTRODUCTION

Recent advancements of power semiconductor technology and magnetic materials have enabled power electronic conversion in medium and high voltage applications. Lack of high voltage power devices and reliability issues with non-modular approaches still remain the major limitation for such applications. Modular multi-level converters have gained great popularity over the last decade for high voltage applications. Cascaded H-bridge (CHB) based multi-level topologies have also become the mainstream in different applications such as in STATCOM, grid tied PV [1], and industrial motor drives [2]. The main advantage of all multi-level topologies is the low switching frequency resulting in reduced switching loss. However, the penalty paid for the gain in reduced loss, is the complexity of control and limitation on scalability due to the centralized control. In both MMC and CHB topologies, the capacitor voltage balancing in different modules remains an open research problem [3, 4]. To achieve scalability or for a large number of modules, very high bandwidth communication is required [5, 6]. To reach higher voltage levels by series cascading multiple converter modules on the AC side and to circumvent the control complexities and high bandwidth communication requirements, small LC filters with the H-bridge modules can be incorporated [7-9]. In this topology, the so-called "Inverter Molecules" are switched at a very high frequency as they are rated for low voltage operation resulting in small switching loss and due to high switching frequency they require very small passive filter components. By adding such small filters, the modules can be controlled in a distributed way. One of the modules is assigned the task of regulating the current in the series connection and is called a current administrator voltage compensator (CAVC), and the rest of the modules regulate their output voltage to independently control their real and reactive power injection. This topology has been utilized for grid-tied PV application. However, the control structure requires inhomogeneous assignment of responsibility to different modules. For example, the CAVC module is solely responsible for regulating the current of the entire loop which leads to a single point of failure situation. The inhomogeneous role of different modules in this distributed control method limits the performance of the systems in terms of modularity, reliability and robustness, and therefore, not attractive for medium voltage or high voltage applications. In [11], a droop based method is proposed to regulate the real power flow through each module. The system uses a central controller that senses the grid voltage and needs to send synchronization signal to all the modules. To the best of the authors' knowledge, a decentralized synchronization method for AC-stacked VSCs without any form of communication has not been reported in the existing literature.

In this work, a complete decentralized control strategy is proposed where each low-voltage module can maintain synchronization without any form of communication with other modules or a central controller. Fig. 1 shows different control structures for AC-stacked systems. Both centralized and distributed control structures require some form of communication [7-11]. However, using proposed decentralized structure each module can independently regulate its own real and reactive power flow using only local measurements. The proposed method can maintain synchronization against deviation in grid frequency. In an AC-stacked PV inverter system panel level maximum power point tracking (MPPT) can be achieved using the proposed method. A special form of the controller has an inherent property that can naturally correct any power sharing error among different modules resulted by sensor inaccuracies or reference mismatches which is highly suitable for modular design of medium or high voltage power electronics. The homogeneity and complete decentralized operation of each module makes the proposed control method suitable for any AC-stacked system, e.g. AC-stacked PV system, medium/high voltage applications such as solid state transformers (SSTs) or, power electronic transformers (PETs), and industrial motor drives.

The rest of the paper is organized as follows: First, the proposed control structure is presented and a comprehensive analytical model of the system is developed. Second, controller parameter selection process is described. Third, small signal stability of the proposed controller is evaluated using eigenvalue analysis. Finally, the proposed method is then adopted in a three-module AC-stacked system and performance of the proposed method is validated in an OPAL RT based real-time simulation platform.

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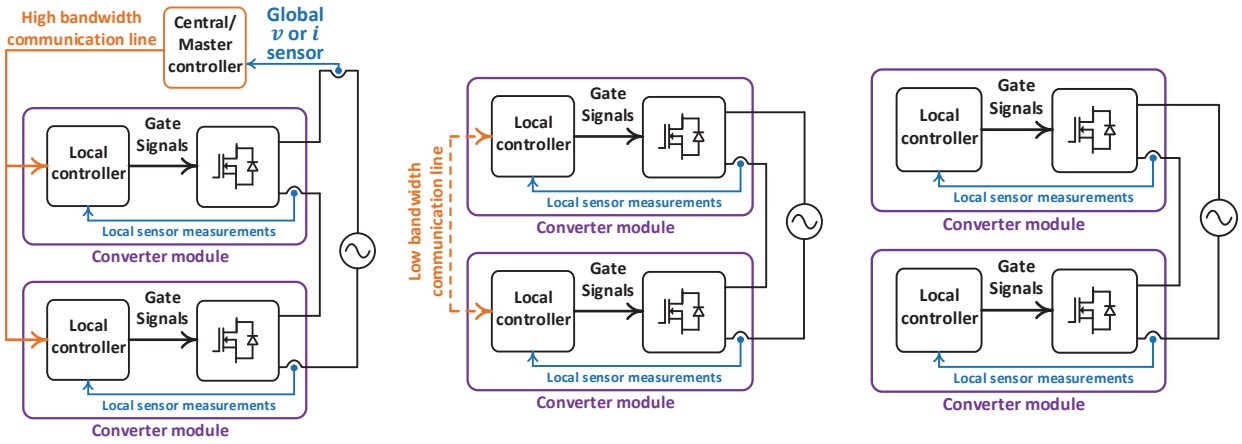

Fig. 1. Different control architecture for AC-stacked VSC system: (a) Centralized control with communication, (b) distributed control with communication, (c) decentralized control without communication.

II. System Description

Fig. 2 shows a system of N AC-stacked VSCs connected to an AC source v_g. For single phase application, each module consists of a single H-bridge unit equipped with an LC filter. For three phase applications, each module consists of three H-bridge units on the front end. However, unlike the multilevel modulation done in [12], an LC filter is to be added to each H-bridge unit. The control objective for each module is to retain synchronization at all times while regulating real and reactive power at its output port without the need for any communication with other modules or a central controller. Therefore, each module controller must operate solely based on sensor measurements locally accessible to that module. Towards that end, a time scale separated control approach is adopted. At the fastest time scale each module employs a voltage tracking controller that ensures precise tracking of the voltage reference provided by a higher-level controller running at a slower time scale which is responsible for maintaining synchronization with other modules and power regulation through its port. It is worth noting that a very high switching frequency for the power devices are assumed which should enable very fast response by the voltage tracking controller. A very wide range of voltage tracking methods for VSCs are available in existing literature which may also include an inner current control loop. These fast scale tracking controllers may be subject to harmonic resonance instability issues [13] which is considered out of the scope for this work. The overall objective of this research effort is to develop a decentralized control method that generates the voltage reference based on local measurements.

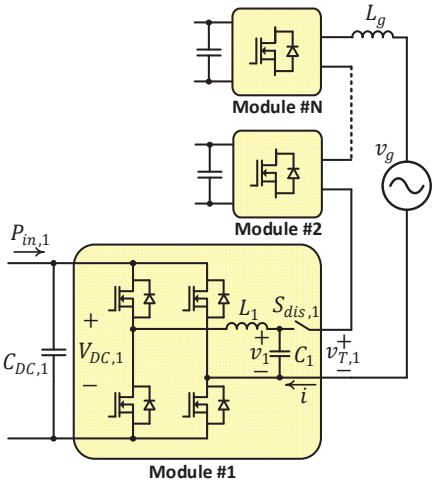

Fig. 2. N voltage source converters (VSC) stacked on the AC side.

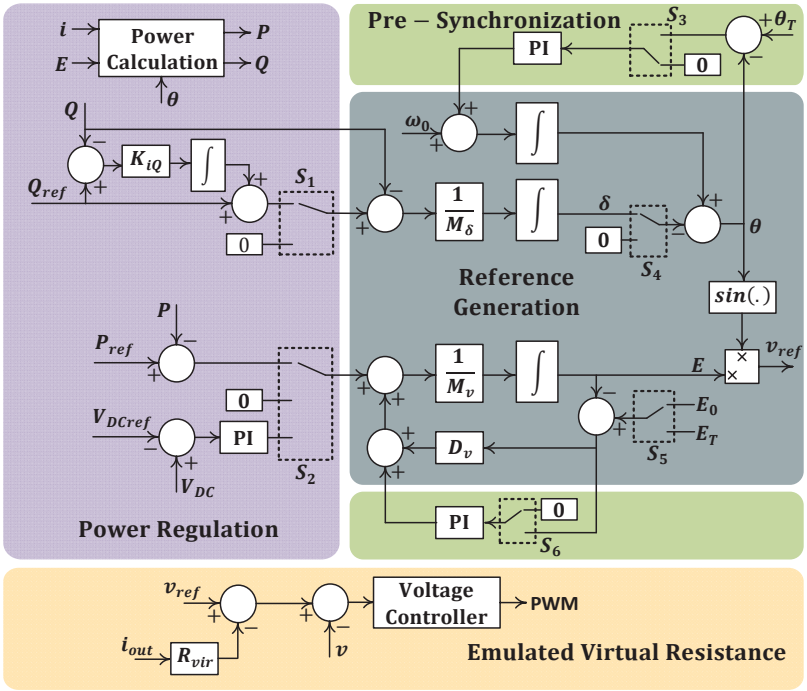

Fig. 3. Proposed decentralized control structure of a VSC module.

III. Principle of Operation

Due to the AC-stacking, identical current i flows through all of the VSC modules. To enable homogeneous control in all the modules, each module is programmed to control its own output voltage. Therefore, real power P_k at the output of the k-th module can be regulated by dynamically updating the output voltage amplitude E_k. Regulation of reactive power is achieved by linking the frequency ω_k with reactive power Q_k. However, ω_k does not correspond to the common frequency of the system but is an internal instantaneous frequency which can be thought of as the self-frequency of each module. Synchronization is achieved in the AC-stacked system when all modules reach identical self-frequencies, i.e., $\omega_1 = \omega_2 = \cdots = \omega_N$. It should be noted that the synchronization of the modules is a complex phenomenon achieved by proper operation of both $P_k - E_k$ and $Q_k - \omega_k$ loops. Certain level of decoupling between the two loops can be achieved by virtually emulating a resistive output impedance in each module.

A. System Model

The inner voltage tracking controller is run at a much faster time scale and must have a high control bandwidth, i.e., at least a decade higher than fundamental frequency. Therefore, for the following analysis of the synchronization and power regulation loops, without loss of any generality prefect voltage reference tracking is assumed, i.e., $v_k = v_{ref,k}$.

The instantaneous voltage at the output of the k-th module is given by

$$v_k = E_k(t)\sin\{\theta_k(t)\} \tag{1}$$

$$\theta_k(t) = \omega_0 t + \delta_k(t) \tag{2}$$

For phasor based analysis, a reference frequency ω_0 is assumed and therefore, the module output voltage has the following phasor representation.

$$v_k = E_k e^{j\delta_k} \tag{3}$$

The current flowing through the AC-stacked system can be expressed as (4).

$$i = \frac{\sum_{k=1}^{N} E_k e^{j\delta_k} - E_g}{R_{eq}} \tag{4}$$

Here, the phase of the source voltage, $v_g = E_g e^{j\delta_g}$, is taken as the reference phase, i.e., $\delta_g = 0$. The emulated virtual resistance R_{vir} is considered as part of the network and is so chosen such that the entire network exhibits a dominantly resistive behavior, i.e., $X/R < 1/10$ for the modules. The total impedance seen by the modules is approximated as $Z_{eq} \approx R_{eq} = NR_{vir}$. Therefore, the real and reactive power flowing out of the k-th module is given by

$$P_k = \frac{E_k^2 + \sum_{m=1,m\neq k}^{N} E_k E_m \cos(\delta_k - \delta_m) - E_k E_g \cos(\delta_k)}{2R_{eq}} \tag{5}$$

$$Q_k = \frac{\sum_{m=1,m\neq k}^{N} E_k E_m \sin(\delta_k - \delta_m) - E_k E_g \sin(\delta_k)}{2R_{eq}} \tag{6}$$

B. Controller Structure

The total control structure for a module is shown in Fig. 3. The controller consists of real and reactive power regulation blocks as well as a pre-synchronization unit. The different parts of the control structure are explained in detail in the following subsections.

1) Real Power Regulation

The control structure can enable both real power reference tracking as well as DC bus voltage control. The AC output voltage amplitude E_k is updated using the following dynamic equation:

$$M_v \dot{E_k} = D_v(E_0 - E_k) + \left(P_{ref,k} - P_k\right) \tag{7}$$

The nominal voltage amplitude is chosen as $E_0 = E_g/N$. It is evident that there exists a steady state error between $P_{ref,k}$ and P_k. This steady state error provides an inherent advantage of naturally correcting power sharing inaccuracies against power reference mismatches among different modules which will be shown in the results section.

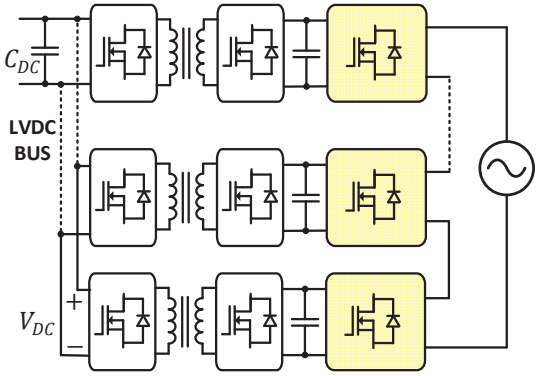

Fig. 4. AC-stacked VSC modules connected to medium voltage with isolated DC-DC stages connected in parallel for low voltage DC output.

For medium voltage to low voltage DC (LVDC) application, N modules can be stacked to support the medium voltage. Each module should include an isolated DC-DC stage. The isolated low voltage DC outputs can be connected in parallel to increase the power capacity. Since each module can locally measure the common LVDC bus, decentralized load sharing can be achieved by implementing a DC droop relation between the common LVDC bus voltage V_{DC} and power injection $P_{DC,k}$ through the DC-DC stage. Each module can run an independent proportional-integral (PI) compensator for controlling the local DC bus voltage $V_{DC,k}$. The dynamics of the DC bus voltage is given as the following.

$$\frac{C_{DC,k}}{2}\frac{dV_{DC,k}^2}{dt} = P_{DC,k} - P_k \tag{8}$$

The power flow through the LVDC bus is dictated by the load or source connected to the bus which directly affects $P_{DC,k}$ in each module. Therefore, for the DC bus voltage tracking, $P_{DC,k}$ is considered as an unknown disturbance and P_k is used for actuating the control. Finally, the bus voltage reference tracking can be achieved by modifying the real power regulation loop as (9).

$$M_v \dot{E_k} = D_v(E_0 - E_k) - \mathcal{G}_k \tag{9}$$

Here, $\mathcal{G}_k = \left(K_p + K_i \int\right)\left(V_{DCref} - V_{DC,k}\right)$. Uniform power sharing by the modules translates into equal voltage sharing by them on the AC side, but even with identical control parameters, sensing inaccuracies along with different PI compensator loops in different modules are expected to lead to

mismatches among g_k in different module controllers. A large enough damping coefficient D_v ensures minimal deviation from nominal voltage E_0 in steady state, which is evident from (9). Therefore, D_v not only dampens oscillations during transients but assists in uniform power sharing by the modules as well. In AC-stacked PV systems, the control objective is to achieve panel level MPPT without an intermediate boost stage which inherently requires each module to process different amount of real power depending on available solar irradiance on respective PV panels. In such application, the isolated DC-DC statge is not present and each module implements a MPPT algorithm which dynamically generates the DC bus voltage reference $V_{DCref,k}$. It is worth noting that (7) implements an explicit negative feedback of real power P, whereas real power feedback is taken implicitly through the DC bus voltage in (9).

2) Reactive Power Regulation

The instantaneous reference phase angle δ_k is generated using the following dynamic model.

$$M_\delta \dot{\delta_k} = -\left(Q_{ref,k} - Q_k\right) - K_{iQ}\xi_k \tag{10}$$

$$\dot{\xi_k} = \left(Q_{ref,k} - Q_k\right) \tag{11}$$

The integral action implemented through ξ_k not only enables reactive power regulation but also dynamically corrects the self-frequency of the module in case of drift in the grid frequency.

3) Pre-Synchronization

Each module is equipped with a disconnect-switch denoted as $S_{dis,1}$ in Fig. 2. Prior to closing the disconnect-switch, each module goes through a pre-synchronization process. A phase-locked-loop (PLL) is run on $v_T = V_T \sin(\theta_T)$ and using two simple PI loops, shown in Fig. 3, the module voltage phase and amplitude can be matched with θ_T and V_T, respectively. During the pre-synchronization step, any deviation in the grid frequency from the preset frequency reference ω_0 is automatically compensated by the PI loop responsible for phase matching. During the pre-synchronization step switches S_1 through S_6 are kept in the 2nd position and once connected to the system the switches are taken back to the default position shown in Fig. 3. Switch S_2 has a third position that can be used for DC bus voltage control.

Note that the proposed control structure requires calculation of real and reactive powers at each module output. As shown in Fig. 3, for power calculation the measured current i through the module and the controller states E_k and θ_k are used. Evidently, the effect of the virtual resistance is excluded from the power calculation which is essential to ensure that the virtual resistance is emulated as a part of the network and not of the module itself. The small error in power calculation contributed by the exclusion of R_{vir} is dynamically compensated through g_k by the PI compensator for DC bus voltage tracking. For single phase systems, the AC variation in real and reactive power is filtered out by using simple low pass filters. For three phase systems, such low pass filters can be used to ensure proper time scale separation among different control levels.

IV. Controller Parameter Selection

The controller parameter selection is to be done based on the overall system specifications. The nominal voltage rating for the modules immediately follows from the number of modules used in the system. At nominal operating condition, the N AC-stacked modules should share the source voltage equally, i.e., $E_0 = E_g/N$. As explained in the following subsection through small signal analysis, it is essential to choose the damping coefficient properly to ensure sufficient damping for the overall stability of the entire system. The preliminary design of D_v can be done based on straightforward power flow solution. Assuming uniform voltage sharing among modules, for any arbitrary power P_{ss} through each module, the current in the AC-stacked system is given as follows:

$$I_{ss} = \frac{2P_{ss}}{E_{ss}} \tag{12}$$

$$I_{ss} \approx \frac{NE_{ss} - E_g}{NR_{vir}} \tag{13}$$

Combining (12) and (13), the following quadratic equation is obtained which can be solved for E_{ss}:

$$NE_{ss}^2 - E_g E_{ss} - 2NR_{vir}P_{ss} = 0 \tag{14}$$

Proper selection of R_{vir} is necessary to ensure that the power flow constraint given by (14) is not violated at any point within the entire operating range, i.e., $P_{ss} \in [P_{min}, P_{max}]$. It is to be noted that operation at unity power factor is considered for the parameter design process. In case of weak grid or higher grid impedance, comprehensive power flow analysis should be performed considering variation in the grid impedance. Solving (14) at the extremes of $[P_{min}, P_{max}]$, the range of operating voltages $[E_{min}, E_{max}]$ of each module can be obtained. Utilizing the range of operating voltages, D_v can be selected as follows:

$$D_v = \frac{P_{max} - P_{min}}{E_{max} - E_{min}} \tag{15}$$

Once D_v is chosen using (15), for a desired response time of the real power regulation loop in the order of T_v, M_v is selected using (16).

$$M_v = T_v D_v \tag{16}$$

The reactive power dynamics given by (10) and (11) is not as straightforward as that of the real power regulation loop. The speed of synchronization and reactive power tracking is affected by the choice of M_δ and K_{iQ}. The stability of the overall system must be analyzed using the small signal model given in the following section. However, a preliminary value of M_δ can be selected using the following.

$$M_\delta = \frac{\Delta Q_{max}}{\Delta \omega_{max}} \tag{17}$$

Here, ΔQ_{max} and $\Delta \omega_{max}$ correspond to the maximum expected variation during transients in reactive power and instantaneous self-frequency of the modules, respectively. A larger M_δ leads to longer response time and vice versa. The integral gain K_{iQ} should be selected considering the stiffness of the grid, i.e., maximum deviation in grid frequency. For a response time in the order of T_δ, an initial selection of $K_{iQ} = 1/T_\delta$ can be made and should be further adjusted through small signal analysis.

V. Small Signal Model

The system model including the controller can be linearized to obtain the following state space model.

$$\dot{\boldsymbol{X}} = \boldsymbol{AX} \tag{18}$$

$$\boldsymbol{X} = [\delta_1\ \delta_2\ \dots\ \delta_N\ E_1\ E_2\ \dots\ E_N\ \xi_1\ \xi_2\ \dots\ \xi_N]^T;$$

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{A_{11}} & \boldsymbol{A_{12}} & \boldsymbol{A_{13}} \\ \boldsymbol{A_{21}} & \boldsymbol{A_{22}} & \boldsymbol{A_{23}} \\ \boldsymbol{A_{31}} & \boldsymbol{A_{32}} & \boldsymbol{A_{33}} \end{bmatrix}$$

Here, $\boldsymbol{X} \in \boldsymbol{\mathcal{R}^{3N}}$, $\boldsymbol{A} \in \boldsymbol{\mathcal{R}^{3N\times 3N}}$, and $\boldsymbol{A_{mn}} \in \boldsymbol{\mathcal{R}^{N\times N}}$. It is worth noting that the dynamics of the DC bus voltage controller is excluded from the linearized model. $P_{ref,k}$ is assumed to be constant for the following analysis. Form (7), (10), and (11), it immediately follows that $\boldsymbol{A_{23}} = \boldsymbol{A_{33}} = [\boldsymbol{0}]_{N\times N}$. The rest of the sub-matrices are defined in Table I.

TABLE I. DEFINITION OF $\boldsymbol{A}$

$\boldsymbol{A}_{11}(k,k)$	$\frac{\sum_{m=1,m\neq k}^{N} E_k E_m \cos(\delta_k-\delta_m) - E_k E_g \cos(\delta_k)}{2M_\delta R_{eq}}$
$\boldsymbol{A}_{11}(k,m)$	$\frac{-E_k E_m \cos(\delta_k-\delta_m)}{2M_\delta R_{eq}}$
$\boldsymbol{A}_{12}(k,k)$	$\frac{\sum_{m=1,m\neq k}^{N} E_m \sin(\delta_k-\delta_m) - E_g \sin(\delta_k)}{2M_\delta R_{eq}}$
$\boldsymbol{A}_{12}(k,m)$	$\frac{E_k \sin(\delta_k-\delta_m)}{2M_\delta R_{eq}}$
$\boldsymbol{A}_{13}$	$-\frac{K_{iQ}}{M_\delta}\boldsymbol{I}_{N\times N}$; $\boldsymbol{I}_{N\times N} \rightarrow$ Identity matrix
$\boldsymbol{A}_{21}(k,k)$	$\frac{\sum_{m=1,m\neq k}^{N} E_k E_m \sin(\delta_k-\delta_m) - E_k E_g \sin(\delta_k)}{2M_v R_{eq}}$
$\boldsymbol{A}_{21}(k,m)$	$\frac{-E_k E_m \sin(\delta_k-\delta_m)}{2M_v R_{eq}}$
$\boldsymbol{A}_{22}(k,k)$	$\frac{-2E_k - \sum_{m=1,m\neq k}^{N} E_m \cos(\delta_k-\delta_m) + E_k \cos(\delta_k)}{2M_v R_{eq}} - \frac{D_v}{M_v}$
$\boldsymbol{A}_{22}(k,m)$	$\frac{-E_k \cos(\delta_k-\delta_m)}{2M_v R_{eq}}$
$\boldsymbol{A}_{31}, \boldsymbol{A}_{32}$	$-M_\delta \boldsymbol{A}_{11}, -M_\delta \boldsymbol{A}_{12}$

The state space model given by (18) can be used for eigenvalue analysis and the controller parameters can be tuned if necessary.

VI. Real-time Simulation

Real-time simulation study is performed to validate the proposed control method using an OPAL RT based system. First, to evaluate the performance of the controller without the dynamics of the DC bus voltage control, a three-module system is considered with ideal DC voltage sources. Later DC bus voltage compensator is added to the system.

A. Real-Time Simulation Setup

The OPAL-RT based real-time simulation platform is a powerful tool for the verification of large-scale power electronics systems. An overview of the platform is depicted in Fig. 5. The AC stacked VSC system, which includes both the circuit and controller part, is first modeled and compiled on Matlab/Simulink, and then loaded in the real-time simulator (OP5607). The electrical signals are available from the Analog Out of the simulator and can be monitored through the oscilloscope.

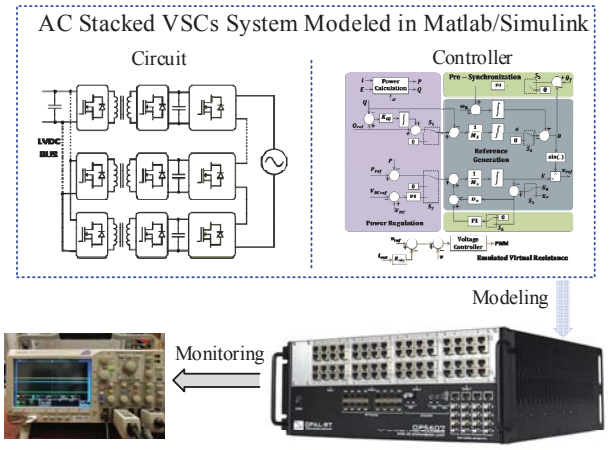

Fig. 5. Opal-RT based real-time simulation platform.

B. Controller Evaluation with Ideal DC Sources

The objective of this simulation study is to evaluate the performance of the proposed control method excluding the effect of DC bus voltage compensator as well as to verify the robustness of the controller against grid frequency variation. The modules are designed for a switching frequency of 50kHz. Table II lists the system parameters. Three modules are used to reach standard household voltage of 120V.

The system settles within nearly six fundamental cycles when a step change is applied in the real power reference in the modules. The reversal of power flow direction is evident from the phase displacement between the module output voltages and grid current in Fig. 6.

TABLE I. SYSTEM SPECIFICATION

System Parameters	
N	3
E_g	169.7 V
ω_0	$2\pi(60)$ rad/s
Module Parameters	
L	75 µH
C	3 µF
V_{DC}	70 V
Controller Parameters	
E_0	56.6 V
R_{vir}	0.1 Ω
D_v	282.3
M_v	2.823
M_δ	10000
K_{iQ}	0.1

1) Robust Synchronization Against Grid Frequency Drift

To evaluate the robustness of synchronization, the grid is modelled with a ramp increase in frequency from the nominal value. Fig. 7 shows the deviation of grid frequency from the nominal 60Hz in a ramp fashion and it settles at 60.1Hz. During the transient disturbance in grid frequency, the reactive power

through the module undergoes transient but quickly retains the nominal operation, i.e., $Q = Q_{ref} = 0$ as soon as the grid frequency settles. The real power injection does not go through any noticeable transient.

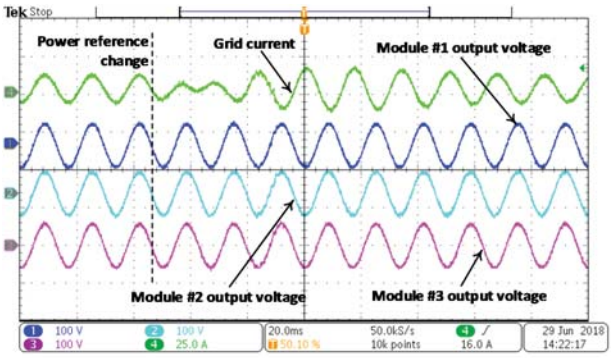

Fig. 6. Grid current and output voltages of the VSC modules in response to step change in real power reference. The power output from each module goes from 250W to -250W.

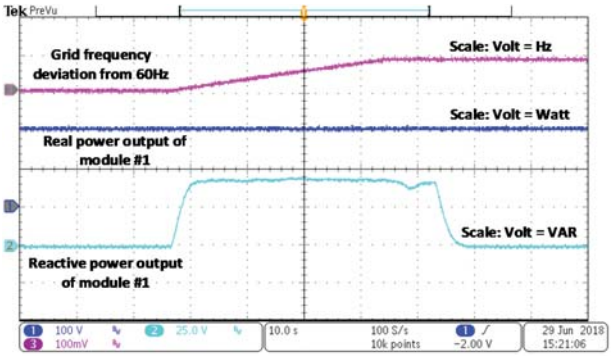

Fig. 7. Response of module #1 during a ramp increase in grid frequency from 60Hz to 60.1Hz.

2) Natural Correction of Reference Mismatch

To observe the system response for mismatch among power references, the three modules are subjected to real power reference change to 125W, 250W, and 175W, respectively from an initial identical reference of 250W.

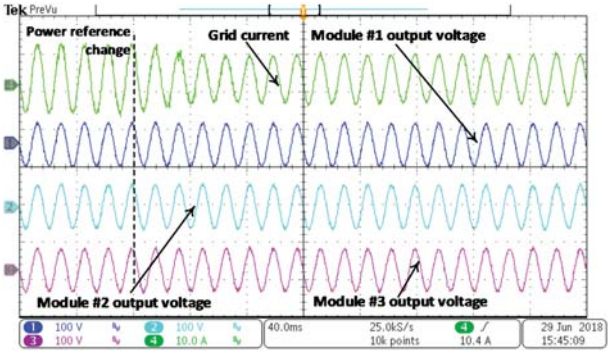

Fig. 8. System response as power reference changes from identical 250W to 125W, 250W, and 175W for modules #1, #2, and #3 respectively.

Despite the reference mismatch, the AC output voltage waveforms of the modules exhibit minimal change which is very difficult to judge from the scope. Fig. 9 shows the output voltage amplitudes for the same simulation condition but done in Simulink instead of OPAL RT. The deviations of the module output voltage amplitudes from their initial values are very small.

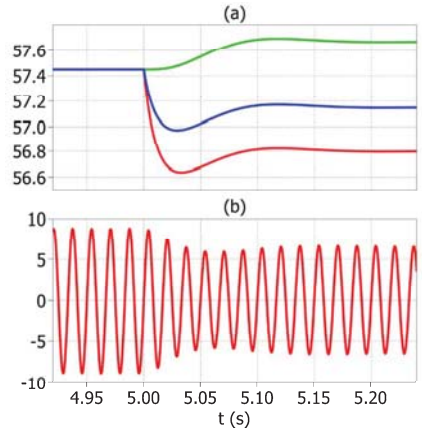

Fig. 9. Almost uniform power sharing by modules with reference mismatch: (a) Module output voltage amplitudes (V), (b) grid current (A).

The real power outputs from the modules settle to 183W, 186W, and 184W, respectively, which shows that even with large mismatches in power references the total power is shared among the modules almost equally.

It is to be noted that the controller forces equal power sharing among the modules despite different references due to a large value of D_v and (7) allows a non-zero steady state error between $P_{ref,k}$ and P_k. However, for AC-stacked PV application an MPPT controller dynamically generates $V_{DCref,k}$ to ensure operation at the maximum power point on the $I-V$ curve of the panel at the current solar irradiance on the panel. The integral part of MPPT controller ensures desired power flow which can be different for each modules.

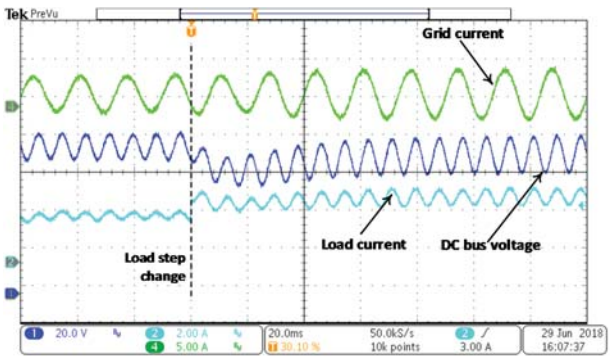

Fig. 10. Common DC bus voltage response to load step change.

C. Controller Evaluation with DC Bus Voltage Tracking

The three-module system described in the preceding subsection is modified to evaluate the controller performance with DC bus voltage tracking. The outputs of all three modules are connected

to a common DC bus with an energy storage capacitor of $500\ \mu$F. The isolated DC-DC stage is operated with a fixed voltage gain of 1. The DC bus voltage reference is set at 80V. Fig. 10 shows the common DC bus voltage response to a step change in the DC load. The change in load is reflected in the grid current. A proportional gain $K_p = 2.45$ and integral gain $K_i = 28.5$ have been used.

VII. Conclusion

The proposed control method can be utilized to stack low voltage rated voltage source converters in series configuration to reach higher voltage on the AC side. The complete decentralized nature of the controller enables plug-and-play type functionality of low voltage modules for medium or high voltage applications such as SSTs/PETs or industrial motor drives without the need for communication among modules or a central synchronization signal. Using the proposed control method, AC-stacked PV inverter systems can be made in a more robust and reliable way removing single point of failure from the system. The homogeneity of hardware and software of the modules can be leveraged to achieve unrestricted scalability and redundancy in any AC-stacked system.

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