Cascaded Active Neutral Point Clamped and Flying Capacitor Inverter Topology for Induction Motor Drives Applications

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***Abstract*—This paper proposes a novel multilevel architecture using active neutral point clamped inverter cascaded with a flying capacitor inverter to form a multilevel inverter topology with higher number of voltage levels for induction motor drives. All the capacitors in the topology can be balanced irrespective of any modulation index or power factor. This topology can be generalized for higher number of voltage levels. The front end DC sources required are of very low value and it can be further halved when using a reconfigured six phase induction machine for higher power. The low value DC sources can be stacked battery cells, hence the topology can find extensive applications in electric vehicles. Detailed experimental results are shown for the steady state and transient operations of the inverter. The proposed topology will be a viable scheme for high power applications.**

***Index Terms*—active neutral point clamped, flying capacitor, capacitor balancing, six phase, induction motor**

I. Introduction

Multilevel inverters (MLI) have remained popular for quite long for high power applications [1] [2]. The main reasons for it being the use of low voltage switches, low switching frequency requirement, better waveform quality, low dv/dt and better electro magnetic compatibility. The basic multilevel topologies are the neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) inverters. NPC was first introduced in [1]. It introduced additional pole voltage level, '0' with respect to the capacitor mid point, compared to the conventional 2-level inverters. NPC inverters have become quite popular for medium voltage drives but NPC suffered from DC link balancing problem [3] [4]. It can be shown that there is a limit on the balancing of these capacitors considering the load power factor and the modulation indices. Therefore increasing the number of voltage levels in diode clamped converters is not practical. Also the large number of power diodes for higher number of voltage levels is another disadvantage. Another issue with the NPC topology is the unequal loss distribution among the switches. To improve this, active NPC topologies (ANPCs) were introduced where the power diodes are replaced with active switches so that it can now control the current flow during the pole voltage level,'0' (with respect to the capacitor mid point) and equalize the semiconductor losses [5] [6]. The FC inverters are another class of MLCs where the additional voltage levels are introduced using charged capacitors. The voltages across these capacitors have to be maintained through proper voltage balancing algorithm when load current flows through them. Balancing these floating capacitor voltages is quite involved as the number of voltage levels increases and also the number of electrolytic capacitors involved in the inverter topology also drastically increases. The electrolytic capacitors are the weakest link in any converters and its quantity should be kept to the minimum [7]. Another class of MLCs are the cascaded H-bridge converters which have the least component count among the MLCs. It has become popular for integrating multiple power sources and feeding with grid. For drives application, the use of CHBs with higher number of voltage levels requires more number of isolated DC sources. The isolated DC sources with its bulky transformers increase the weight, size and cost of the system. Therefore its use in drives applications is limited.

Several combinations of these basic MLC topologies have been proposed in literature for generation of higher number of voltage levels [8] [9]. Cascade connections of FC and multiple CHBs with 5-level [10] and 17-level [11] have been reported in literature. Some of them suffer from limitations in the modulation indices for balancing the floating capacitors in them. Some literature used stacking of the cascade combination of FC and CHB using selector switches to generate higher number of voltage levels. For drives applications, the limitation on modulation indices will restrict the speed range of operation of the induction motor. Research has moved on from hexagonal space vector (SV) structure to dodecogonal SV structure to eliminate the 5th and 7th harmonic component and suppress the higher order harmonics.

Instead of using 3-phase Induction motors, if a reconfigured 6-phase machine is used such that the 180 deg opposite windings are paralleled with appropriate polarity, the DC link voltage requirement for driving this motor is reduced to half. In addition to this, the MLC will have reduced DC link voltage requirement. therefore the DC sources can be replaced

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with stacked battery cells and finds extensive application in electric vehicles (EV). This also allows the use of low voltage MOSFETs, which will have better efficiency.

II. Operation of the Cascaded ANPC and FC Inverter Topology

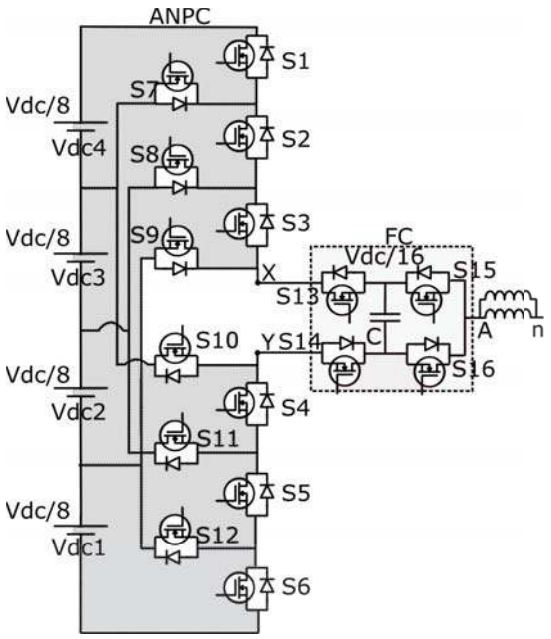

Fig. 1. Cascaded ANPC-FC 9-level multilevel inverter topology for phase A

A. Reconfigured 6-phase windings as 3-phase induction machine

This section discusses about reconfiguring a symmetric six phase (windings placed 60^o apart) winding pattern to a three phase winding. As shown in Fig. 3(a), the six windings a_1-a_2, c_3-c_4, b_1-b_2, a_3-a_4, c_1-c_2, b_3-b_4, are 60^o apart. It can also be noticed that there are three winding pairs which are exactly 180^o opposite to each other which are a_1-a_2 and a_3-a_4, b_1-b_2 and b_3-b_4, c_1-c_2 and c_3-c_4. For a six phase machine, these 180^o opposite windings need to be fed with 180^o opposite phase voltages. It needs additional power electronic components to feed the windings with opposite phase volatges. The 180^o opposite windings can be connected in parallel in such a way that the windings still see opposite phase voltages. For this, the windings have to be connected as shown in Fig. 3(b) that is for the A and A' phases, terminals a_1 and a_4 are connected together and the other ends, a_2 and a_3 are also connected. Similar configuration for the other 180^o opposite phases. It should be noted that for a machine with six phase windings, the DC link voltage requirement (Vdc) at the front end is half that of the three phase winding for supplying the same power. Here Vdc is the DC link voltage required for a conventional two level inverter. This reduces the voltage ratings of the power electronic components of the inverter. In this case of three phase windings obtained by paralleling the opposite phases, the current through the devices is double that of the each winding current. In Fig. 3(b), I_{a1a2} is half that of the phase current I_a.

B. Operation of ANPC as selector switch

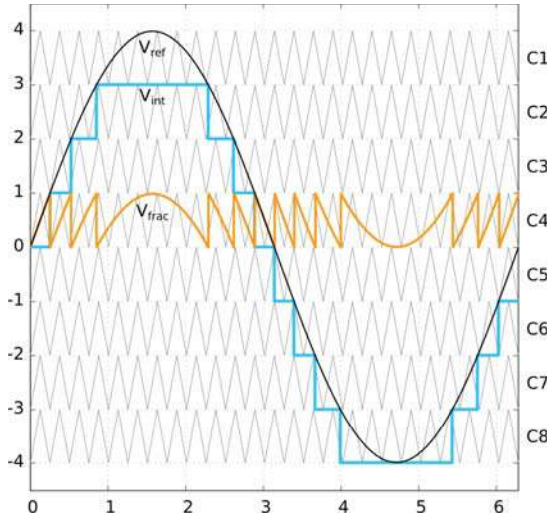

Fig. 2. Level shifted carrier based space vector PWM for 9-level inverter.

This section describes the operation of the ANPC (Fig. 1) as selector switches, that is to connect the FC to the appropriate DC source during the operation of the inverter. Level shifted carrier based PWM (Fig. 2) is used for the implementation [12] [13]. The modulating signal is scaled from 0 to 8 and is divided into 4 equal vertical sections. During each of these sections, the FC has to be connected to each of these DC sources to generate the nine pole voltage levels. To connect the FC to the bottom DC source, Vdc1, the switches S9, S4, S5 and S6 have to be ON. For connecting to Vdc2, the switches S8, S3, S4, S5 and S12 have to be ON. Similarly for Vdc3 and Vdc4. the switches S7, S2, S3, S4, S11 and S1, S2, S3, S10 have to be ON respectively. It should be noted that these switches are switching at low frequency and have low voltage blocking requirements. Since these switches are used only for selecting the appropriate DC sources, they are called here as selector switches. Also, due to the operation of the selector switches, the voltage, V_{XY} is always maintained at Vdc/8.

C. Operation of the ANPC with FC and generalization

This section explains the FC operation with ANPC. FC can generate three pole voltage levels, 0, Vdc/16, Vdc/8 with respect to Y (V_{AY}), if the voltage maintained across the capacitor, C is maintained at Vdc/16, which is explained in the next section. The generation of the nine pole voltages can be explained as follows. When the FC is connected to Vdc1, the pole voltage, V_{AN} can have values, 0, Vdc/16, 2Vdc/16. When the FC is connected to Vdc2, the pole voltage, V_{AN} can take values which are Vdc/8 added with the above values which are, Vdc/8, 3VDC/16 and 4Vdc/16. Similarly when the FC is connected to Vdc3, V_{AN} can take values, 4Vdc/16, 5Vdc/16

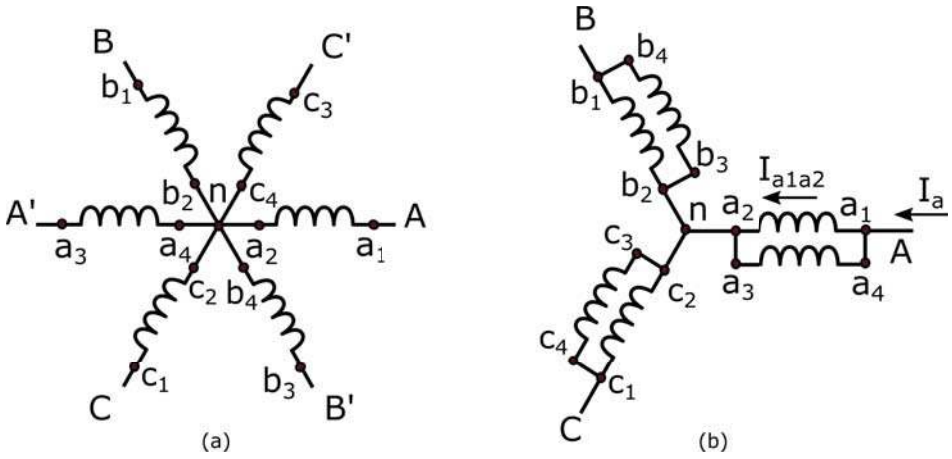

Fig. 3. Reconfiguring a symmetric six phase winding (Fig. 3(a)) as a three phase winding (Fig. 3(b)).

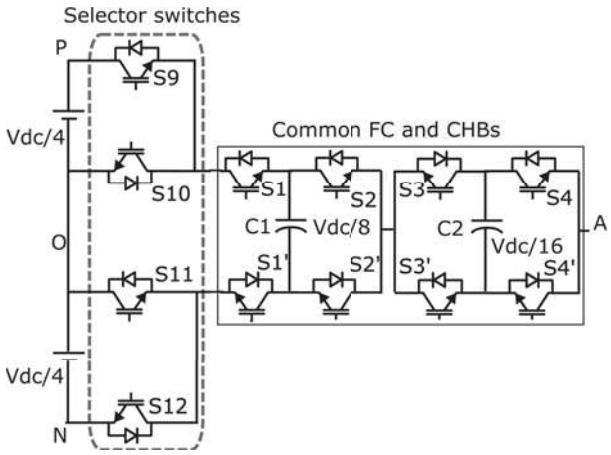

Fig. 4. Cascaded 3-level ANPC-FC-CHB multilevel inverter topology for phase A

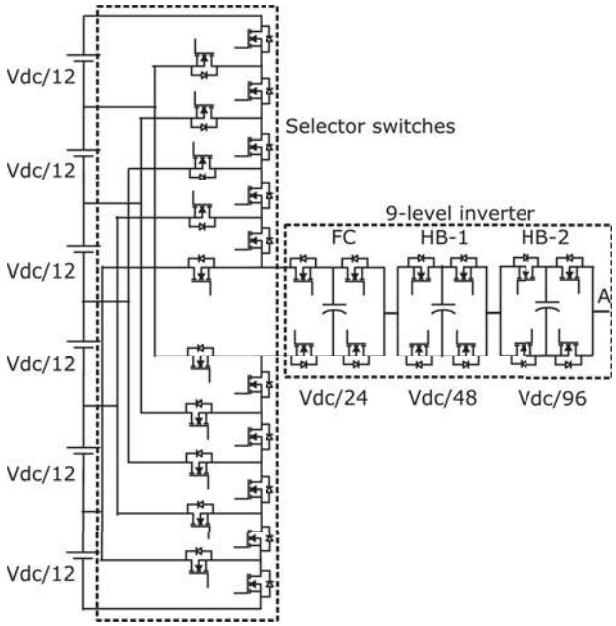

Fig. 5. Cascaded 7-level ANPC-FC-CHB multilevel inverter topology for phase A

and 6Vdc/16. Finally when the FC is connected to Vdc4, the values V_{AN} can take are 6Vdc/16, 7Vdc/16 and 8Vdc/16. Hence this topology can generate the nine pole voltage levels. This structure can be generalized to obtain still higher number of voltage levels using a higher level ANPC. A 9-level inverter developed by using a 3-level ANPC and cascade combination of FC and CHB as shown in Fig. 4. Also the FC can be cascaded with multiple CHBs to generate much higher number of voltage levels as shown in Fig. 5. In this, the DC voltage requirement at the front end is only Vdc/12, hence stacked battery cells can be used along with low voltage MOSFETs and finds applications in electric vehicles.

III. Capacitor voltage balancing

For proper operation of the multilevel converter, the capacitor voltage has to be maintained at Vdc/16. This can be done using the switching state redundancies of the available pole voltage levels. An example of the capacitor voltage balancing is shown in Fig. 6 for balancing the capacitors for pole voltage of 3Vdc/16 (V_{AN}). Fig. 6(a) shows the charging of capacitor for the positive direction of current from the inverter output, 'A' to the machine neutral, 'n' using the switching state 0011100100011001 where '1' denotes the switch is ON and '0' indicates the switch is OFF. This switching state generates Vdc/8 +Vdc/8-Vdc/16=3Vdc/16 For discharging the capacitor, the switching state, 0011100100010110 is used as shown in Fig. 6(b), where the pole voltage generated is again Vdc/8+Vdc/16=3Vdc/16. The capacitor is balanced within a switching cycle and is independant of any load power factor and modulation indices. The capacitor can be sized based on the switching frequency, peak of the load current and the allowable voltage deviation. The tolerance band provided for all the flying capacitor voltages are 2% around the reference values. The capacitance value, C is

TABLE I
SWITCHING STATE REDUNDANCIES FOR THE POLE VOLTAGES AND THEIR EFFECT ON THE CAPACITOR VOLTAGES.

S.No	Switch States	V_{AN}	I_a	C
1	0001110010000101	0	+	U
2	0001110010001001	Vdc/16	+	C
3	0001110010000110	Vdc/16	+	D
4	0001110010001010	Vdc/8	+	U
5	0011100100010101	Vdc/8	+	U
6	0011100100011001	3Vdc/16	+	C
7	0011100100010110	3Vdc/16	+	D
8	0011100100011010	Vdc/4	+	U
9	0111001000100101	Vdc/4	+	U
10	0111001000101001	5Vdc/16	+	C
11	0111001000100110	5Vdc/16	+	D
12	0111001000101010	3Vdc/8	+	U
13	1110000001000101	3Vdc/8	+	U
14	1110000001001001	7Vdc/16	+	C
15	1110000001000110	7Vdc/16	+	D
16	1110000001001010	Vdc/2	+	U

Note: 'U' - Unaffected, 'C'- Charging, 'D ' - Discharging. '+' indicates current flow from inverter pole 'A' to machine neutral 'n'. Switch State is defined as (S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16). '1' indicates switch is ON and '0' indicates switch is off.

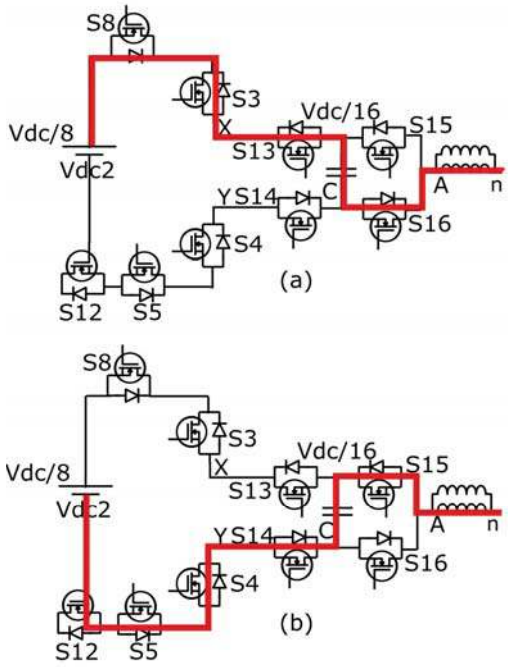

Fig. 6. Capacitor voltage balancing for pole voltage, 3Vdc/16 of phase A

decided by $C = I_p T_s / \Delta V_c$, I_p is the peak load current, ΔV_c is the peak to peak voltage ripple and T_s is inverter switching time. Capacitance value of 2200μF is selected in the experiment.

IV. EXPERIMENTAL RESULTS

The laboratory prototype for the 9-level inverter is developed for driving a reconfigured 6-phase induction motor. Level shifted PWM is implemented in TMS320F28335 DSP. The capacitor voltage is sensed using the ADC module in the DSP.

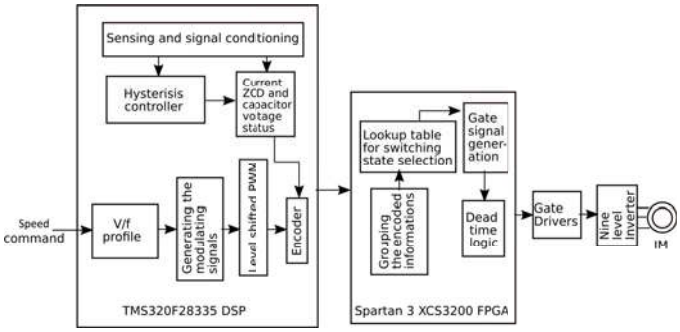

Fig. 7. Implementation block diagram of the 9-level inverter topology.

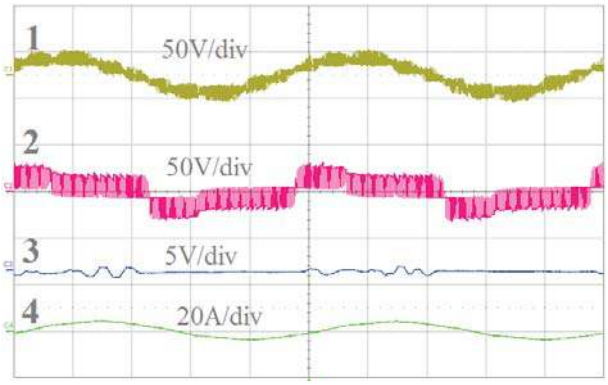

Fig. 8. 10 Hz operation, 1. Phase voltage (V_{An}), 2. Pole voltage (V_{AN}), Capacitor voltage (Vc), Phase current (I_a), x-axis: 20ms/div.

The capacitor voltage, pole voltage and the PWM information are transfered to the Spartan 3 XCS3200 FPGA, which selects the appropriate switching state and passed to the inverter through the gate driver as shown in Fig. 7. The induction motor is driven by the inverter using V/f control scheme for different speed operation from 10Hz to 45Hz operation. The phase voltage, pole voltage, capacitor voltage and phase current for 10Hz, 20Hz, 30Hz and 45Hz operation are shown in Figs. 8, 9, 10, 11 respectively. All the waveforms are taken at no load which shows the worst case current ripple. The

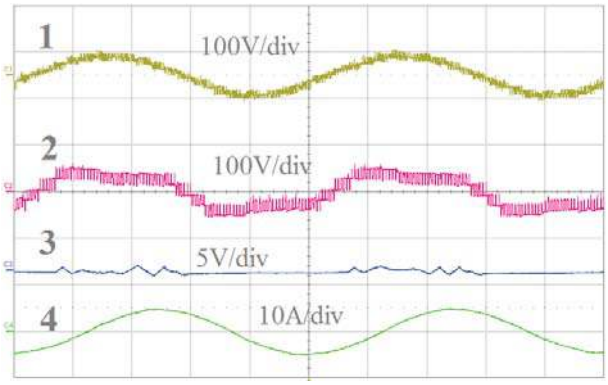

Fig. 9. 20 Hz operation, 1. Phase voltage (V_{An}), 2. Pole voltage (V_{AN}), Capacitor voltage (Vc), Phase current (I_a), x-axis: 10ms/div.

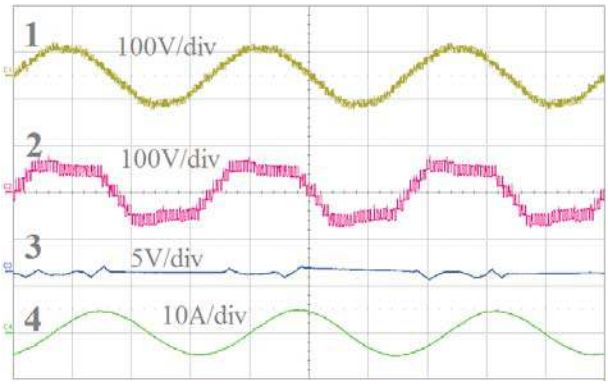

Fig. 10. 30 Hz operation, 1. Phase voltage (V_{An}), 2. Pole voltage (V_{AN}), Capacitor voltage (Vc), Phase current (I_a), x-axis: 10ms/div.

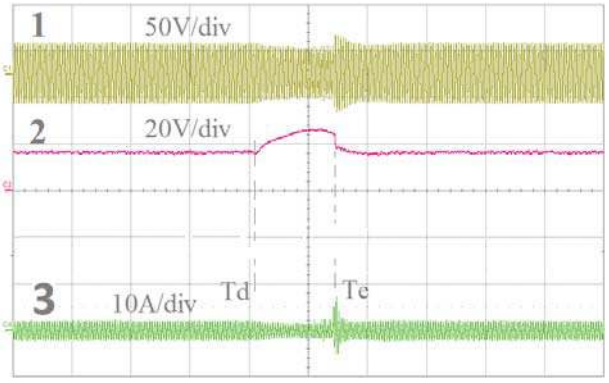

Fig. 13. Intentional capacitor unbalancing, 1. Phase voltage (V_{An}), 2. Capacitor voltage (Vc), Phase current (I_a), x-axis: 500ms.

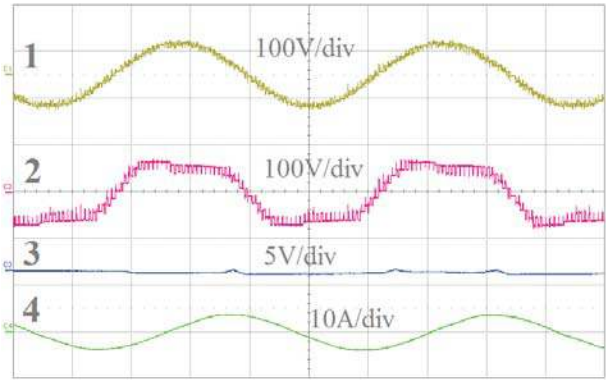

Fig. 11. 45 Hz operation, 1. Phase voltage (V_{An}), 2. Pole voltage (V_{AN}), Capacitor voltage (Vc), Phase current (I_a), x-axis: 5ms/div.

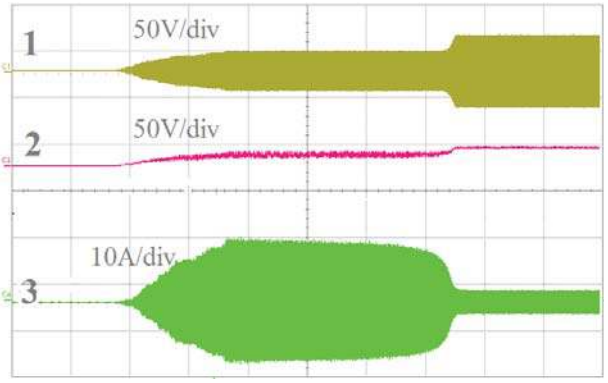

Fig. 14. Motor starting, 1. Phase voltage (V_{An}), 2. Capacitor voltage (Vc), Phase current (I_a), x-axis: 500ms/div.

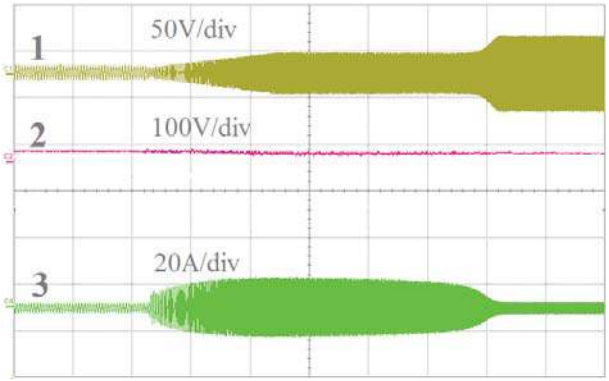

Fig. 12. Motor acceleration, 1. Phase voltage (V_{An}), 2. Capacitor voltage (Vc), Phase current (I_a), x-axis: 500ms/div.

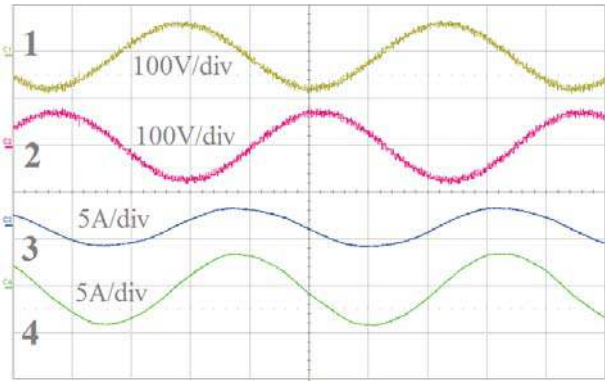

Fig. 15. 1. Motor Phase voltage (V_{a1a2}), 2. Motor Phase voltage (V_{a3a4}), 3. Winding current (I_{a1a2}), 4. Phase current (I_a) for phase A. x-axis: 5ms/div

capacitor voltage ripple shown in trace-3 of the figures shows the capacitor voltage which are tightly controlled using the capacitor voltage balance algorithm described in section-III. Also from 10Hz to 45Hz operation, the pole voltage levels increase from 3 to 9. To test the transient stability of the capacitor voltage balancing algorithm, the motor is accelerated from 10Hz to 45Hz in 4s as shown in Fig. 12. The trace-2 shows the capacitor voltage which are tightly controlled. The stability of the capacitor voltage balancing algorithm is shown in Fig. 13 where the balancing algorithm is disabled at Td and then re-enabled at Te. The capacitor voltage initially deviates from the reference and then on re-enabling immediately tracks the reference. No precharging of the capacitor voltage is needed since the balancing algorithm itself takes care of the capacitor voltage build up as shown in Fig. 14. Fig. 15 shows the motor phase voltage waveforms applied to the 180 deg

opposite windings a1 -a2 and a3 -a4 in traces 1 and 2 which are also 180deg opposite. Trace-3 shows the current through the winding a1 -a2 , Ia1a2 which is half that of the motor phase current, Ia shown in trace-4. The FFT plot of the inverter

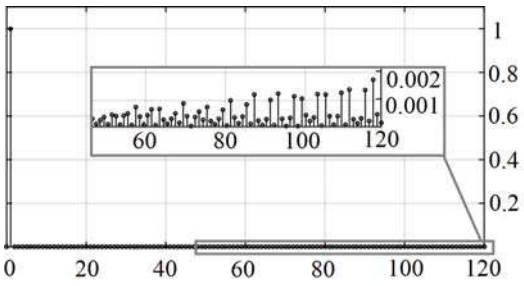

Fig. 16. 10Hz, THD: 2.28%

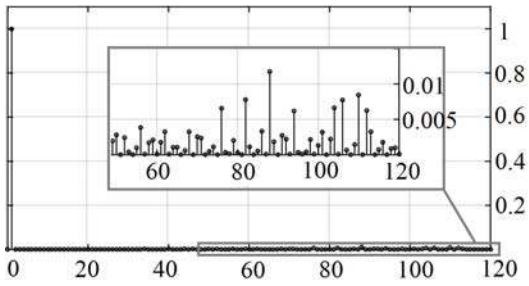

Fig. 17. 20Hz, THD: 2.03%

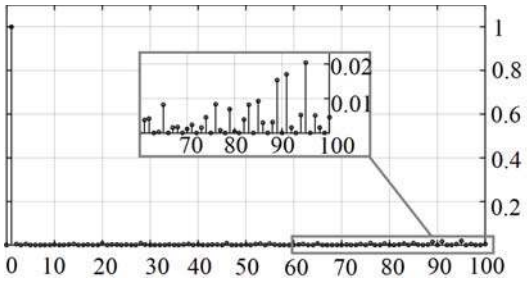

Fig. 18. 30Hz, THD: 1.6%

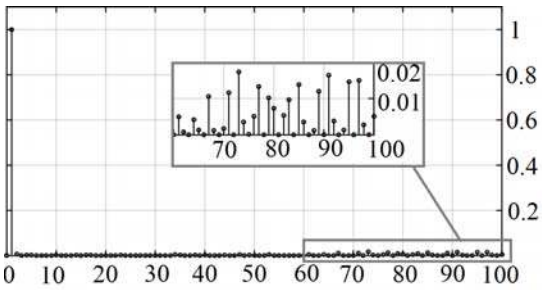

Fig. 19. 45Hz, THD: 1.02%

output voltages (V_{An}) at various frequencies of operation is given in Fig. 16 - Fig. 19 where the fundamental amplitude is normalized to 1.

V. Conclusion

This paper describes a simple configuration of a six phase IM by paralleling the opposite windings and driving the reconfigured machine through a nine level inverter topology. Six phase machine itself enables the use of low voltage devices for supplying the same power compared to a three phase machine. Also the ANPC-FC-CHB inverter uses low voltage devices for its operation. So driving a reconfigured six phase machine with a stacked inverter further reduces the device voltage ratings. On using higher level ANPCs, the DC voltage supply requirement at front end reduces further and they can be replaced with stacked battery cells. Also by cascading with more CHBs, more voltage levels with lower voltage devices can be achieved. Using low voltage devices (MOSFETs) and stacked battery cells at the front end makes it a suitable option for electric vehicle applications. Detailed experimental results with both steady state and transient operation ensures that this novel combination of reconfigured six phase machine driven using a ANPC-FC-CHB inverter will be viable scheme for high power applications.

REFERENCES

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sept 1981.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[3] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, July 2010.

[4] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source pwm inverters," *IEEE Trans.Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar 2000.

[5] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. 2005 IEEE Power Electron. Special. Conf.*, June 2005, pp. 2296–2301.

[6] T. Bruckner, S. Bernet, and H. Guldner, "The active npc converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, June 2005.

[7] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters ;an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sept 2014.

[8] P. Rajeevan, K. Sivakumar, K. Gopakumar, C. Patel, and H. Abu-Rub, "A nine-level inverter topology for medium-voltage induction motor drive with open-end stator winding," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3627–3636, Sept 2013.

[9] J. Li, S. Bhattacharya, and A. Huang, "A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Trans.Power Electron.*, vol. 26, no. 3, pp. 961–972, March 2011.

[10] P. Roshankumar, P. Rajeevan, K. Mathew, K. Gopakumar, J. Leon, and L. Franquelo, "A five-level inverter topology with single-dc supply by cascading a flying capacitor inverter and an h-bridge," *IEEE Trans.Power Electron.*, vol. 27, no. 8, pp. 3505–3512, Aug 2012.

[11] P. Kumar, R. Kaarthik, K. Gopakumar, J. Leon, and L. Franquelo, "Seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridges," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3471–3478, July 2015.

[12] R. Kanchan, M. Baiju, K. Mohapatra, P. Ouseph, and K. Gopakumar, "Space vector pwm signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," *Electric Power Applications, IEE Proc. Electr. Power Appl.*, vol. 152, no. 2, pp. 297–309, March 2005.

[13] B. McGrath and G. Holmes, "Multicarrier pwm strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug 2002.