Mobile Utility Support Equipment based Solid State Transformer (MUSE-SST) for MV Grid Interconnection with Gen3 10 kV SiC MOSFETs

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***Abstract*—With the increasing maturity of Silicon Carbide (SiC) semiconductor devices at medium voltage (MV) level, high switching frequencies and low conduction losses in MV applications is possible. Higher switching frequency operation enables the reduction in size and weight of transformers. In an application such as MV-MV or MV-LV grid-interconnection, a solid state transformer offers a multitude of advantages compared to conventional transformers. A reduction in size and weight, in addition to having active and reactive power flow control have made SSTs a lucrative replacement to conventional low frequency (LF) transformers. Lower conduction losses exhibited by SiC devices (as compared to their silicon counterparts) have made it possible to achieve similar efficiencies as compared to conventional LF transformers. This paper aims at providing an overview of a MV MUSE-SST topology. A brief idea on control and monitoring is also provided. Practical design considerations that are required to build a MV system is provided to aid researchers in designing converters for MV applications. The protection aspects of the MV MUSE-SST system is also highlighted. Basic experimental results for the gate driver is also shown. Initial testing results with the Gen3 10 kV SiC MOSFETs and the challenges associated with it are also discussed. This research aims at being a building block for implementation and testing of the medium voltage converter systems.**

Keywords*—*10 kV SiC devices, gate driver, grid interconnection, medium voltage, MUSE-SST, solid-state transformer, XHV-6 modules, XHV-9 modules

I. Introduction

An increased penetration of renewable energy sources like PV and wind has catalyzed the need to modernize the conventional power distribution system [1]–[3]. MV solid-state transformers (MV-SSTs) serves as a lucrative replacement to conventional transformers, on account of their advantages over conventional low frequency (LF) transformers. Even though the conventional transformers, used in the distributed systems, have been used throughout the twentieth century, it incorporates a lot of downsides in itself. They are generally sensitive to harmonics, requires additional circuitry for protection and overloads, unable to control power flow, and performance under dc-offseted loads [4]–[6]. In addition, these transformers are often oil-cooled (raising environmental concerns) and bulky. This poses an issue regarding the ”mobile utility” of conventional transformers.

MV-SSTs addresses these concerns and provides suitable solutions for each of them. The MV SSTs are made possible due to the advent of wide-bandgap Silicon Carbide (SiC) devices [7]–[9]. With the high switching frequency operation of 10 kV SiC MOSFETs, it is now possible to reduce the size of the transformer required to convert the medium voltage to low voltage (typically from 4160 V to 480V). Traditionally, for distribution grids (up to 13.8 kV and 60 Hz), higher order multilevel converters (more than three level) have been used. Availability of high voltage blocking SiC devices have enabled power converters without the use of multilevel converters and complicated control strategies [7], [10]–[12]. In addition to the reduction in size, the MV-SST offers a multitude of advantages which includes

- Protection of load from power supply disturbances
- Controlling the power flow between different grid connections
- Limiting the fault currents i.e. protection against output short circuit
- Integration with energy storage units
- Maintaining the power factor
- Voltage harmonics and sag compensation
- Provide voltage regulation and communication capabilities

Fig. 1 illustrates the basic structural difference between the conventional low frequency (LF) transformers and medium frequency (MF) solid state transformers. The power electronics converter stages in the SST enables control over its full range. In addition to these advantages, the MV-SSTs incorporates a few downsides to it mainly in terms of reliability

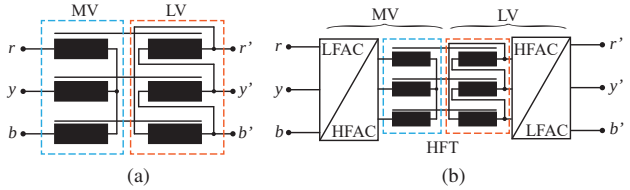


Fig. 1: Structural schematic of (a) a typical star-delta connected conventional LF transformer, and (b) a MV solid-state transformer. The galvanic isolation in the solid state transformer is provided by the high frequency transformer (HFT). LF represents low frequency which is typically at 50 Hz or 60 Hz, and HF represent high frequency which is typically 20-50 kHz. The increased frequency in the HFT leads to a reduction in size.

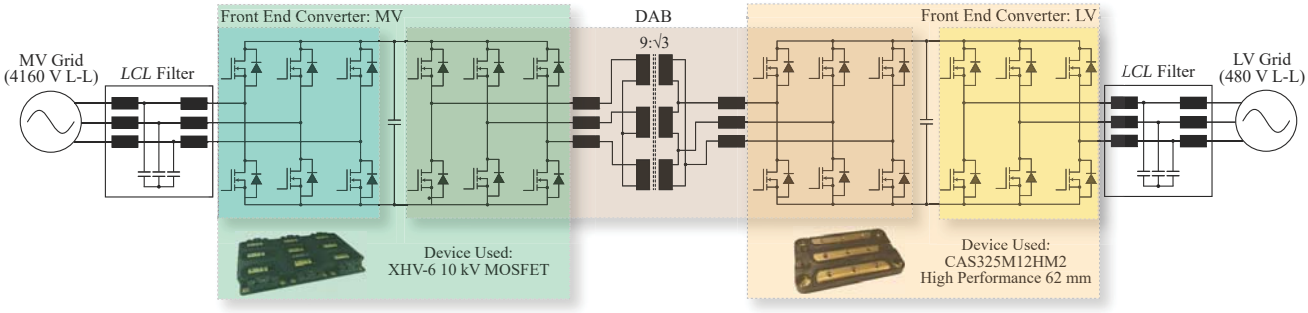


Fig. 2: Schematic of the hardware implementation of the overall system architecture. The MUSE-SST consists of three parts: MV AFEC, DAB and LV AFEC. In the actual system, the LCL filter has an additional $R_d - C_d$ damping.

and ruggedness. However, the study on the reliability is out of the scope of this paper.

This paper provides an overview for a MV MUSE-SST topology used for grid inter-connection. A brief idea on the control and protection of the system is also provided. In addition, practical design considerations, such as designing the gate drivers, magnetics, thermal solutions and other ancillary services needed for operation are also addressed. Since the 10 kV SiC devices are currently in its infancy, initial tests to validate the operation of these devices with the custom gate driver have been carried out. The working of the 10 kV SiC MOSFETs have been validated using double pulse tests, buck and boost operation. The detailed experimental setup with the working of the full system is currently under development.

The paper is arranged as follows. The operational overview is provided in Section II. The system architecture is explained in details in Section III. It is accompanied by a description of the MV and LV devices used for the converter system. The practical design aspects, including gate driver and thermal considerations are provided in Section IV. Section V describes the protection schemes used in the MUSE-SST converter system . Section VI gives initial test results carried out with the Gen3 10 kV SiC devices, and it is followed by conclusions and references.

II. Operational Overview of MUSE-SST

The MUSE-SST provides a concept for the replacement of a conventional 4.16 kV to 480 V LF distribution transformer. While the detailed quantitative comparison between the two, is beyond the scope of this paper, the theoretical advantages offered by the MV-SST makes it a viable and lucrative option in distribution systems.

A. Reactive Power Capability

It is assumed that a 1 p.u VA load is connected to the system with a real power of 0.8 p.u and a reactive power of 0.6 p.u. The conventional transformer, in this case, supplies the load and draws the same amount of real power from the MV grid which might result in a voltage dip and an increased line loss at the MV grid. In contrast, the MUSE SST is capable of handling the load at the LV feeder without drawing any reactive power from the MV grid. It draws 0.8 p.u real power from the MV grid and injects the 0.6 p.u. reactive power from the LV grid and thus decreases the line loss and avoids the voltage sag. Fig. 3 shows the reactive power capability of the MUSE-SST when compared to the conventional transformer.

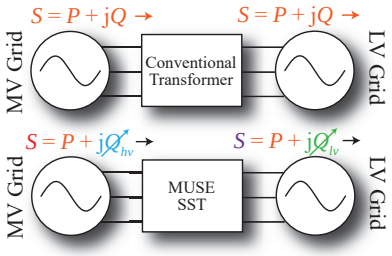


Fig. 3: Power flow direction of a conventional transformer and MUSE-SST. The conventional transformer draws both the active and reactive power from the MV grid where as the MUSE-SST is capable of supplying reactive power locally.

III. System Architecture of MUSE-SST

A schematic of the implementation of the overall system architecture is provided in Fig. 2. In this system, a grid interconnection between a 4.16 kV (L-L) - 60 Hz grid to a 480 V (L-L) - 60 Hz is studied. The voltage transformation is handled by the three-stages- Front-End Converter: MV (MV:AFEC), Dual Active Bridge (DAB) and the Front-End Converter: LV (LV:AFEC). The system consists of LCL with $R_d - C_d$ filters on both the grid-connected converters.

A. Topology Selection

In the literature, three level neural point clamped (NPC) topology is proposed for similar applications using 15 kV IGBTs [8]. The three-level NPC topology was adopted due to the increased failure of the 15 kV IGBTs at higher blocking voltages. With the development of Gen3 10 kV MOSFETs, a blocking voltage of around 8 kV on a single MOSFET can be used without device failure considerations (at the initial stage). A 3-phase, 2-level topology is adopted for MUSE-SST due to its simplicity and limited failure modes. In this topology, the 3-phase 4.16 kV grid voltage is rectified by the

inverter (MV:AFEC), followed by the DAB (which acts as a dc-dc and isolation stage) and a LV dc-ac inverter (LV:AFEC). The MV stage is isolated from the LV stage using a high frequency medium voltage transformer, operating at 20 kHz. This topology is enabled by Wolfspeed 10 kV, 75 A XHV-6 modules on the primary side and CAS325M12HM2 Wolfspeed modules on the low voltage (LV) side [13].

B. 10 kV XHV-6 Modules

Fig. 4 shows the 10 kV XHV-6 module from Wolfspeed. Each submodule consists of a half-bridge, so that the switching inductance can be kept to a minimum value. In the module, by custom design, the first submodule is populated and the other two submodules are kept open due to some design considerations. Table I gives the basic characteristics of these XHV-6 modules. Six dies are connected in parallel for each MOSFET position to increase the current carrying capacity. Each die is capable of blocking 10 kV and carry a current of around 15 A [14]. Fig. 5 shows the internal schematic of the XHV-6 module.

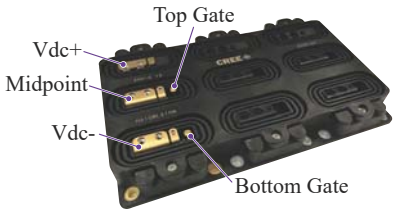


Fig. 4: 10 kV SiC MOSFET packed in a XHV-6 module from Wolfspeed. Only, the first sub-module is populated and the other two sub-modules are kept un-populated.

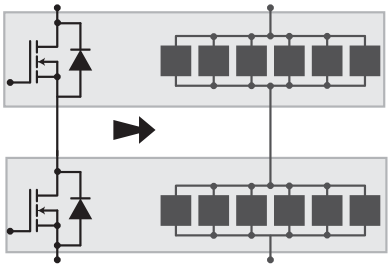


Fig. 5: Internal schematic of the 10 kV SiC MOSFET packed in a XHV-6 module from Wolfspeed. This shows only the first submodule since the other submodules are not populated.

TABLE I: Parameters of Gen3 10 kV XHV-6 module

Parameter	*Value*
Topology	Half-bridge
Blocking voltage	10 kV
Maximum Current (at 25oC)	75 A
Maximum Current (at 125oC)	35 A (calculated)
On-state Resistance (at 25oC)	56 mOhm
On-state resistance (at 125oC)	168 mOhm

C. Control Implementation

The control strategy for the MV and LV inverter is aimed at maintaining the corresponding dc-link voltages at 7200 V and 800 V respectively. The dc-link voltages are chosen according to the minimum dc-link voltages required for power transfer with space vector modulation. Fig. 6 gives the control strategy of the entire system. A three-phase synchronous-PLL is used to calculate the voltage angle. The dc-link voltage controller generates the d-axis reference (i^*_{sd}) and the q-axis reference is user controlled. A PI current controller is used as an inner current control loop to control the current.

The control of DAB is done in a straightforward manner. Since, the dc-link voltage is maintained on either side of the DAB, only a phase angle control is implemented for the DAB. This method is simple and easy to implement. However, there are issues associated with in respect to transformer saturation. To avoid the transformer saturation, a rate limiter is implemented at the phase angle output which does not allow the phase angle to change abruptly. This makes the control slower as compared to other techniques. However, this helps in avoiding current sensing for the DAB currents and consequently, does not require any fast analog-to-digital conversion systems (ADCs).

Another control option is programmed in the control to control the LV dc-link voltage through the DAB and run the LV AFEC in an open loop configuration. This is used for testing the MUSE-SST and to use the converter configuration to directly feed into a load (when the LV grid is absent).

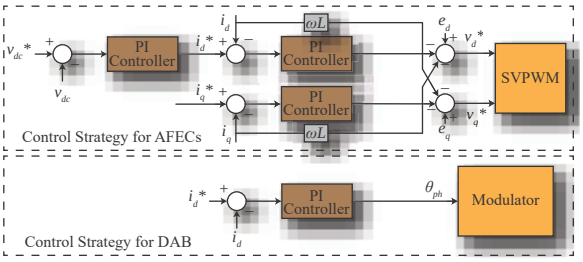


Fig. 6: Control block implemented for MUSE-SST. The MV and the LV AFEC use a similar control technique where a conventional PI controller is used to maintain the dc-link voltage on the MV and the LV side.

IV. Practical Design Considerations of MUSE-SST

Implementation of a MV converter calls for a number of design considerations. This section elaborates on the major factors required for implementation of the MUSE-SST system.

A. Gate Driver Designs

The gate driver design is one of the most important criteria for driving MV SiC MOSFETs. The major difference in designing the gate drivers arise from the fact that the dv/dt exhibited by MV devices is in orders of 50-70 kV/µs [15]. This necessitates proper design of parasitic capacitances through the common mode paths. In the gate driver, the major common mode path

is through the isolation transformer and the signal path (optical fiber in most cases). The optical fiber offers very low isolation capacitance, and most of the common mode current flows through the isolation transformer as shown in Fig. 7. The magnitude of the common mode (CM) current (I_{cm}) is directly affected by the dv/dt and parasitic capacitance (C_p)

$$i_{cm} = C_p \frac{dv}{dt} \tag{1}$$

The gate driver (especially the isolation) should be designed considering these main parameters:

- High isolation voltage between primary and secondary
- Low coupling capacitance between primary and secondary
- Small, optimized footprint while maintaining the insulation standards

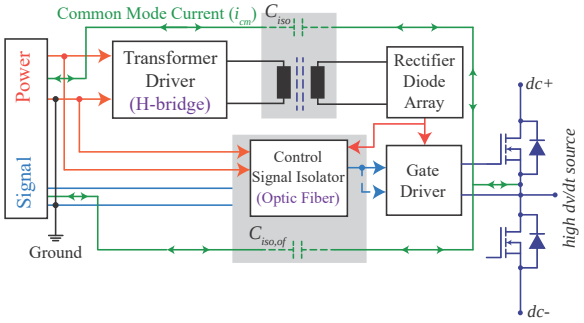


Fig. 7: Common mode current paths in the MV gate driver.

Fig. 8 shows the custom made gate-driver for MUSE-SST. The gate driver transformer is designed to have a minimal parasitic capacitance for driving the 10 kV SiC MOSFETs with such high dv/dt. The isolation capacitance of the designed gate driver is measured to be around 2 pF. In practice, a trade-off has to be made between the size and the coupling capacitance. Fig. 9(a) and Fig. 9(b) validate the operation of the gate driver by double pulse tests at 7.2 kV and 7.5 kV dc-link voltage, respectively. In addition to the basic requirements, additional

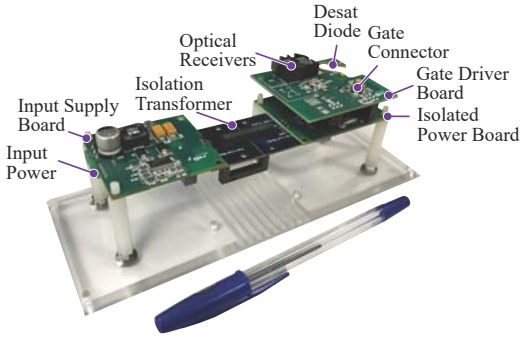


Fig. 8: Designed gate driver for driving 10 kV SiC MOSFETs in the high voltage side of MUSE SST. The overall dimensions are 6 in $\times$ 2 in $\times$ 1.5 in.

features should be added in order to have continuous and reliable operation. A short circuit feature is provided in the gate driver which is explained in details in the following sections. The interface between the gate driver and control board is done through optical cables which has better common mode performance.

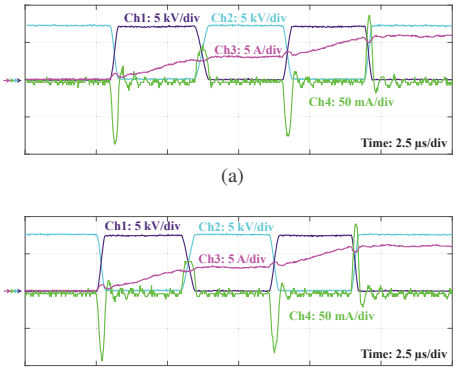


Fig. 9: Double pulse tests to validate the gate driver operation at (a) 7.2 kV, and (b) 7.5 kV dc-link bus voltages. The common mode currents through the gate driver can be observed. (Ch1: Voltage across bottom device; Ch2: Voltage across top device; Ch3: Current through the inductor; Ch4: Common mode currents through the gate driver circuit).

Similar to the MV gate drivers, the fabricated LV gate driver is shown in Fig. 10. The routing is carried out such that the high-speed signals have differential path (to increase the noise immunity). The gate driver is built with two isolated channels on the same PCB, which can drive both the devices on one CAS325M12HM2 independently. Gate power is isolated through galvanic isolation of a transformer and the gate signal is isolated through optical isolator. The interface between the gate driver and control board is done through optical cables which has better common mode performance.

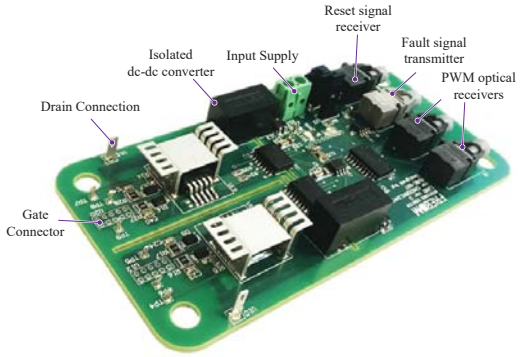
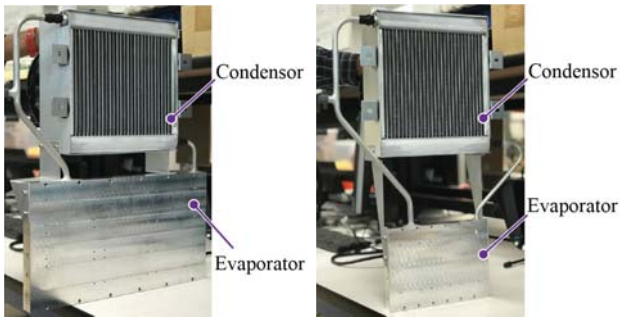


Fig. 10: Designed gate driver for driving CAS325M12HM2 in the low voltage side of MUSE SST. The overall dimensions are given by 5 in $\times$ 2.5 in $\times$ 0.75 in.

B. Thermal Solutions

Conventional heatsink designs include naturally cooled or forced air cooled fin-type heatsinks. MUSE-SST employs

a more efficient thermal solution which uses a loop thermosyphoon based product manufactured by Advanced Cooling Technologies (ACT) [16]. Heat generated by the power semiconductor devices during operation causes the liquid inside the evaporator to change its phase. This, combined with the condensation of liquid in the condenser, generates a gravitational pressure imbalance which maintains the fluid circulation between the condenser and evaporator [16]. Fig 11(a) and Fig. 11(b) shows the thermal solutions for both the MV and the LV side assembly, respectively. The MV heatsink and the



(a) (b)

Fig. 11: Loop thermosyphoon used for cooling the power semiconductor devices for (a) MV power devices, and (b) LV power devices.

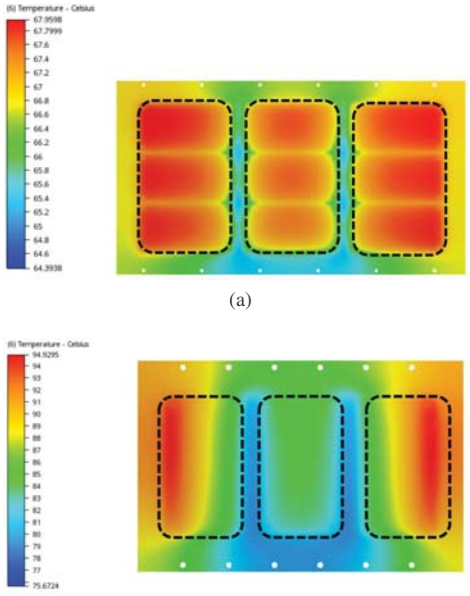
LV heatsink are designed to handle up to 2 kW of power losses for a temperature rise of 40°C and 70°C respectively. The heatsinks are over designed for MUSE-SST application in order to maintain a significantly lower junction temperature, and for repeatable use for higher power converters. Thermal simulation results showing the temperature distribution of the evaporator assembly for both the MV and the LV side is shown in Fig. 12(a) and Fig. 12(b), respectively. A maximum power dissipation of 2 kW is taken for both the evaporators. The maximum cold plate temperature of the MV evaporator reaches around 68°C. A similar analysis on the LV evaporator shows the maximum baseplate temperature to be around 95°C. Combining these results with the thermal resistance of the module, the junction temperature is found to be maximum 85°C for the MV power devices and 112°C for the LV power devices, which is within the specified limits.

C. High Frequency Magnetics Design

The practical design of the high frequency magnetics is becomes a challenge for the MV SiC MOSFETs due to the high dv/dt associated with these devices. The parasitic capacitances across the filter inductors and the high frequency transformer leads to an additional current [17]. The paths for these currents is shown in Fig. 14. The common mode current flows through the devices and cause additional switching losses. Fig. 13 shows the effect of the parasitic capacitance of the inductor on the current waveform.

V. Protection Aspects of MUSE-SST System

In order to protect the MUSE-SST system from abnormal and fault conditions, various protection schemes are introduced in



(a)

(b)

Fig. 12: Thermal simulation results for the loop thermosyphoon used for cooling the power semiconductor devices for (a) MV power devices, and (b) LV power devices. A maximum power dissipation of 2 kW is taken for both the evaporators.

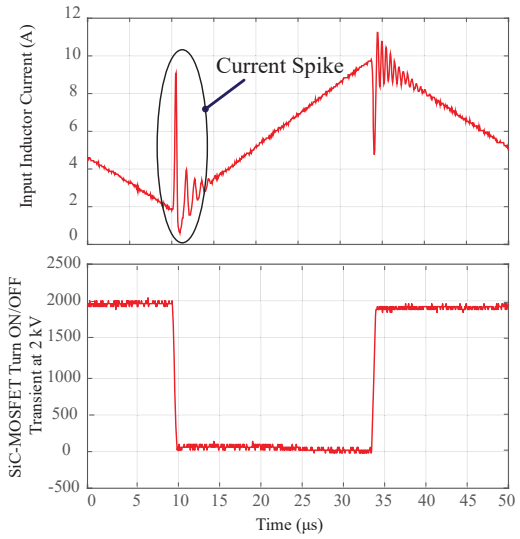


Fig. 13: Effect of inductor parasitic capacitance on the current waveform. The experiment has been done on a buck converter to validate the effect of the parasitic capacitor on the inductor [17].

the system. Various protection schemes used in the system is shown in Fig. 15.

A. Metal Oxide Varistors (MOVs)

Metal-oxide varistors or surge arrestors are placed at the connecting points of the MV and LV grids. MOVs have a very

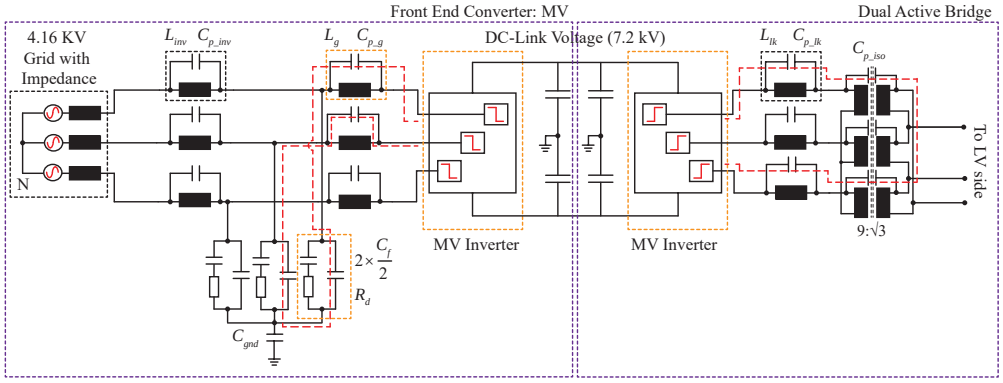


Fig. 14: Path for the common mode currents which arise due to the parasitic capacitances across various components and the high dv/dt associated with the device switching. These currents are mainly seen in the MV side converter since the dv/dt of the switches are comparatively higher than those of the LV devices.

large impedance under normal operating conditions. When it is subjected to a voltage more than a specific value, a low impedance is observed, thus diverting the surge voltages away from the converter to the ground [18], [19].

B. Fuses

The MUSE-SST is connected to the MV and LV grids via fuses to offer a one-time over-current protection. The 10 kV SiC MOSFETs are successfully tested up to a load current of 75 A. The breaking limit of the fuses is kept at a maximum current of 69 A which ensures a safe operation of MV side 10 kV SiC devices [20]. In the LV side, the devices are rated for 325 A. A fuse of 300 A is used in order to ensure the safe operation of the LV side devices.

C. Circuit Breakers (CBs)

Breaker protection systems are added to break the over-currents arises during the short circuit conditions. The typical breaking time of a breaker is 50 to 100 ms. Usually, in AC breaker systems, the breaking event occurs at the zero crossing currents irrespective of their phases [21]. The breaker system acts as a short-circuit protection scheme. Additional faster protection schemes like solid-state breakers can be used to break the current. However, it is currently not considered for the system. Additionally, breakers are used to isolate MUSE-SST from the grids during maintenance.

D. Protection and Deadtime Generation (PD) Board

The protection and deadtime generation board forms an additional level of protection from the PWM generation side. Overcurrents and overvoltages at specific nodes are fed into the sensor and consequently, sensed on the PD board for control purposes. The sensed inputs are compared with reference values for sensing an overvoltage or overcurrent.

The control signals generated by the controller gets conditioned by the PD board before sending the signal to the gate drivers. A deadtime generator is present to create the complementary signal on the board itself rather than being generated at the controller. This protects the device against any software faults. Further, all the PWM signals are passed through an enable circuitry which makes sure that all the PWMs go low, as soon as a fault is detected or an emergency stop is applied.

E. Software Protection

As an additional layer of protection, an enable circuitry, similar to that of the PD board, is created in the FPGA. The downside of this is the sampling time of the analog-to-digital (ADC) converter, which samples the input every 10 µs.

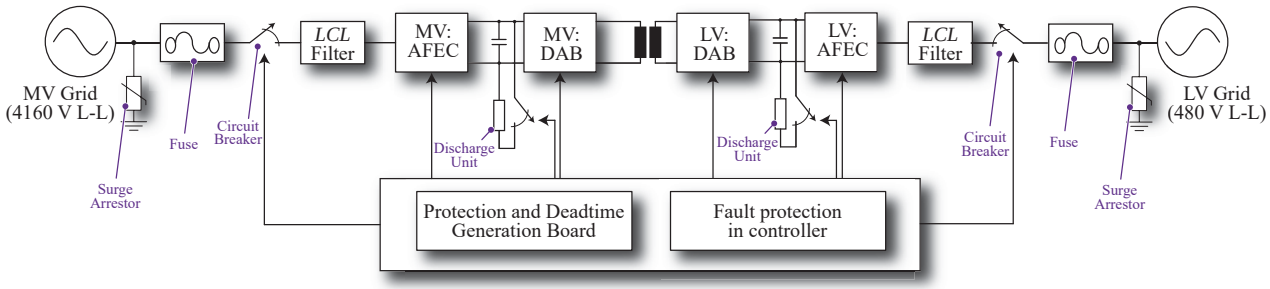


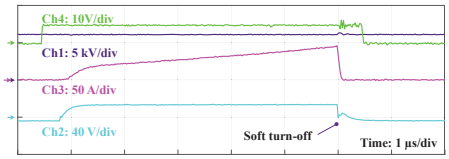
Fig. 15: Various protection schemes used for MUSE-SST. In addition to the mentioned protection schemes, additional protection for the devices, such as de-sat protection are also provided.

F. Discharging Units

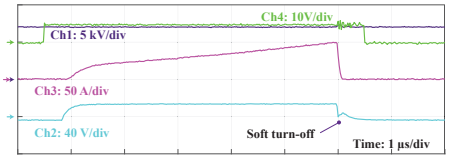
After the complete shutdown of MUSE-SST, the MV and LV DC bus capacitors retain their previous voltages, which need to be discharged for the safe operation and maintenance. In addition to that, this offers a protection scheme if the dc-link voltages swell up.

G. Short Circuit (De-Sat) Protection

A short circuit protection scheme is implemented to protect the devices in case of abnormal short circuit conditions. A conventional de-sat scheme is used in both the MV and the LV side to ensure the protection. Fig. 16(a) and Fig. 16(b) shows the experimental results for a short circuit condition on the MV dc-link for a dc-bus voltage of 6 kV and 7 kV respectively.



(a)



(b)

Fig. 16: Experimental results showing the short circuit protection capability of the designed gate driver for dc-link voltages of (a) 6 kV, and (b) 7 kV. The gate driver turns off the device within 5 µs of the fault. (Ch1: Voltage across the device; Ch2: Gate-source voltage at the device; Ch3: Current through the device; Ch4: Input pulse from the DSP/FPGA).

VI. Experimental Testing of 10 kV Devices

The basic building block for the MV side converters is the 10 kV SiC MOSFET. The packaging of the dies into a module is done maintaining the clearance and creepage requirements. Since, the 10 kV SiC MOSFETs are still in its infancy, there are a lot of challenges involved in its design and operation. The realization of MUSE-SST system in a hardware setup needs to be done after figuring out the issues associated with the continuous operation of 10 kV SIC MOSFETs. The design of the gate driver and initial double pulse tests has already been discussed. The next step involves a testing of the 10 kV SiC MOSFETs in a continuous operating mode. Initially, the device is switched at no load (half-bridge configuration with no inductors or resistors connected to the midpoint) as shown in Fig. 17(a). The top and the bottom power devices are switched alternately to make sure that the gate driver can handle the no load dv/dt and to figure out any issues with the common mode currents through the ground. The device is tested upto 6.5 kV in this case. Fig. 17(b) shows the synchronous buck operation at no load of the XHV-6 module with an input voltage of 2.8 kV and a peak current of 10 A. The common mode current is measured at the input to the gate driver of the top-side device. The common-mode current is found to be well within limits. This can be attributed to the design of the gate driver transformer. The synchronous buck operation at no load validates the soft switching operation of the converter. The XHV-6 module as well as the gate driver is tested for hard switching in a synchronous buck operation with a resistive load as shown in Fig. 17(c). The final validation of the XHV-6 module is carried out by its use in a boost converter where the voltage is boosted from 2100 V to 5.5 kV as shown in Fig 17(d). It should be noted that the tests are down up to 6 kV in continuous mode operation since the voltage protection is kept at 6.2 kV in order to avoid any catastrophic failures.

VII. Conclusions

In this paper, an overview of the MUSE-SST system is presented. A brief idea on the development of the solid-state transformers is also provided. The topology used for grid interconnection, devices used, and the method of implementation of the control is there after provided. Important practical design considerations are shown in order to help researchers identify the focus points, while designing a medium voltage system. The MUSE-SST is expected to be an attractive alternate solution for the distribution transformer in terms of providing ancillary services, such as power flow control and also be a mobile equipment for immediate replacement, in case of transformer faults. The aim of this paper is to provide an overview for building and testing MUSE-SST. A brief idea regarding the gate driver, the thermal solutions and the effect of the parasitic capacitance of the magnetic components on the entire system is discussed. The 10 kV SiC MOSFETs' operation is validated using double pulse and continuous tests at different voltage and current levels to ensure its proper operation when connected to the MUSE-SST system. This research aims at being a building block for implementation and testing of the MUSE-SST system.

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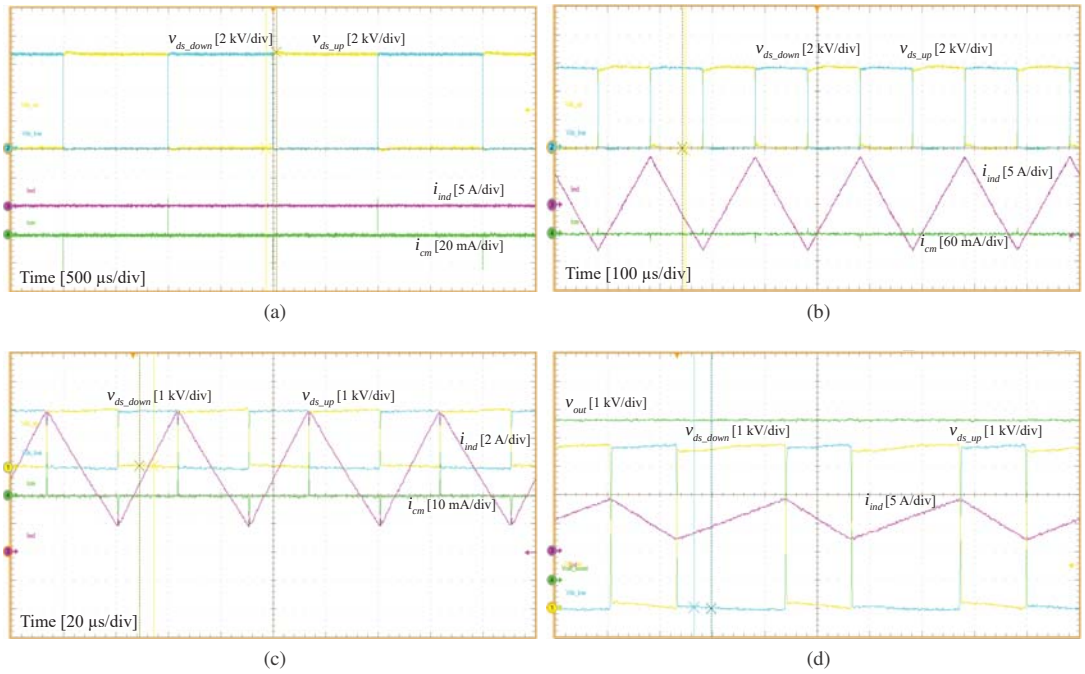

Fig. 17: Experimental results for validating the operation of the 10 kV MOSFET in the XHV-6 packaging. (a) Operation at no load and a dc-input of 6.5 kV at 500 Hz. The high voltage supply is limited in its current output capability which prevents the tests at higher voltage levels (b) Operation at a synchronous buck mode at no load. (c) Operation at synchronous buck mode with a resistive load (d) Boost mode of operation where the boost duty cycle is taken to be 0.65. The reference scales and time divisions are provided in the respective figures.

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