Multiple PR Current Regulator based Dead-time Effects Compensation for Grid-forming Single-Phase Inverter

1st Siyuan Chen FREEDM Systems Center North Carolina State University Raleigh, NC, USA schen36@ncsu.edu 2nd Zibo Chen FREEDM Systems Center North Carolina State University Raleigh, NC, USA zchen49@ncsu.edu 3rd Wensong Yu FREEDM Systems Center North Carolina State University Raleigh, NC, USA wyu2@ncsu.edu

Abstract-A multiple proportional resonant (PR) current regulator based dead-time effects compensation method for gridforming single-phase inverter is proposed. Most of dead-time effect studies are based on the polarity of the average inductor current. However, dead-time effect is eliminated at zerocrossing zone of the inductor current. Conventional dead-time compensation methods based on the polarity of the average inductor are not suitable for grid-forming single-phase inverter because of the large inductor current ripple and wide load range. In this paper, the dead-time effect considering ripple current is investigated and the relation between the load current and the range of the zero-crossing zone is discussed. Furthermore, the zero current clamping (ZCC) phenomenon and oscillation induced by dead-time are also discussed. In order to compensate the dead-time effects, a multiple PR current regulator based dadtime compensation method is proposed to reduce the voltage disturbance caused by dead-time effect in single-phase gridforming inverter. The simulation and experiment results show the validity of the analysis and the distortion of the inverter output voltage is eliminated.

Index Terms—grid-forming single-phase inverter, dead-time effects, multiple PR regulator

I. INTRODUCTION

Single-phase grid-forming inverters are widely used in AC microgirds. The purpose is to build up the ac power system voltage and frequency in the microgrids when operating in islanding mode. In pulse-width-modulation (PWM) controlled single-phase inverters, the dead-time is a necessary method to avoid short-circuit of the two-level inverter legs. As the main nonlinear characteristic of the semiconductor switching device, the dead-time produces serious waveform distortion to the output voltage. To compensate the dead-time effects, the dead-time analysis is needed to be discussed first. The deadtime produces a difference between the ideal output voltage and real output voltage and this difference is determined by the polarity of inductor current [1] during the dead-time interval. In [2], the fundamental component of the voltage difference waveform was considered when modeling the small-signal model of voltage source inverter. However, these dead-time analysis are based on the polarity of the average inductor current and the ripple current is ignored. In [3] and [4], the

effects of the ripple current and the ZCC phenomenon are investigated. However, the load change and the oscillation induced by dead-time are not discussed.

Many dead-time effects compensation methods have been proposed in the previous work [2] [3] [4] [5] [6]. Most of the dead-time compensation methods are developed based on the polarities of the average inductor current, which are not suitable for grid-forming single-phase inverter since the filter inductor in LC filter is small and the ripple current is large. The zero-crossing effect is considered in [3] and an adaptive compensation is proposed. However, because the non-linearity of the duty cycle error induced by the dead-time, it is difficult to predict the feed-forward compensation duty cycle. The dead-time compensation methods proposed in [4] [5] are feedforward compensation methods and the noise of the sensor circuits is a serious issue for these methods. [6] proposes a repetitive controller based feedback compensation method and compares compensation effects of the multiple resonant controller and repetitive controller. However, the repetitive controller is difficult to design and high frequency oscillation will be introduced.

In this paper, an equation is used to describe the relation between the load current and the range of the zero-crossing zone and the graphics solution is shown in section II. The oscillation induced by the discontinuous mode is also investigated. From the analysis, the voltage error caused by dead-time is considered as a voltage disturbance to the control system. Based on the state feedback control strategy in [7] and [8], multiple resonant controllers are used in the inner current loop to reduce the disturbance caused by the dead-time effects. Simulation and experimental results are performed to verify the analysis and effectiveness of the proposed compensation method.

II. DEAD-TIME EFFECTS ANALYSIS

In this section, the dead-time effects is analyzed. The range of the zero-crossing zone, discontinues mode effects and oscillation phenomenon are discussed.

A. Inductor Current Analysis

The topology of the typical half-bridge grid-forming inverter is shown in Fig. 1. In practice, in order to prevent the power switching devices from shoot-through during a switching period, the dead time has to be implemented in order to prevent the inverter from shoot-through during the switching interval. V_{dc} , v_o and i_L are the DC bus voltage, the output voltage and the inductor current. L and C are the filter inductor and filter capacitor respectively.



Fig. 1. The single-phase grid-forming inverter with LC filter



Fig. 2. Inductor current shape

Fig. 2 shows the inductor current shape. The fundamental cycle can be divided into three zones. The polarity of inductor current is positive within the positive zone and is negative within the negative. In zero-crossing zone, the polarity of the inductor current is changed within one switching period. The inductor current i_L consists of fundamental component $\overline{i_L}$ and ripple current i_r . $\overline{i_L}$ is calculated by using averaging model shown in Fig. 3. The ripple current i_r iddet function inductor.

$$i_L = \overline{i_L} + i_r \tag{1}$$

Using phase vector to calculate the fundamental component $\overline{i_L}$. Supposing that 1) output voltage is $\vec{v_o} = V_o \angle 0^\circ$ 2) the load is resistance load and its current is $\vec{i_o} = I_o \angle 0^\circ$. The



Fig. 3. Averaging model of single-phase inverter

phase vector and time domain expression of inductor current is expressed as (2) and (3).

$$\vec{i_L} = \vec{i_o} + j\omega C \vec{v_o} = \sqrt{I_o^2 + (\omega C V_o)^2} \angle \arctan \frac{\omega C V_o}{I_o} \quad (2)$$

$$\overline{i_L}(t) = \sqrt{I_o^2 + (\omega C V_o)^2} \sin\left(\omega t + \arctan\frac{\omega C V_o}{I_o}\right)$$
(3)

Thus, the phase vector and time domain expression of average bridge voltage is expressed as (4) and (5).

$$\vec{v_s} = j\omega L \vec{i_L} + \vec{v_o}$$

$$= \sqrt{(1 - \omega^2 L C)^2 V_o^2 + (\omega L I_o)^2} \angle \arctan \frac{\omega L I_o}{(1 - \omega^2 L C) V_o}$$
(4)
$$v_o(t) = V_o(I_o) \sin(\omega t + \alpha(I_o))$$
(5)

Where $V_s(I_o) = \sqrt{(1 - \omega^2 LC)^2 V_o^2 + (\omega L I_o)^2},$ $\alpha(I_o) = \arctan \frac{\omega L I_o}{(1 - \omega^2 LC) V_o}$

For the ripple current, the duty cycle is:

$$d(t) = 0.5 + \frac{v_s(t)}{V_{dc}} = 0.5 + \frac{V_s(I_o)\sin(\omega t + \alpha(I_o))}{V_{dc}}$$
(6)

Hence, the ripple current is:

$$i_{r}(t) = \frac{0.5V_{dc} - v_{o}(t)}{2L}T_{s}d(t)$$

= $\frac{(0.5V_{dc} - V_{o}\sin\omega t)T_{s}}{2L}\left(0.5 + \frac{V_{s}(I_{o})\sin(\omega t + \alpha(I_{o}))}{V_{dc}}\right)$ (7)

For zero-crossing zone, the boundary condition is:

$$\overline{i_L}(t)| \le i_r(t) \tag{8}$$

The equation (8) is transcendental equation and there is no explicit solution for (8). The graphical method is used to find the solution under some specific operation condition. Supposing that $L = 300\mu H$, $C = 22\mu F$, fundamental frequency f = 60Hz, switching frequency $f_s = 37.5kHz$,output voltage $V_o = 120V_{ac}$ and DC bus voltage is $V_{dc} = 760V$. Fig. 4 shows graphical waveform $|\bar{i}_L(t)| - i_r(t)$ under half load (1.25kW) condition.

Under different load condition, the ratio of the zero-crossing zone is shown in Fig. 5.



Fig. 4. Zero-crossing zone boundary



Fig. 5. Zero-crossing zone ratio

B. Voltage Disturbance Caused by Dead-time

During the dead-time, all switches of the same lag are turned off and the bridge voltage V_{an} is determined by the polarity of the inductor current. Fig. 6 shows the three modes of these diodes. Assuming the midpoint of the DC bus is the neutral point. When the inductor current flows through the freewheeling diode of switch S_1 , the bridge voltage $V_{an} = \frac{Vdc}{2}$. When the inductor current flows through the freewheeling diode of switch S_2 , the $V_{an} = -\frac{Vdc}{2}$. When the inductor current is zero, the $V_{an} = V_o$.

Fig. 7 shows the all possible (seven) situations of inductor current within one switching period if the ZCC phenomenon is considered. In S1, the magnitude of voltage error is $-V_{dc}$ and the width is T_d . In S2, the voltage error includes two parts. The magnitude of voltage error is $-V_{dc}$ in $T_d - T_m$ (where T_m is the time of ZCC) and $V_o - 0.5V_{dc}$ in T_m . In S3, the magnitude



Fig. 6. The models of half bridge inverter during dead-time (a) positive current (b) negative current (c) zero current

of voltage error is $V_o - 0.5V_{dc}$ in T_m . In S4, the voltage error is zero. In S5, he magnitude of voltage error is $V_o + 0.5V_{dc}$ in T_m . In S6, the magnitude of voltage error is V_{dc} in $T_d - T_m$ and $V_o - 0.5V_{dc}$ in T_m . In S7, the magnitude of voltage error is V_{dc} and the width is T_d .

The time of ZCC is small in one switching period. Ignore the ZCC phenomenon, the disturbance of average bridge voltage can be expressed as:

$$v_{e} = \begin{cases} -V_{dc} \frac{T_{d}}{T_{s}} & ,t \in (t_{1} \sim t_{2}) \\ 0 & ,t \in (t_{2} \sim t_{3}) \\ V_{dc} \frac{T_{d}}{T_{s}} & ,t \in (t_{3} \sim t_{4}) \end{cases}$$
(9)

Where the T_d is the dead time and T_s is the switching period. The waveform of the voltage disturbance v_e is a square wave as shown in Fig. 8 and its Fourier series is expressed as:

$$v_e(\omega t) = \frac{4}{\pi} \frac{V_{dc} T_d}{T_s} \sum_{n=1,3,5}^{\infty} \frac{1}{n} \sin \frac{n\theta}{2} \cos\left(n\omega t\right)$$
(10)



Fig. 8. Average bridge voltage error waveform

Using (8), the θ is calculated under different load conditions. Fig. 9 shows that the voltage disturbance is injected into bridge voltage of the inverter. According to the spectrum of v_e , the resonance frequencies of multiple resonant controllers are selected to compensate v_e .



Fig. 7. The switching pattern of switching device (a)S1 (b)S2 (c)S3 (d)S4 (e)S5 (f)S6 (g)S7



Fig. 9. Control plant of single-phase inverter

C. Oscillation Induced by ZCC

The single-phase inverter enters the discontinuous mode (DCM) during the ZCC as shown in Fig. 7. The small signal model is changed from CCM model to DCM model. Ignoring other disturbance, the small signal model is shown in Fig. 10



Fig. 10. Small signal model for DCM and CCM of single-phase inverter

Where $j_2 = \frac{2M(1-M)V_{in}}{D}$, $R_e = \frac{2LM^2}{D^2T_s}$, $M = \frac{V_o}{V_{in}}$ When the inverter operates from CCM to DCM, a damping

When the inverter operates from CCM to DCM, a damping resistor is added to the plant. During the ZCC interval, the average value of inductor current keeps constant. When the inverter enters CCM from DCM, the damping resistor is removed and oscillation happens because of the current distortion created during DCM interval. Fig. 11 shows the average value of inductor current under 30% load condition.

From the FFT analysis of the indutor current, the oscillation frequency is the resonant frequency of the output filter which is expressed as:

$$f_r = \frac{1}{2\pi} \sqrt{\frac{1}{LC}} \tag{11}$$

Hence, the loop gain of the current control loop at f_r needs to be as large as possible.



Fig. 11. Oscillation waveform of inductor current

III. MULTIPLE RP BASED FEEDBACK COMPENSATION METHOD

Most dead time compensation methods are based on the average current value over an entire switching period and

feed-forward compensation methods are used to modified the duty cycle to compensate the dead time effect. However, those methods cannot correctly estimated the lost voltage within zero-crossing zone because the range of zero-crossing zone is related with load. Some compensation methods are based on the detection of ripple current, which required high bandwidth current sensors and noise issue is a big problem. Besides, these feed-forward compensation methods cannot deal with the ZCC phenomenon and the oscillation problem. Hence, the feedback compensation method is preferred in this paper.

A. Feedback Compensation Method

Various feedback control strategies are available to control the output voltage of single-phase grid-forming inverter. In [7], the state feedback control topology is introduced and [8] proposed a dual-loop with state feedback control topology for inverter control. To overcome the output voltage distortion and voltage disturbance, most of papers focus on the voltage regulator design and different types of controllers are used to reduce the distortion. However, the bandwidth of the outer voltage loop is relatively low and high bandwidth voltage controller is difficult to design. Thus, disturbance with high frequency is hard to be eliminated. Compared to the outer voltage loop, inner current loop has much higher bandwidth than outer voltage loop. Also, most disturbance are injected into inner current loop including the disturbance caused by dead-time and PWM delay . Thus, it is easier to design a high bandwidth current controller in the inner current loop to reduce high frequency disturbance. In [9], the sliding mode controller (SMC) is used in the inner current loop to improve the THD of the output voltage. However, the SMC is difficult to design and implementation is complicated. Compared to SMC, PR controller is easy to implemented and the computation burden is negligible. The proposed multiple PR controllers based current regulator is shown in Fig. 12.



Fig. 12. Dual-loop control diagram for single-phase grid-forming inverter

B. Multiple PR current Controller Design

As shown in Fig. 12, the voltage disturbance is added to the current loop. For current inner loop, the transfer function of plant is:

$$G_p = \frac{1}{sL} \tag{12}$$

The transfer function for multiple PR controller is

$$G_{PR} = K_P + \sum_{i=1,3,5,\dots} K_i \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_i^2}$$
(13)

Where ω_c is the cut-off frequency and $\omega_i (i = 1, 3, 5, \cdots)$ is the resonance frequency.

From [10], the K_P determines the bandwidth of inner current loop. Hence,

$$\frac{K_P}{sL} = \frac{\omega_{pi}}{s} \tag{14}$$

$$K_P = \omega_{pi}L\tag{15}$$

Where ω_{pi} is the cut-off frequency. From [10], the maximum bandwidth for current loop is

$$\omega_c = \frac{\pi/2 - \phi_m}{T_d} = \frac{\pi/2 - \phi_m}{1.5T_s}$$
(16)

Supposing $\phi_m = 45^\circ$, switching frequency $f_s = 37.5 kHz$. Then $\omega_c = 3.125 kHz$. In this paper, $\omega_c = 3kHz$.

Since the $\omega_i(i = 1, 3, 5, \cdots)$ is much smaller than the bandwidth of the current loop. Resonant parts have little influence in high frequency zone. The gain of the resonant controllers can be set to a large value. In this paper, the K_i is set to 100 and ω_c is set to 4π . The open loop gain bode plot shown in Fig. 13.



Fig. 13. Bode plot of open loop gain

The transfer function between the voltage disturbance and inductor current is:

$$G_{vi} = \frac{G_p}{1 + G_p G_c} = \frac{G_p}{1 + T}$$
(17)



Fig. 14. Bode plot of G_{vi}

Where G_c is the transfer function of current regulator and T is the open loop transfer function. The bode plot of G_{vi} is shown in Fig. 14.

For the voltage regulator design, a PR controller is used to regulate the output voltage. Because of the high bandwidth of the inner current loop, the bandwidth for the voltage loop does not need to be very high. In this single-phase inverter, the bandwidth for voltage loop is 300Hz and the gain for the resonant regulator is 100.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The system parameters for single-phase inverter is shown in Table. I.

 TABLE I

 Parameters of single-phase grid-forming inverter

Parameters	Values
L_f	$300\mu H$
C_f	$22\mu F$
V_{dc}	760V
V_o	$120V_{ac}$
f_f	60Hz
f_s	37.5kHz

A. Simulation Results

Using PSIM simulation platform to simulate the singlephase grid-forming inverter. Output voltage V_o , inductor current I_L and bridge voltage V_s are observed. Three load conditions(750W, 1250W and 2000W) are simulated for each operation mode.

1) Open loop simulation: In open-loop simulation, a fixed modulation index SPWM gate signals are given to the half bridge to ensure that the output voltage $V_o = 120V_{ac}$



Fig. 15. Simulation results of average bridge voltage V_s and voltage disturbance V_e under open-loop operation

Fig. 15 shows the average bridge voltage V_s and voltage disturbance under different load conditions. The relation between the range of zero-crossing zone and load is verified by the waveform of V_e .



Fig. 16. Simulation results of inductor current I_L under open-loop operation

From the average inductor current waveform in Fig. 16, it can be seen that there is an oscillation when the inverter enters CCM from DCM.



Fig. 17. Simulation results of output voltage Vo under open-loop operation

2) Closed loop simulation with proportional current regulator: Proportional inner current regulator is widely used in dual-loop control scheme. Fig. 18 shows the duty cycle generated by the current regulator and the compensation duty cycle V_{com} . The shape of V_{com} is similar to the voltage error V_e in open loop simulation.



Fig. 18. Simulation results of duty cycle and compensation duty cycle V_{com} with P current regulator



Fig. 19. Simulation results of output voltage V_o with P current regulator

3) Closed loop simulation with multiple PR current regulator: Multiple resonant controllers are used in the inner current loop. Fig. 20 shows the compensation duty cycle generated by the current regulator and the compensation duty cycle V_{com} . Compared with the V_{com} in Fig. 18, the shape of V_{com} in Fig. 20 is more similar to the voltage error V_e in open loop simulation.



Fig. 20. Simulation results of duty cycle and compensation duty cycle V_{com} with multiple PR current regulator



Fig. 21. Simulation results of output voltage V_{o} with multiple PR current regulator

From Fig. 17, Fig. 19 and Fig. 21, the THD of the output voltages are shown in Table. II

TABLE II SIMULATION RESULTS OF THE THD OF OUTPUT VOLTAGE V_{o}

THD	Openloop	P Controller	PR Controller
750W	5.6%	2.6%	1.9%
1250W	6.1%	2.6%	1.9%
2000W	6.1%	2.6%	1.7%

B. Experimental Results

To validate the proposed dead-time compensation method, a 2.5kW SiC MOSFETs based high switching frequency singlephase grid forming inverter has been built and experimented. The hardware testbed is shown in Fig. 22.



Fig. 22. 2.5kW SiC MOSFETs based single-phase grid-forming inverter

1) Experiment results for open loop operation: Fig. 23 shows average bridge voltage and voltage disturbance under different load conditions. The experiment results verify the zero-crossing zone analysis.



Fig. 23. Experiment results of bridge voltage V_s under open loop operation

From the average inductor current waveform in Fig. 24, it can be seen that there is an oscillation just after ZCC zone.



Fig. 24. Experiment results of inductor current I_L under open loop operation



Fig. 25. Experiment results of output voltage Vo under open loop operation

2) Experiment results for closed loop control with P current regulator: With P inner current regulator, the output voltage is shown in Fig. 26.



Fig. 26. Experiment results of output voltage V_o with P current regulator

3) Experiment results for closed loop control with multiple PR current regulator: With multiple PR inner current regulator, the output voltage is shown in Fig. 27.



Fig. 27. Experiment results of output voltage V_o with multiple PR current regulator

From Fig. 25, Fig. 26 and Fig. 27, the THD of the output voltages are shown in Table. III

TABLE III EXPERIMENTAL RESULTS OF THE THD OF OUTPUT VOLTAGE V_{o}

THD	Openloop	P Controller	PR Controller
750W	5.07%	3.58%	1.76%
1250W	6.18%	3.73%	1.77%
2000W	7.48%	3.57%	1.60%

V. CONCLUSION

As for grid-forming single-phase inverter, the dead-time effects considering filter inductor current ripple and wide load range is discussed in this paper. The quantitative analysis is made on the relation between the zero-crossing zone and the load current. Furthermore, the oscillation induced by the dead-time is discussed. The dead-time analysis is verified by the simulation and experimental results. Based on dead-time analysis, a voltage disturbance model induced by dead-time is built and a multiple PR current regulator based feedback compensation methods is proposed to reduce the dead-time effects. In contrast to the conventional feed-forward compensation methods, the multiple PR current regulator based compensation method can compensate the dead-time effects under wide-load condition and it is easy to implement. Its performance is verified by the THD reduction of the output voltage in the simulation and experiments results.

References

- N. Urasaki, T. Senjyu, K. Uezato, and T. Funabashi, "An adaptive deadtime compensation strategy for voltage source inverter fed motor drives," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1150–1160, Sept 2005.
- [2] S. Ahmed, Z. Shen, P. Mattavelli, D. Boroyevich, and K. J. Karimi, "Small-signal model of voltage source inverter (vsi) and voltage source converter (vsc) considering the deadtime effect and space vector modulation types," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4145–4156, June 2017.
- [3] M. A. Herran, J. R. Fischer, S. A. Gonzalez, M. G. Judewicz, and D. O. Carrica, "Adaptive dead-time compensation for grid-connected pwm inverters of single-stage pv systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2816–2825, June 2013.
- [4] H. Wang, X. Pei, Y. Chen, Y. Kang, and X. Yue, "An adaptive deadtime compensation method for sinusoidal pwm-controlled voltage source inverter with output lc filter," in 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), March 2011, pp. 778–785.
- [5] S. H. Hwang and J. M. Kim, "Dead time compensation method for voltage-fed pwm inverter," *IEEE Transactions on Energy Conversion*, vol. 25, no. 1, pp. 1–10, March 2010.
- [6] Y. Yang, K. Zhou, H. Wang, and F. Blaabjerg, "Harmonics mitigation of dead time effects in pwm converters using a repetitive controller," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2015, pp. 1479–1486.
- [7] M. J. Ryan, W. E. Brumsickle, and R. D. Lorenz, "Control topology options for single-phase ups inverters," in *Proceedings of International Conference on Power Electronics, Drives and Energy Systems for Industrial Growth*, vol. 1, Jan 1996, pp. 553–558 vol.1.
- [8] P. C. Loh, M. J. Newman, D. N. Zmood, and D. G. Holmes, "A comparative analysis of multiloop voltage regulation strategies for single and three-phase ups systems," *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1176–1185, Sept 2003.
- [9] Z. Li, C. Zang, P. Zeng, H. Yu, S. Li, and J. Bian, "Control of a gridforming inverter based on sliding-mode and mixed H₂/H_∞ control," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3862– 3872, May 2017.
- [10] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase ac current regulators," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2417–2426, Nov 2009.