Reliability Oriented Design of Dual Active Bridge Converter for Power Supply on Heavy-Vehicles

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***Abstract*—The design of power electronic converters is often driven by goals such as full-load efficiency, power density or cost per watt of power transferred. In the paper, application of power electronic conversion system in heavy-duty vehicle industry is considered; in this low-volume industry, system reliability and availability along with economies of scale are also crucial. In this respect, a dual active bridge (DAB) based *dc-dc* power electronic building block (PEBB) is considered to supply an auxiliary load. Economies of scale are achieved by designing the PEBB for its reliable operation across different vehicle platforms of the original equipment manufacturers (OEM), while catering to their disparate specifications. A method is proposed in the paper to realise a design of a DAB based PEBB for maximum system availability by minimising the lifetime consumption of the semiconductor device for a defined load-cycle. It is illustrated for a load-cycle of air-conditioning compressors in heavy vehicles.**

***Keywords*—Bidirectional dc-dc converter, dual active bridge, DAB, optimal design, semiconductor loss modeling, reliability.**

I. Introduction

In the modern day and age when there is emerging and growing conciousness in the world about the environmental impact of its energy consumption, the transportation sector is seeing a renewed push toward electrification. The primary focus of transportation electrification is its propulsion system, which requires complete overhaul of the vehicle drive-train. The heavy-duty vehicle industry is typically reluctant to change due to established reliability credentials of the existing technologies. Therefore, movement toward electric propulsion is gradual when compared to passenger car industry. However, all vehicles, especially the heavy-duty vehicles, also have other uses of electricity. Auxiliary loads such as power steering, oil pumps, water pumps, cooling fans, air-brake compressor, starter motor and alternator in a heavy-duty truck were traditionally mechanically powered. Similarly, in commercial aircrafts, several loads such as environment control system (ECS), flight control actuators including rudders and over-wing control surfaces are also mechanically powered [1]. All these loads are now being shifted to electrical systems to achieve, most of all, weight reduction and improved reliability; electrification or hybridization of such loads has demonstrated excellent potential for fuel savings [1], [2].

A major road-block in adoption of electrification is the ability of a power electronic converter to operate in harsh environment, where it is subjected to thermal and mechanical stresses beyond those in other applications. Therefore, although there has been a concerted push towards

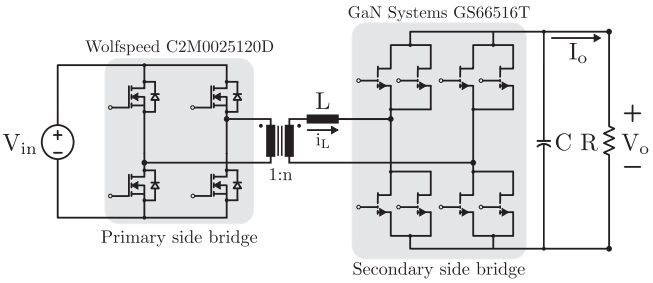

Fig. 1: Circuit topology of dual active bridge.

vehicle electrification, it has accelerated in recent times due to commercialization of enabling technologies, such as Silicon Carbide (SiC) and Gallium Nitride (GaN) based semiconductor devices. The advent of these wide band-gap (WBG) semiconductor devices allow the power converters to operate at temperatures exceeding 100°C [3], [4].

In this paper, an auxiliary power supply system is designed. The intended application of the converter is to supply power to auxiliary services in heavy-duty vehicles. These are, typically, capital-intensive equipment and are required to have maximum availability for cost recuperation. Hence, long term reliability and system availability, particularly at elevated operating temperature, are core priorities for heavy-duty vehicle power electronic applications. In any converter, semiconductor devices and capacitors contribute to most failures resulting in down-time. At these temperatures, the efficiency is also impacted due to increased losses. Further, the variability of load conditions result in semiconductor devices being subjected to large thermal cycles with a high mean temperature. It is reported that the magnitude of these cycles and their mean are the most important parameters affecting the reliability of semiconductor devices [5]–[7].

Another key issue in the heavy-duty vehicle industry is the low production volume. A successful new product introduction, therefore, requires sufficient economies of scale. These are achieved by developing a basic power electronic building block (PEBB) to be utilized on all vehicle platforms of an original equipment manufacturer (OEM); the desired power rating may be achieved by integrating multiple PEBBs. Moreover, such modular structure allows distribution of losses and improved system availability. However, to retain compatibility with existing voltage systems, wide range of input and/or output voltage operation may be specified. Hence, any optimal design must account for the specified operating range. In the present application, a bidirectional isolated *dc-dc*

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TABLE I: System parameters

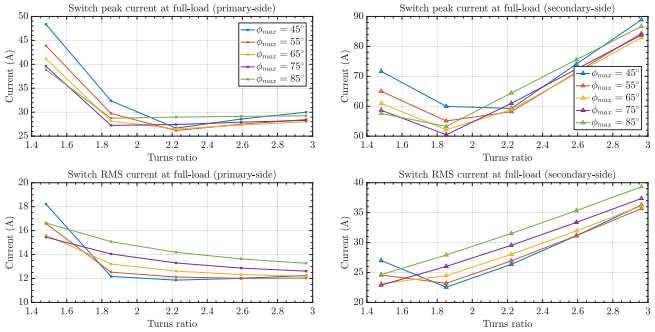
Parameter	Variable	Value
Rated power	$P_{o,\max}$	6kW
Input voltage	V_{in}	400V - 800V
Output voltage	V_o	270 V
Ambient temperature	T_A	105°C

power conversion system is to be designed according to specifications in Table I. The converter is to be operated at elevated temperature to utilize same thermodynamic cooling loop as that of the engine. It eliminates the typically used second cooling loop, operating at 70°C [8] and specifically designed for electronics, leading to savings in space, weight and fuel.

The dual active bridge (DAB) converter, shown in Fig. 1 and introduced in [9], is a popular topology for providing high, bi-directional, isolated, *dc-dc* power conversion in automotive applications [10]. The converter operation is characterized by two full-bridge converter circuits generating high frequency *ac* voltage across a transformer-inductor arrangement. DAB converter is preferred due to its high conversion ratio, bi-directional power transfer capability with galvanic isolation, low passive component count and a simple control scheme. It also has soft turn-on capability eliminating a major component of switching losses when MOSFETs or GaN HEMTs are used.

Several papers have reported optimal design and operation of DAB converter [11]. In these, designs with minimum RMS or peak current or maximum power density have been realised. In the paper, a guideline is proposed to design for maximum availability based on lifetime consumption of semiconductor devices for a given load profile. Foremost, the losses of semiconductor devices are mapped for varying currents, voltages and temperatures based on the characterization tests or data-sheet values. Also, the thermal response of the package to a unit power loss is mapped. Subsequently, a temperature profile for the device is estimated when the converter is subjected to a given load-profile. Thereafter, rainflow counting method [12] is utilized to count the number of effective thermal cycles, as well as their magnitude and mean. The data can, then, be used in the models separately developed for devices to estimate the total lifetime consumption across the defined design space. The process is repeated for expected load profiles and their input voltages for each vehicle platform. Subsequently, based on business needs and objectives, the average converter availability across different vehicle platforms is estimated and optimized.

The paper is organized as follows: section II establishes the design space for design of a DAB converter. Section III introduces the method to model the loss-data – turn-on, turn-off and conduction losses – for semiconductor devices. Similarly, the thermal response of the devices is also modeled as n-layer Foster network in section IV. Subsequent sections propose a method to apply these models to a given load profile of a DAB converter. Here, an air-conditioner compressor load profile [13] is used to generate the temperature profiles of semiconductor devices. Finally lifetime consumption of the device per load cycle and its mean time to failure (MTTF) can be computed based on available device failure models. The design may then be optimized to achieve the best business value for the developed PEBB.



(a) (b)

Fig. 2: Switch currents, peak and RMS, at different maximum phase-shift angles ($\phi_{\max}$) and turns-ratio (n) for (a) primary-side bridge and (b) secondary-side bridge.

II. Preliminary Design and Design Space

A design of a DAB converter can be characterized by four parameters: the transformer turns-ratio (n), switching frequency (f_s), maximum phase-shift angle ($\phi_{\max}$) and the power transfer inductance (L). All four parameters are interdependent and, therefore, if three of these are specified, the fourth parameter can be calculated from the power transfer expression in (1).

$$P_{\max} = \frac{nV_{in,\min}V_o}{2\pi f_s L}\phi_{\max}\left(1 - \frac{\phi_{\max}}{\pi}\right) \tag{1}$$

In the present case, the DAB converter is designed utilizing parameters $\{n, f_s, \phi_{\max}\}$, while L is calculated from (1). It is essential to note that for a specific turns-ratio and maximum phase-shift angle, the switching frequency and inductance are inversely proportional to each other. The device currents, therefore, are independent of switching frequency and inductor value. The switching losses, however, are a function of f_s and L. Therefore, in a preliminary design where the semiconductor devices are to be selected, a nominal switching frequency of 50kHz is considered.

The two variables, n and $\phi_{\max}$, remain to be specified. The outer limits on the design space for the transformer turns ratio are defined by the input voltage specification. The design space for transformer turns ratio, n, is between 400/270 and 800/270. The design space for maximum phase-shift requires attention; for a given rated power, when the input voltage is minimum, the phase-shift angle will be maximum. When the input voltage is maximum, the phase-shift angle will be minimum. Since the converters are digitally controlled, it will determine the quantum of power – at maximum input voltage – affected by the change in the least significant bit of the control variable, as implemented in a micro-controller or a DSP. The range for $\phi_{\max}$ is, arbitrarily, set between 45°-85°.

The variation of switch peak and RMS currents across the design space is illustrated in Fig. 2. Additionally, the maximum input and output voltages are 800V and 350V, respectively, when over-voltage conditions are also considered. Therefore, 1200V, 60A SiC MOSFET (Wolfspeed C2M0025120D) and 650V, 47A GaN HEMT (GaN Systems GS66516T) are selected for primary and secondary side devices respectively. These selected semiconductor devices have non-isolated

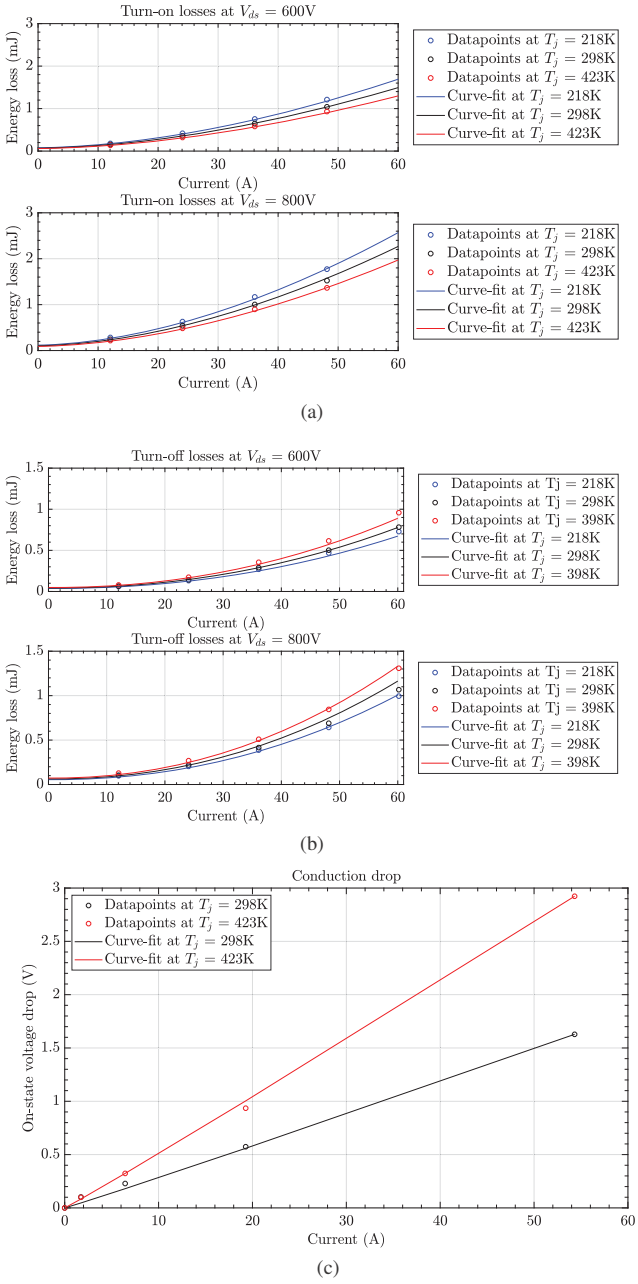


Fig. 3: Comparison of (a) turn-on and (b) turn-off loss curves, and (c) on-state voltage drop curves for Wolfspeed C2M0025120D with their fitted plots.

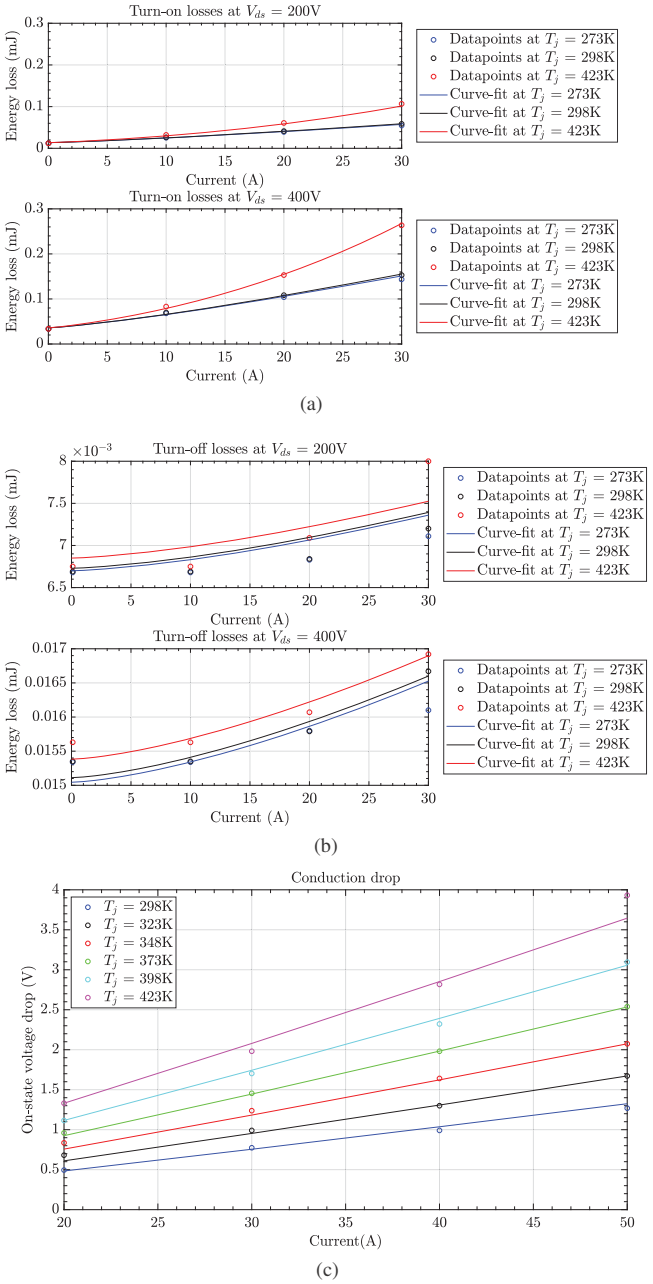


Fig. 4: Comparison of (a) turn-on and (b) turn-off loss curves, and (c) on-state voltage drop curves for GaN Systems GS66516T with their fitted plots.

thermal pads, and therefore, require an electrically-insulating, thermally-conducting material for interfacing it to a heat-sink. The drastic reduction in thermal resistance to ambient requires de-rating of semiconductor devices. In fact, in case of GaN devices, two parallel devices are required for the secondary side full-bridge circuit, as shown in Fig. 1.

III. Loss Models

The *second step* in the procedure is to model the semiconductor losses, switching and conduction, which will be used to compute power loss across a given load profile. The semiconductor loss data may be derived through extensive characterization tests or extracted from data-sheet values. If accurate switch model is available, SPICE simulations may also be used for loss characterization. Presently, the loss data for Wolfspeed devices are extracted from their data-sheet [14] and those for GaN Systems devices from simulations using its SPICE model [15].

$$\{E_{\text{on}}, E_{\text{off}}\} = (a \cdot I_{\text{ds}}^{b} + c)\left(\frac{V_{\text{ds}}}{V_{\text{ds,nom}}}\right)^{d}\left(\frac{T_j}{T_{j,\text{nom}}}\right)^{e}$$
$$V_{\text{ds,on}} = a \cdot I_{\text{ds}}^{b} \cdot \left(\frac{T_j}{T_{j,\text{nom}}}\right)^{c} \tag{2}$$

TABLE II: Coefficients of the loss models of Wolfspeed C2M0025120D

Coefficients	a	b	c	d	e
Turn-on loss	0.0011	1.7527	0.0687	1.4516	-0.3988
Turn-off loss	1.1e-4	2.1547	0.0424	1.3993	0.4642
On-state voltage drop	0.0264	1.0321	1.6708	–	–

TABLE III: Coefficients of the loss models of GaN Systems GS66516T

Coefficients	a	b	c	d	e
Turn-on loss	0.0017	1.2565	0.0359	1.3988	0.0004*
Turn-off loss	1.03e-5	1.4629	0.0151	1.1671	0.0507
On-state voltage drop	0.0179	1.0996	2.8898	–	–

TABLE IV: Thermal response network parameters

Wolfspeed C2M0025120D		GaN Systems GS66516T	
Thermal Resistance (°C/W)	**Time Constant (s)**	**Thermal Resistance (°C/W)**	**Time Constant (s)**
0.0066	18.9×10^{-6}	0.0055	1×10^{-6}
0.0197	0.28×10^{-3}	0.0249	25.3×10^{-3}
0.0738	2.53×10^{-3}	0.1281	0.44×10^{-3}
0.1392	27.8×10^{-3}	0.1377	2.41×10^{-3}

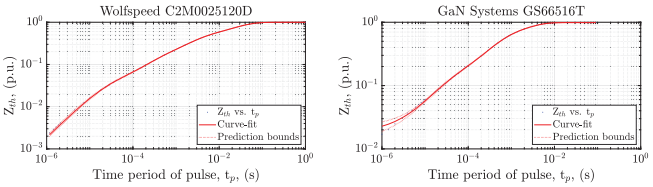
The extracted switching energy loss and on-state voltage drop data are curve-fitted to the assumed non-linear models of the form given in (2). The exponents, b, d and e, may be constants, linear or non-linear functions of drain current (I_{ds}), drain-to-source voltage (V_{ds}) or junction temperature (T_j). Foremost, the switching energy loss data are modeled at nominal voltage and temperature of the device, as a non-linear function of drain current. Coefficients a and b are thus derived. Subsequently, a scaling factor, d, is derived to model the switching energy loss at off-nominal voltage values. Thereafter, another scaling factor, e, is derived to model the variations with temperature. Similarly, the on-state voltage drop is modeled at nominal temperature, as a non-linear function of drain current and then scaled to accommodate off-nominal temperatures. At each step, goodness of fit, RMS error and normal distribution of residuals are verified to ensure correct fit. The parameters of the curve-fit models of semiconductor losses are summarized in Table II and Table III.

A. Wolfspeed C2M0025120D: 1200V, 60A SiC MOSFET

The turn-on, turn-off losses and conduction voltage drop for Wolfspeed C2M0025120D are extracted from the data-sheet curves supplied by the manufacturer [14], and compared with the extracted models in Fig. 3a, Fig. 3b and Fig. 3c, respectively. The parameters $\{a,b,c,d,e\}$ are constant. All models fit the data with less than 1% RMS error.

B. GaN Systems GS66516T: 650V, 47A GaN-FET

The turn-on, turn-off losses and conduction voltage drop for this device are extracted from simulation using the SPICE model supplied by the manufacturer [15], and compared with the extracted models in Fig. 4a, Fig. 4b and Fig. 4c, respectively. The parameters $\{a,b,c,d\}$ are constants, whereas e is a function of drain-current and temperature (3). The turn-on loss and conduction drop fit the data with less than 1% RMS error. The RMS error of the curve-fit models of turn-off losses is larger, although its maximum absolute value is less than 0.5µJ. Therefore, the model is considered acceptable.



(a) (b)

Fig. 5: Comparison of thermal response plots for (a) Wolfspeed C2M0025120D and (b) GaN Systems GS66516T with their fitted curves.

$$e(I_{\text{ds}}, T_j) = k \cdot I_{\text{ds}} \cdot (T_j - T_{j,\text{nom}}) \tag{3}$$

IV. Thermal Models

In this section the model for thermal response network of the semiconductor device is developed. It determines the propagation of heat from the device junction to its case. The packaging of the device plays an important role as each layer adds its own thermal resistance and capacity. It can be accurately determined by conducting extensive open-package thermal characterization of devices, which is beyond the scope of the paper. Here, the thermal response is modeled by way of fitting the data-sheet curves to a fourth-order Foster network [16] and expressed in (4). $R_{\text{th},i}$ is the thermal resistance of layer 'i' and τ_i is its thermal time-constant. In steady-state, the exponential terms will decay to zero and (4) will reduce to thermal resistance, R_{th}, specified in the datasheet.

$$Z_{\text{th}} = \sum_{i=1}^{4} R_{\text{th},i}\Big(1 + \exp\big(-\frac{t}{\tau_i}\big)\Big) \; ; \; \tau_i = R_{\text{th},i} \cdot C_{\text{th},i} \tag{4}$$

A. Thermal interface material and heat-sink

For the purpose of the study, Bergquist Company's SilPad 2000 thermally conductive tacky tape has been considered as the thermal interface material (TIM) for C2M0025120D and Henkel's gap filler GS3500S35 as that for GS66516T. The TIM has a thermal resistance of 0.68°C/W for the base-area of C2M0025120D (0.3sq.in.) and 1.49°C/W for the base area of GS66516T (0.072 sq.in.). The thermal resistance from the liquid cooled heat-sink surface to the fluid is assumed to be 0.5°C/W for C2M0025120D and 1.0°C/W for GS66516T, while the fluid temperature is assumed constant at 105°C.

B. Thermal response network model

The eight parameters of the four-layer Foster thermal response network in form of thermal resistances and time constants are derived using the non-linear least squares curve-fit method. These parameters are listed in Table IV. The developed models are compared with the data extracted from the corresponding data-sheets [14], [17] in Fig. 5. The RMS error in fitting the curve to the data of both the semiconductor devices is less than 1%. Note that the thermal response is form of impedance normalized to the corresponding steady-state thermal resistance values.

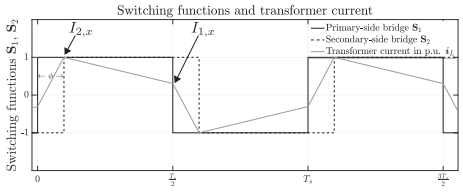


Fig. 6: Per-unitized *ac* waveforms of PSM-DAB converter.

V. Expressions for DAB converter

A typical operation of DAB converter in phase-shift modulation (PSM) is shown in Fig. 6. The primary-side bridge *ac* voltage leads that of generated by secondary-side bridge by an angle ϕ. As shown in Fig. 6, the inductor current is trapezoidal in nature with its corner points defined by switching instants. The primary-side devices switch when the inductor current is $\pm I_1$ referred to primary side, whereas secondary-side devices switch when the current is $\pm I_2$ referred to secondary side. The subscript 'x' in Fig. 6 is used to indicate either primary or secondary side of the transformer. The expressions of currents at switching instants and the RMS value of inductor current on the primary-side is given in (5).

$$\begin{aligned} I_{1,\text{pri}} &= \frac{1}{2}\frac{V_{\text{in}}\cdot\pi - n\cdot V_o\cdot(\pi-2\phi)}{\omega L} \\ I_{2,\text{pri}} &= \frac{1}{2}\frac{n\cdot V_o\cdot\pi - V_{\text{in}}\cdot(\pi-2\phi)}{\omega L} \\ I_{\text{RMS,pri}} &= \sqrt{\frac{I_{1,\text{pri}}^2 + I_{2,\text{pri}}^2 + I_{1,\text{pri}}I_{2,\text{pri}}(1-2\phi/\pi)}{3}} \end{aligned} \tag{5}$$

The secondary-side current at the switching instants and the transformer RMS current are scaled by the turns-ratio, n. The RMS currents in semiconductor devices are scaled as $1/\sqrt{2}$ of the corresponding transformer RMS current (6).

$$\begin{aligned} I_{1,\text{sec}} = \frac{I_{1,\text{pri}}}{n}\ ;\ I_{2,\text{sec}} = \frac{I_{2,\text{pri}}}{n}\ ;\ I_{\text{RMS,sec}} = \frac{I_{\text{RMS,pri}}}{n} \\ I_{\text{sw,RMS},x} = \frac{I_{\text{RMS},x}}{\sqrt{2}}\ \forall x \in \{\text{pri,sec}\} \end{aligned} \tag{6}$$

The currents at the switching instants determine the switching energy loss at turn-on and turn-off of the semiconductor devices. If I_1 is positive, then the primary side devices turn-on at zero voltage; and, if I_2 is positive then the secondary side devices turn-on at zero voltage. At these operating points, the respective turn-on losses are negligible. Similarly, if I_1 or I_2 is negative, then the primary side or secondary side devices, respectively, turn-off into zero voltage. At these operating points, the turn-off losses are negligible.

As mentioned in earlier sections, a DAB converter supplying rated power, $P_{o,\text{max}}$, is defined by any three of the four parameters: n, L, ϕ_{max} and ω. In the paper, as the design space is defined in $\{n, \phi_{\text{max}}, \omega\}$, the *ac* inductor L is calculated using (7).

$$L(n,\omega,\phi_{\text{max}}) = \frac{1}{P_{o,\text{max}}}\frac{n\cdot V_{\text{in,min}}\cdot V_o}{\omega}\phi_{\text{max}}\Big(1-\frac{\phi_{\text{max}}}{\pi}\Big) \tag{7}$$

At a particular design point, $\{n, \phi_{\text{max}}, \omega, L\}$, and given load profile: for each point in the load profile, the phase-shift angle ϕ needed to transfer the required power is calculated using (8).

$$P_o = \frac{n\cdot V_{\text{in}}\cdot V_o}{\omega L}\phi\Big(1-\frac{\phi}{\pi}\Big) \tag{8}$$

The semiconductor currents at switching instants and their RMS value, for the given load profile, are calculated using (5) and (6).

VI. Reliability oriented design process

A. Load, loss and temperature profiles

In the section, a sample load profile to which the power converter will be subjected is considered. The load profile is that of a converter supplying an air-conditioner compressor load. The compressor is assumed to operate with a periodic 10-minute cycle [13], as shown in Fig. 7b. The operating range of the compressor is discretized from 0% to 100% load in steps of percentage-point load. Given the load profile, the switching and conduction loss models along with the thermal response network models are used to compute loss and temperature profiles of the semiconductor devices. The method outlined here is not restricted by a specific load profile; any other profile, such as those generated through experiments, user-data or testing procedures, may also be used with this method.

The flow-chart of the design process is shown in Fig. 7a. The Euclidean norm approach to this optimization problem is infeasible, because the damage or lifetime consumption of semiconductor device does not have a closed-form expression. Instead, the design space is split into finite number of areas defined by corner points. The process of evaluating the parameters, generating device current profiles using (5)-(8) and iterative realization of loss/temperature profiles is repeated at every design point.

The design space for turns-ratio and maximum phase-shift angle enumerated in section II is split and defined by 81 equally-spaced design points, as expressed in (9).

$$\begin{aligned} \phi_{\text{max}} = 45 + 5\cdot k;\ n = \frac{400+50\cdot k}{270} \\ \text{where; } k = \{x | x\in\mathbb{Z}, x\geq 0, x\leq 8\} \end{aligned} \tag{9}$$

At every point on the load profile, the semiconductor loss and junction temperature is required to be computed. However, the semiconductor loss is a function of not only the drain currents and drain-to-source voltages, but also that of junction temperature. Hence, it is essential to understand how the junction temperature is to be calculated using thermal response network model and superposition theorem. Incorrect application of superposition theorem may result in incorrect inferences. The thermal response network impedance, Z_{th}, represents its response to a one Watt step-input power loss. Any derived power loss profile may be be seen as several power pulses stacked alongside one another on the time axis. Each pulse may be represented as a sum of two step functions of equal magnitude, one positive and one negative, separated in time by the pulse duration. The combined response of the thermal impedance network to constituent step functions realizes the thermal response to that pulse of power.

A semiconductor device conducts power and, therefore, generates losses for half the switching period. In the other half-cycle when it is not conducting, the die or junction temperature starts to fall. This switching frequency ripple in junction temperature is assumed negligible. It is rooted in the fact that only one time constant of the thermal impedance network, listed in Table IV, is in the same order as the

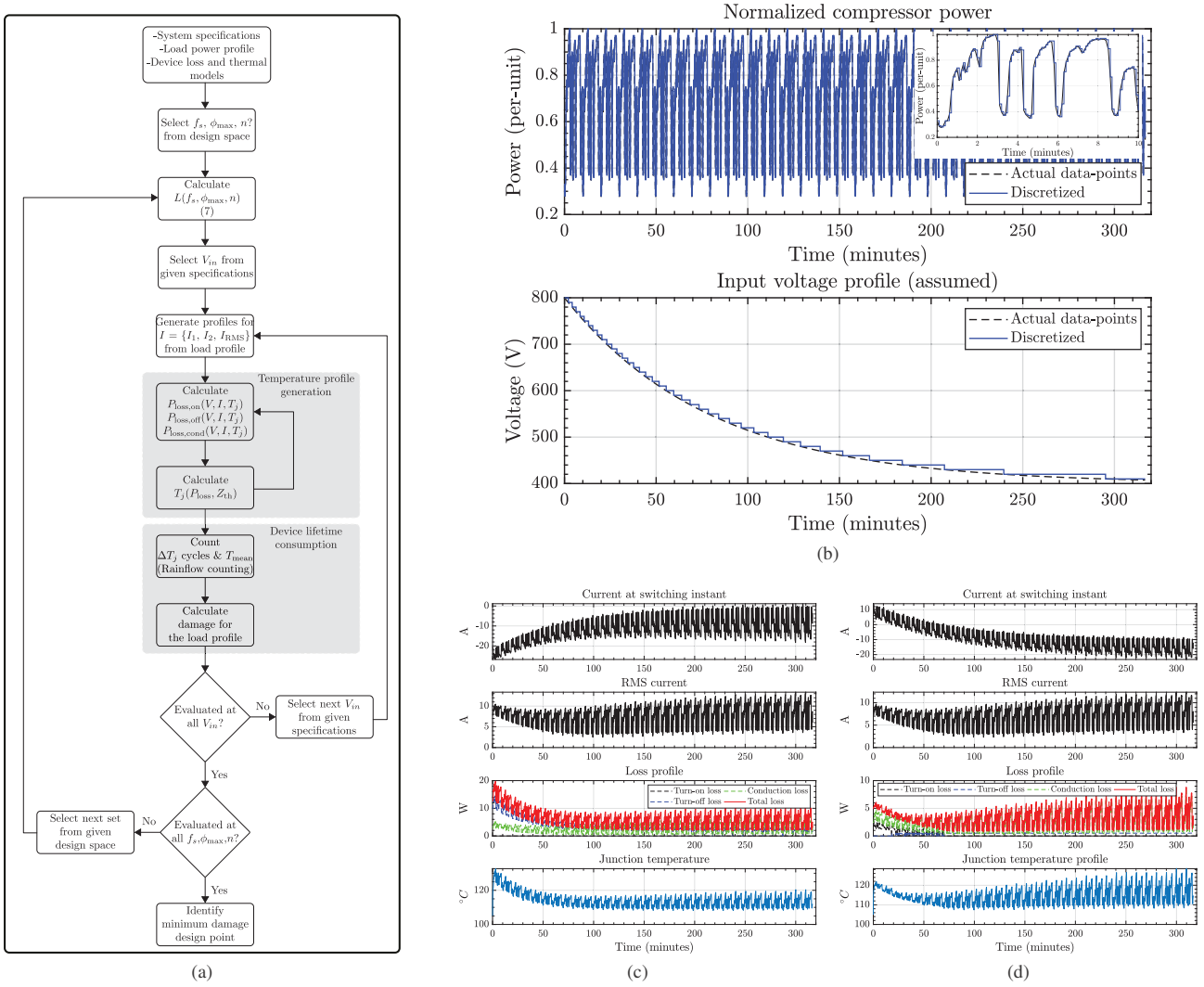


Fig. 7: (a) Process flow-chart, (b) 10-minute load profile of the air-conditioner compressor [13] extended to 320 minutes and the assumed V_{in} profile. Current, loss and temperature profiles for (c) primary-side and (d) secondary-side semiconductors when $\{n,\phi_{\text{max}},f_s\}$ = {500/270, 75°, 50kHz}.

switching period; and, that it has a very low associated thermal resistance. It indicates that, the loss power, pulsing at switching frequency, and flowing through this resistance will result in negligible temperature change. For instance, a 20W power loss generated by C2M0025120D will result in a steady-state increase of 0.1°C across $R_{th,1}$.

Apart from the load profile, an input voltage profile must also be known. The input side *dc* bus may be fed from an inverter, holding the *dc* voltage constant, or it may be supplied from a battery system where it is allowed to discharge. Disparate input voltage profiles for application in different vehicle platforms of the OEM may also be considered. In the paper, the input voltage profile, shown in Fig. 7b, is considered to be an exponentially decaying function of time. At each design point, the switching loss, conduction loss and junction temperature profiles are iteratively computed. The process described above is illustrated for C2M0025120D in Fig. 7c and for GS66516T in Fig. 7d when $\{n,\phi_{\text{max}},f_s\}$ = {500/270, 75°, 50kHz}; switch currents and temperature profiles are shown.

B. *Visualization of energy loss and temperature cycling*

The thermal profiles generated for all the design points in the specified design space are utilized to compute failure rate using the lifetime models of the semiconductor devices. In semiconductor devices, time dependent dielectric breakdown (TDDB) of gate-oxide, high temperature reverse bias (HTRB), bond-wire lift-off and die solder cracking are the most common failure mechanisms.

The failure rates are dependent on lifetime models of semiconductor devices, which are non-linear functions of amplitude of regular, periodic temperature cycle and its mean. However, converting irregular thermal profiles generated in the previous section to regular cycles requires a counting algorithm. It identifies the peaks and valleys in the thermal profile to compute total number of full or half cycles of temperature characterized by their amplitude (ΔT_j), mean ($T_{j,\text{mean}}$) and period (t_{prd}). While several counting methods are reported [12], rain-flow counting algorithm is one of the most popular methods which is also applied in the paper. The

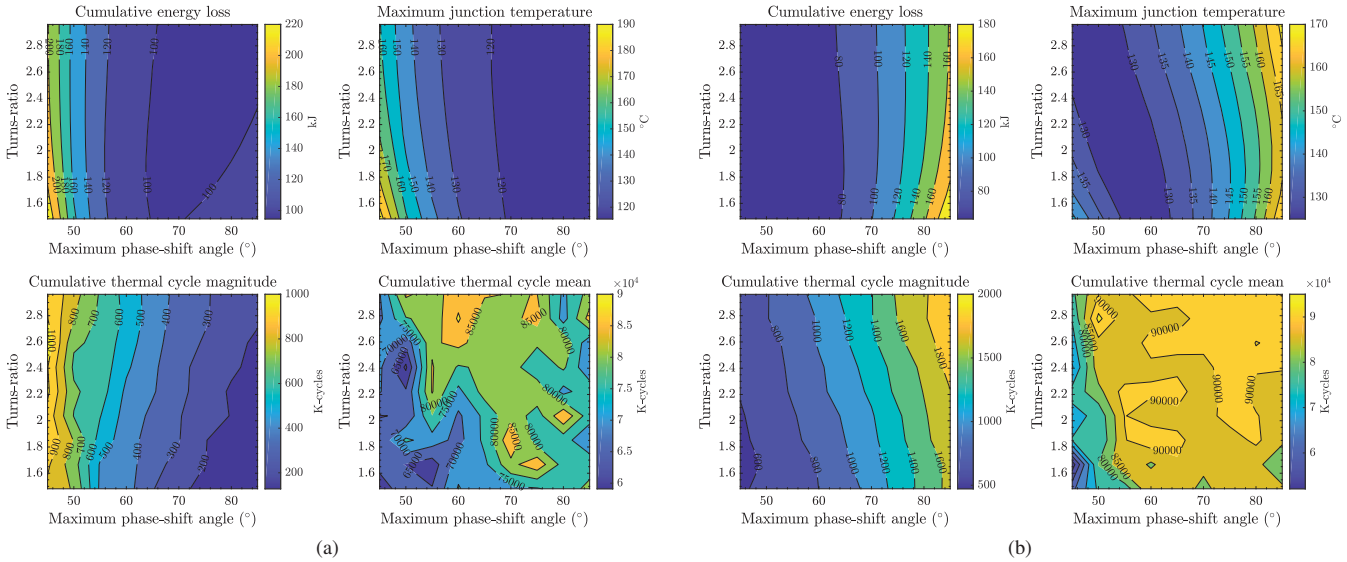


Fig. 8: Cumulative energy loss in Joules and maximum junction temperature over the given load profile, along with cumulative sum of amplitudes and that of mean of all thermal cycles (Kelvin-cycles) within the temperature profile for (a) Wolfspeed C2M0025120D and (b) GaN Systems GS66516T.

temperature cycles, thus generated, are characterized by four plots given in Fig. 8 for each of the two semiconductor devices. These plots are:

- Cumulative energy loss in Joules for the load profile of Fig. 7b.
- Maximum junction temperature, in °C, computed across the load profile.
- Cumulative sum of amplitudes of all thermal cycles in Kelvin-cycles.

$$\sum \Delta T_j \cdot N(\Delta T_j, \sim). \tag{10}$$

- Cumulative sum of mean of all thermal cycles in Kelvin-cycles.

$$\sum T_{j,\text{mean}} \cdot N(\sim, T_{j,\text{mean}}). \tag{11}$$

The contour plots of the four characteristic factors of loss and temperature cycles for C2M0025120D are shown in Fig. 8a and those for GS66516T are shown in Fig. 8b. Many design points can be eliminated by placing a constraint on the maximum allowable junction temperature, which in this case is 150°C.

From the cumulative temperature cycle mean plots of the two devices, it is evident that the GS66516T runs at a higher mean temperature across most of the design space. Similarly, the cumulative cycle magnitude plots indicate that, in general, GS66516T suffers temperature cycles of larger magnitude which may result in greater lifetime consumption of the device. It is on account of lower thermal pad area and mass of GS66516T, despite having lower energy losses over given load profile.

VII. Calculation of Lifetime Consumption

A. Failure due to thermo-mechanical stresses

Thermo-mechanical stress in the bond-wire generated due to thermal cycles is the leading cause of failure in semiconductor devices. The temperature cycles counted using the rain-flow counting algorithm [12] are used to compute the lifetime consumption of the device; i.e., the number of temperature cycles (of specific amplitude and mean) at which the device will fail. The LESIT model (12), developed for silicon devices [5], combines the Arrhenius equation and Coffin-Manson's law to model the temperature dependency of the aforementioned failure mechanisms. It can also describe the lifetime model of SiC MOSFETs [7], [18].

$$N_f = A \cdot (\Delta T_j)^{-\alpha} \cdot \exp\left(\frac{E_a}{k \cdot (T_{j,\text{mean}} + \Delta T_j)}\right) \tag{12}$$

N_f is the number of temperature cycles to failure, A is the pre-exponential factor, E_a is the activation energy and k is Boltzmann constant. These factors are dependent on the semiconductor material, interface materials and package topology. The cumulative effect of the cycles constituting a thermal profile is the damage incurred by the device per load cycle, which is calculated using Miner's rule in (13).

$$D = \sum \left[(N(\Delta T_j, T_{j,\text{mean}}))/N_f\right] \tag{13}$$

N is the number of temperature cycles with amplitude, ΔT_j, and mean, $T_{j,\text{mean}}$. The model for failure of SiC devices due to thermo-mechanical stresses are extracted using power cycling tests, results of which are reported in [7]. The data from [7] are curve-fitted using the LESIT model (12) and its parameters are listed in Table V. The root mean square error (RMSE) is less than 0.2%.

The damage per load cycle is computed using (13). It is interpreted that the device is considered a failure when damage equals unity. Therefore, reciprocal of damage, D, is the number of load-cycles the semiconductor can continuously operate before failure. Therefore, mean-time to failure (MTTF) due to thermo-mechanical stresses is calculated using (14).

$$MTTF = \frac{T_{\text{load-cycle}}}{\sum \left[(N(\Delta T_j, T_{j,\text{mean}}))/N_f\right]} \tag{14}$$

TABLE V: Parameters of LESIT model for thermo-mechanical stresses in Wolfspeed devices curve-fitted to reported data [7].

Parameters	Value	95% confidence interval	
		Lower bound	Upper bound
A	1.254×10^9	1.771×10^8	2.33×10^9
α	5.072	5.316	4.827
E_a	0.4631 eV	0.449 eV	0.4772 eV

In GS66516T, the absence of bond-wires eliminates a major contributor to thermo-mechanical stress related failures. However, other thermo-mechanical stresses such as those due to different coefficients of thermal expansion (CTE) of GaN die and its silicon substrate are yet extant. The lifetime models for these devices are not yet reported in the literature; but, the method to calculate the failure rate for the given application may be used when the models are available.

B. Failure due to gate-oxide TDDB and drain-to-source HTRB

Besides thermo-mechanical stress related failures, other failure mechanisms such as gate-oxide TDDB and drain-to-source high temperature reverse bias (HTRB) are also a function of junction temperature and are modeled using Arrhenius equation [18]. If the accelerated failure tests conducted at reference junction temperature ($T_{j,\text{ref}}$) produced a failure rate of $MTTF(T_{j,\text{ref}})$, then the MTTF at operating temperatures are calculated by eliminating the acceleration factor.

$$MTTF(T_j) = MTTF(T_{j,\text{ref}}) \cdot \exp\Big(\frac{E_a}{k}(\frac{1}{T_j} - \frac{1}{T_{j,\text{ref}}})\Big) \tag{15}$$

The damage accumulated in the semiconductor device with respect to TDDB/HTRB failure mechanisms over the load profile is expressed as cumulative sum of damage incurred for each counted cycle.

$$\begin{aligned} D_{\text{TDDB/HTRB}} &= \sum \frac{t_{\text{prd}}}{MTTF(T_{j,\text{mean}})} \\ MTTF_{\text{TDDB/HTRB}} &= \frac{1}{D_{\text{TDDB/HTRB}}} \end{aligned} \tag{16}$$

As aforementioned, t_{prd} and $T_{j,\text{mean}}$ are the period and mean temperature of the thermal cycles counted using rain-flow counting algorithm.

VIII. Conclusions

In the paper, a dual active bridge (DAB) converter is considered as a basic power electronic building block (PEBB) across all heavy-duty vehicle platforms of the original equipment manufacturer (OEM). The concept of PEBB allows economies of scale in the low-volume industry. However, its use on different platforms may require disparate input voltage specifications. The paper proposes a load-profile based reliability-oriented design to ensure maximum availability of converter across all operating voltages and vehicle platforms. It is shown that the losses in semiconductor devices and their thermal response networks can be accurately modeled as mathematical expressions. The selected load profile and the loss models are used to generate junction temperature profiles. Finally, these profiles may be utilized to estimate the damage per load cycle and the MTTF for the semiconductor device. The process is repeated for every design point and an optimized design based on business needs may be selected.

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