A Variable Power Factor High Power Testbed for Traction Inverter Using Back-to-Back Connection

Yukun Luo
FREEDM Systems Center
North Carolina State University
yluo9@ncsu.edu

Li Yang
FREEDM Systems Center
North Carolina State University
lyang20@ncsu.edu

Juhamatti Korhonen
Laboratory of Applied Electronics
Lappeenranta University of Technology
Juhamatti.Korhonen@lut.fi

Wensong Yu
FREEDM Systems Center
North Carolina State University
wyu2@ncsu.edu

Iqbal Husain
FREEDM Systems Center
North Carolina State University
ihusain2@ncsu.edu

***Abstract*—A new inverter test method using back-to-back inverter power circulating strategy is presented in this paper. Using the method, high power test for traction inverter with wide power factor range can be achieved by selecting appropriate modulation scheme. The zero-sequence current issue inherent to the setup is investigated and addressed in order to improve the output current quality. Moreover, the similarities and the differences between the proposed setup and open-end winding motor drives are discussed. Experimental results verifying the high-power operation with wide power factor range achievable by the proposed method are provided.**

***Index Terms*—Traction Drive, Back-to-Back, Inverter test, Power Factor**

I. Introduction

The power rating of Electrical Vehicle (EV) traction drive can range from 30 kW to 250 kW [8-13], and the testing of these traction inverters with conventional R-L load are difficult and expensive. On the one hand, high rating power supply and load bank are needed for the entire operation range. While on the other hand, achieving tests with wide range of power factor requires good match between the inductor/resistor values and the fundamental frequency. Because of the limitations, many circulating test strategies have been used in practice. In [1,2], motor and generator emulator concept are proposed for the same inverter back-to-back setup as proposed in this paper achieving variable load conditions but only at a low power level and additional communication is needed. In [14,15], similar testing with circulating power have been implemented at an increased power level, but additional hardware, like dynamo-meter and transformers, are required. The circulating power test setup could also be used as a power system emulator as presented in [16]. In this paper, a testing method using similar topology as open-end-winding motor drive is used for circulating high power test on the traction inverter with high power flow control accuracy and full power factor range adjust ability. In the proposed method, no load bank is needed, and only a small DC power source to supply the system loss is required. With the modulation and control strategy proposed in the paper, high power level and full range (0 to 1) adjustable power factor can be achieved for the inverter under test simultaneously. The main contribution of this paper is the derivation and visualization of the relationship between achieved power factor and modulation parameters.

II. Topology and Operation Principle

The testing system consists of two back-to-back inverters with inductor load connected in between, as shown in Fig. 1. The basic idea is to adjust the voltage vectors of the two back-to-back connected inverters so that magnitude and phase angle of the voltage across inductor loads can be changed. In this way, the output power of Inverter 1 and power factor angle can be controlled. The concept is shown in Fig. 2, where V_1 and V_2 are the two voltage vectors modulated for Inverter 1 and Inverter 2 with magnitude of M_1 and M_2 and phase shift of θ. The voltage across inductor load will be the vector difference between V_1 and V_2. The inductor current orthogonal to inductor voltage will be away from V_1 by angle α, which to Inverter 1 is a load with cos (θ) power factor. Based on the strategy, the target apparent power output from Inverter 1 S_{INV1} can be calculated as:

$$S_{INV1} = \frac{3}{2} \cdot M_1 \cdot \left(\frac{U_{DC}}{2}\right)^2 \cdot \frac{\sqrt{M_1^2 + M_2^2 - 2 \cdot M_1 \cdot M_2 \cdot \cos(\theta)}}{2\pi f \cdot L} \quad (1)$$

The power factor under given modulation index M_1/M_2 and phase angle θ is:

$$PF = -\sin\left(\arctan\left(\frac{\sin(\theta)}{\frac{M_1}{M_2} - \cos(\theta)}\right)\right) \quad (2)$$

A 3D graph of power factor with respect to modulation index ratio M_1/M_2 and phase shift angle θ is plotted in Fig. 3(a) based on (2). The range of M_1/M_2 is chosen within range from 0 to 10, and phase shift angle θ is within -π to π. From the plotted figure, it can be seen that a wide power factor range is achievable. Based on (1), if M_1 is kept at 0.9, a 3D graph of apparent power (S) with respect to M_2 and phase shift angle Theta can also be plotted, as shown in Fig. 3(b) where U_{DC} = 600 V, fundamental frequency f = 95 Hz and load inductance is

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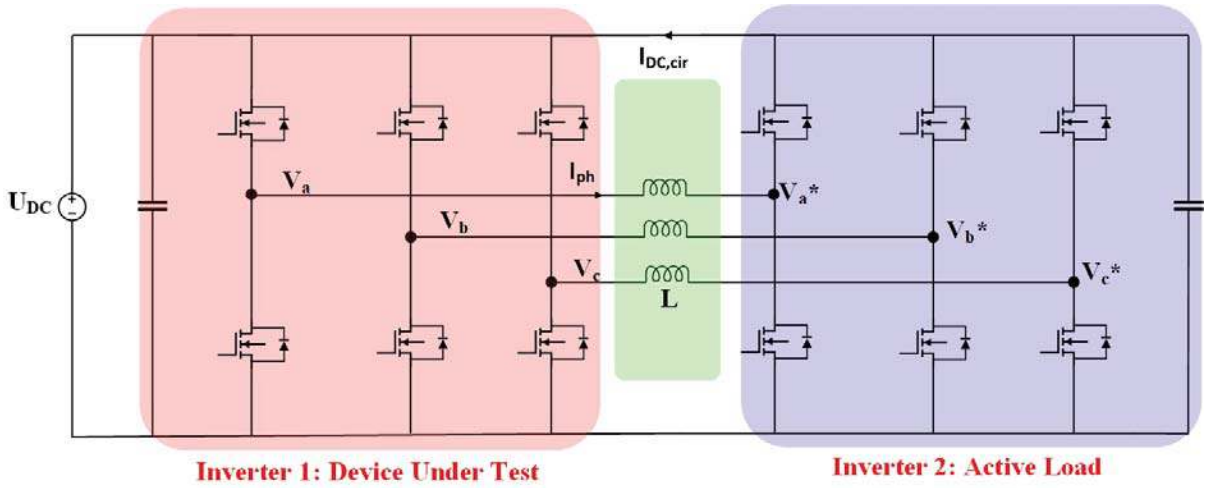


Fig. 1: Back-to-back inverter circulating test setup.

1.5 mH per phase. For practical implementation, phase current could be limited below system maximum value according to (3), the feasible operating region is then determined. Thus, by choosing proper modulation indexes and phase shift angle θ for the two inverters, the setup could be operated with a wide range of power factor and high output power level.

$$\left(\frac{U_{DC}}{2}\right)^2 \cdot \frac{\sqrt{M_1^2 + M_2^2 - 2 \cdot M_1 \cdot M_2 \cdot \cos(\theta)}}{2\pi f \cdot L} \leq I_{\max} \qquad (3)$$

III. ZSC Source and Suppression

A. Modulation Strategy

The main reason that sinusoidal PWM (SPWM), instead of space vector PWM (SVPWM), is chosen for this test setup is that SVPWM strategy would introduce huge zero-sequence current. The zero-sequence current (ZSC) issue is inherent to parallel three-phase inverters sharing only one DC power supply. As mentioned in previous works [3-5], the main source of ZSC are asynchronous carrier, zero sequence voltage introduced by PWM modulation and dead-band time. This issue has already been observed and discussed for open-end winding motor drive [3, 4, 6]. For open-end winding motor drive with SVPWM modulation, the reference voltages are modulated 120° phase shifted with the same magnitude in order to eliminate the zero-sequence voltage. However, for the testing purpose as in this paper, in order to change the power factor and power level of the inverters, the phase angle shift and modulation indexes need to be freely changed, which then generates zero sequence voltage. The effect is simulated in PSIM as shown in Fig. 4, where V_{ma} and V_{ma2} are the two reference voltages of the same phase leg for Inverter 1 and Inverter 2, while V_{ma}-V_{ma2} is the voltage applied across the inductor load. Fig. 4(a) shows the case where the two references have same magnitudes and 120° phase shift, while Fig. 4(b) shows the case where the two references have different magnitudes and phase shift of 45°. It can be seen that the inductor voltage will be sinusoidal for case (a). But inductor voltage will contain zero sequence components in case (b). Meaning only under the condition of same modulation index and 120° phase shift will two SVPWM modulated back-to-back inverters generate pure sinusoidal current in the load. According to [7], the harmonic injected in SVPWM is given by (4), which verifies that the harmonics could only be canceled if the phase angle shift is 120° and their modulation indexes are the same, otherwise there is zero sequence voltage applied on the load inductors, as illustrated in Fig. 4. Because of aforementioned limitations on SVPWM, SPWM is used in this application.

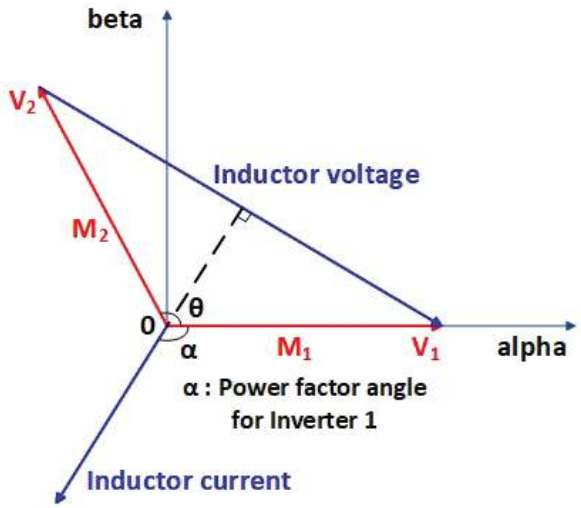
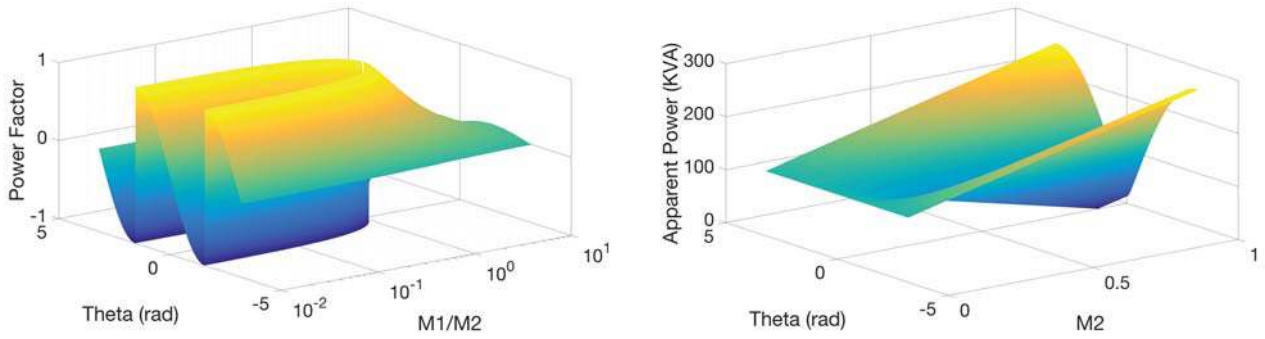
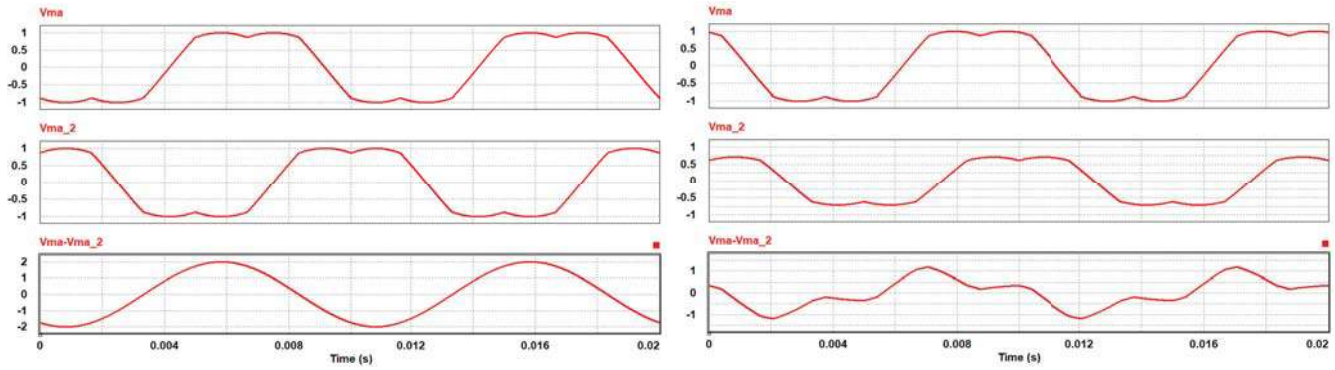


Fig. 2: Vector diagram.



(a) Power factor. (b) Apparent power.

Fig. 3: 3D plot of power factor and apparent power versus modulation indexes and phase shift angle.



(a) M_1=1, M_2=1, θ=120°. (b) Apparent power.

Fig. 4: zero sequence voltage generated by modulation scheme.

$$V_{ma} = MI \cdot \left[\sin(\omega t + \theta) + 0.25 \cdot \left(\sum_{i=0}^{N} (-1)^n \cdot n^{-2} \cdot \sin(3n(\omega t + \theta)) \right) \right] \quad (4)$$

$$(n = 2i + 1)$$

B. Deadband Time Effect

Incorporation of dead-band time into the inverter operation is another source of zero sequence current. In this paper, dead-band time compensation and zero-sequence PI controller [6] are both used. In order to have minimal modification on the device under test (Inverter 1), all the deadband time compensation and control algorithm are only applied to active load (Inverter 2). Therefore the device under test (Inverter 1) only has the simple open loop phase current control. In [3], the effect of dead-band time on zero-sequence voltage has been investigated. From switching cycle point of view, during dead-band time the current commutates through the body diode causing zero-sequence voltage. The average zero-sequence voltage over one switching period can be written as (5). Where t_D is the dead-band time, T_{sw} the switching period, and U_{DC} the DC link voltage. From fundamental cycle point of view, the polarity of zero-sequence voltage changes every 60° (fundamental frequency) as one of the three-phase load current changes polarity. The dead-band time compensation modifies each phases voltage reference based on each phases current polarity [5], the details are shown in Table I. The overall zero-sequence current control block diagram for Inverter 2 is shown in Fig. 5.

$$U_0 = \frac{2 \cdot t_D \cdot U_{DC}}{3 \cdot T_{sw}} \quad (5)$$

C. Carrier Synchronization

In the setup, two inverters are controlled by two individual DSPs, it is crucial to synchronize their carrier wave. Asynchronous carrier wave of the two controllers is the third source of ZSC. In order to eliminate the effect of asynchronous

TABLE I: Deadband Time Compensation Value

DB Comp Value	$I_n < 0$ (n = a,b,c)	$I_n \geq 0$ (n = a,b,c)
$U_{comp\ a,b,c}$	$-t_D/T_{sw}$	t_D/T_{sw}

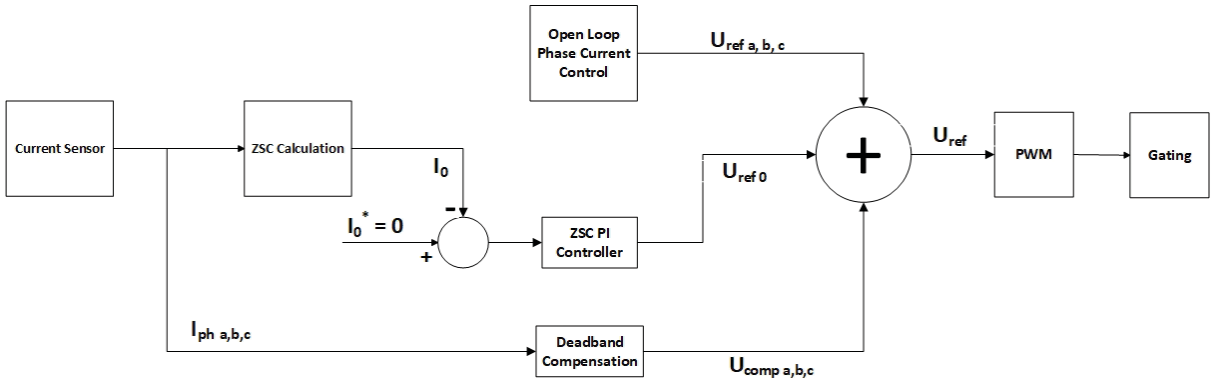


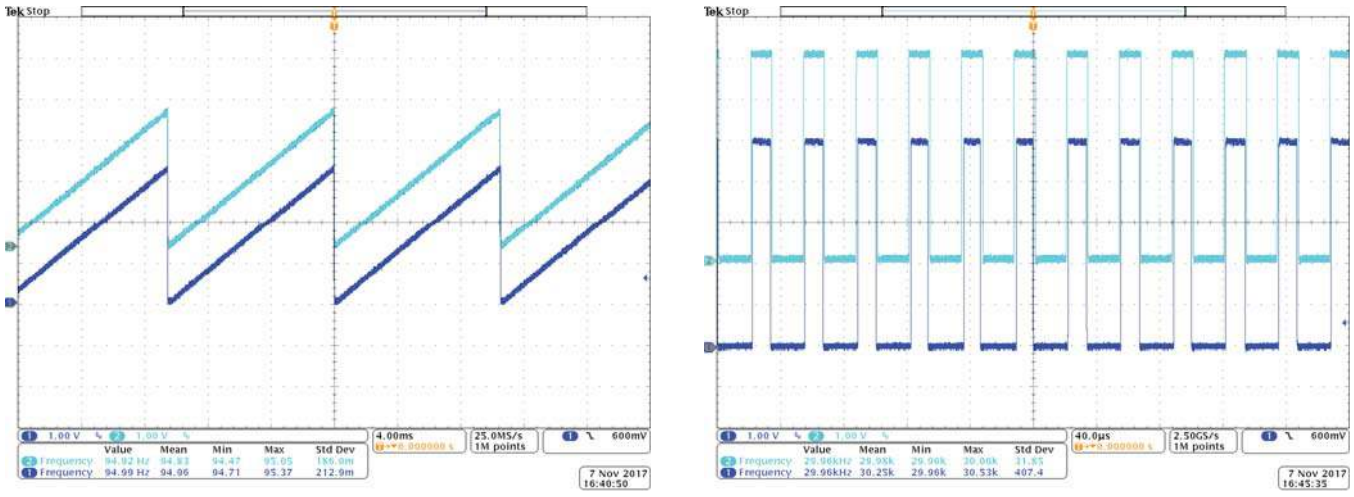
Fig. 5: ZSC suppression block diagram for Inverter 2.

carrier, external synchronization has to be adopted. From practical implementation point of view, phase angle of both voltage vectors (V_1 and V_2) modulated for each inverter has also to be synchronized. Because asynchronous phase angle of voltage vector V_1 and V_2 would result in unstable phase shift angle θ. If the carriers are aligned with each other, current ripple on the DC link as well as sinusoidal phase current output can be minimized [17]. In the previous works [1,2], the carrier synchronization and phase angle synchronization are realized via CAN communication and PLL respectively. In this work, however, two inverters are synchronized using one common external pulse signal of fundamental frequency. And a synchronization board is connected to both inverters with optical fiber cable. The function of the synchronization board is to generate and transmit the synchronization pulse at the fundamental frequency of sine waves. For the phase angle synchronization, two controller DSPs execute their phase angles incremental with the same frequency, and when the external pulse is detected, both DSP reset their phase angle to zero. Thus, the phase angle is synchronized once every fundamental cycle. As for the carrier wave, the external pulse signal is connected to the synchronization inputs of EPWM module of both DSPs such that whenever there is pulse coming from the synchronization board, the carriers of the two DSPs are reset by hardware. The synchronized phase angle and PWM carrier wave are shown in Fig. 6(a) and Fig. 6(b) respectively.

IV. Experimental Results

A. ZSC Suppression

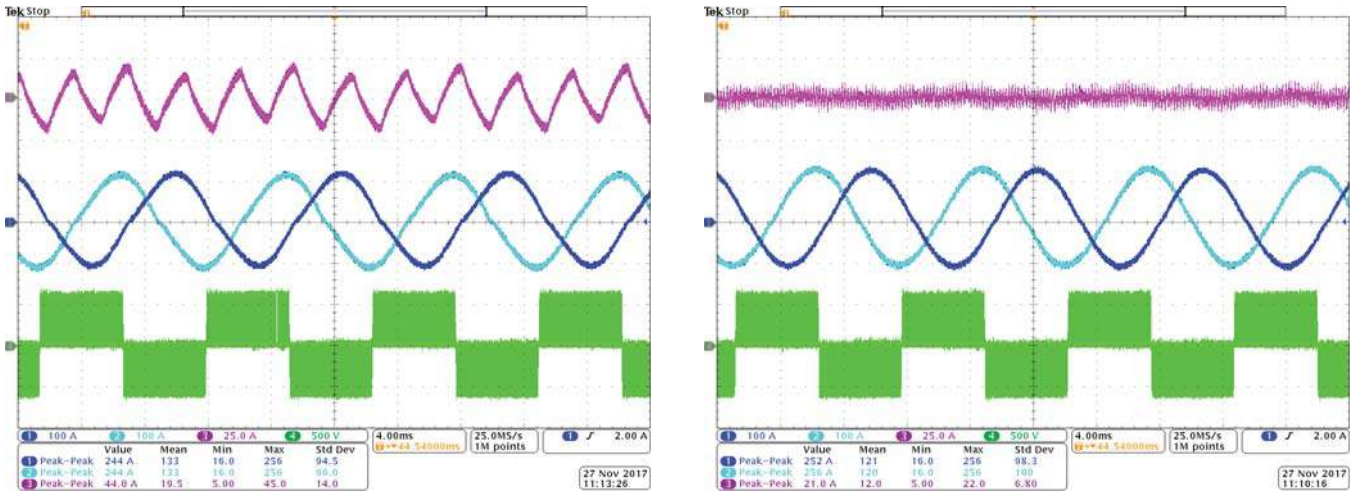
To verify the proposed inverter testing method, a setup consists of two high power inverters utilizing SiC devices with liquid cooling is built. The testing parameters are listed in Table. II. The overall ZSC suppression strategy block diagram is shown in Fig. 5. The effectiveness of ZSC suppression strategies is verified via experiment first. In this test, the modulation indexes of Inverter 1 and Inverter 2 are kept at 0.2 and the phase shift angle θ is set to be 120°. The results are shown in Fig. 7(a) and Fig. 7(b) respectively with ZSC suppression disabled and enabled. From the experimental



(a) Phase angle synchronization.

(b) Carrier wave synchronization. (Shown via PWM)

Fig. 6: Synchronization verification.



(a) ZSC suppression disabled.

(b) ZSC suppression enabled.

Fig. 7: ZSC suppression result. CH1, CH2: phase current, CH3: ZSC (x3), CH4: phase to phase voltage (V_{ab}) of Inverter 1.

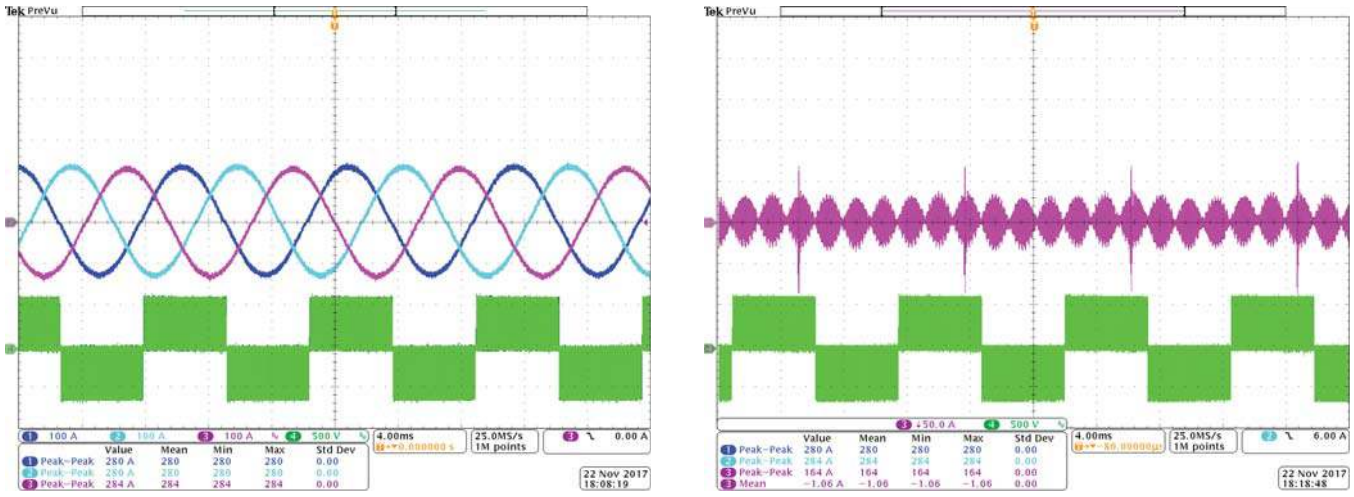
results, the third harmonic in ZSC is significantly reduced and the peak-to-peak value of three phase current summation (*i.e.*, three times the ZSC) is reduced from 44 A to 21 A. Evident to see that with the ZSC suppression algorithm, the quality of sinusoidal phase current gets improved significantly.

TABLE II: Back-to-back Inverter Test Setup Parameters

Parameters	Value
DC Link Voltage (U_{DC})	600 V
Switching Frequency ($1/T_{sw}$)	30 kHz
Fundamental Frequency (f)	95 Hz
Load Inductance (L)	1.5 mH
Phase Current Limit (I_{max})	130 A
Dead-band Time (t_D)	600 ns
Inverter 2 ZSC PI controller proportional term (K_P)	4.8
Inverter 2 ZSC PI controller integral term (K_I)	0.048

B. Variable Power Factor Operation

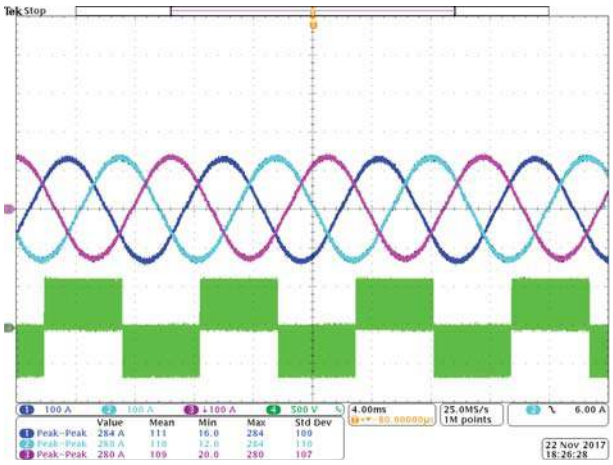
In order to verify the proposed variable power factor testing method, experiments were designed as follow. The maximum system apparent power and maximum phase current amplitude are set as 45 kVA and 130 A respectively, considering the actual test setup parameters and ratings. Then four theoretical power factor operation points 0, 0.5, 0.866 and 1 are selected. Based on the constraints above, the combination of modulation indexes M_1, M_2 and angle θ could be calculated according to (1)-(3), shown in Table. III. In this way, all the setting parameters under various power factor operation could be obtained. The relation between achieved apparent power of Inverter 1 S_{INV1} and modulation index M_1 is described in (6). And by measuring the DC circulating current $I_{DC,cir}$ (labeled in Fig. 1), the real power circulating within the system can be



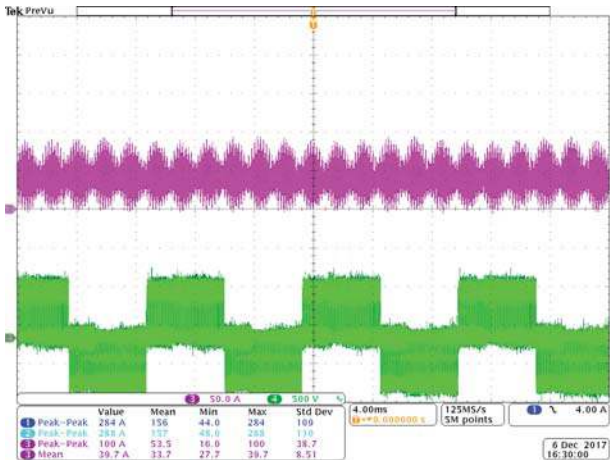
(a) Three-phase current and phase-to-phase voltage V_{ab}.

(b) DC circulating current $I_{DC,cir}$ and phase-to-phase voltage V_{ab}.

Fig. 8: PF = 0.

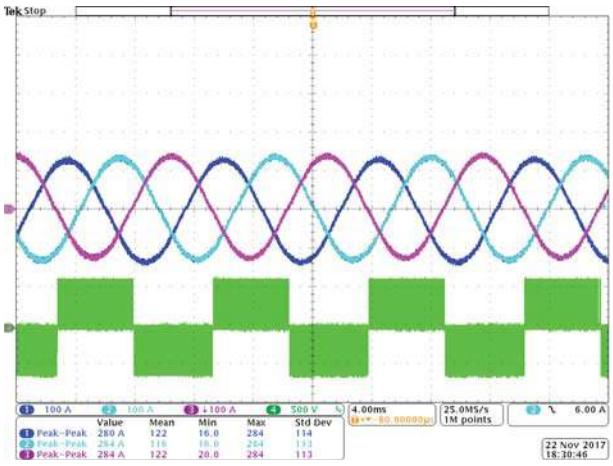


(a) Three-phase current and phase-to-phase voltage V_{ab}.

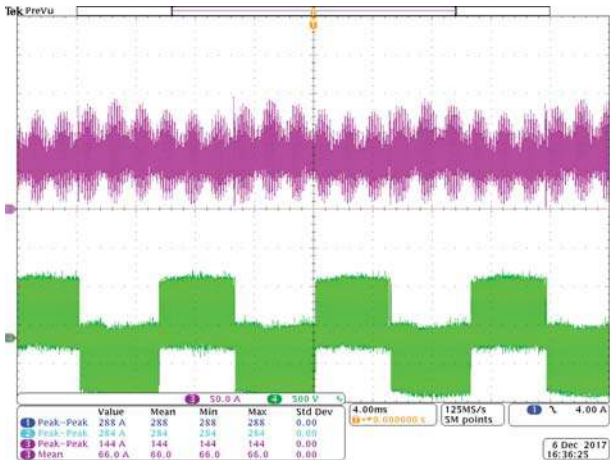


(b) DC circulating current $I_{DC,cir}$ and phase-to-phase voltage V_{ab}.

Fig. 9: PF = 0.5.

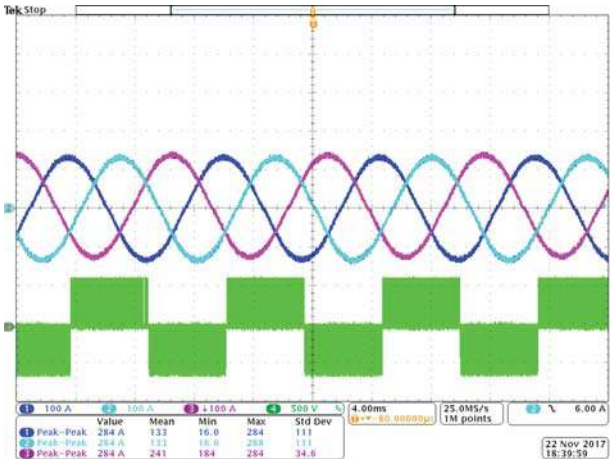


(a) Three-phase current and phase-to-phase voltage V_{ab}.

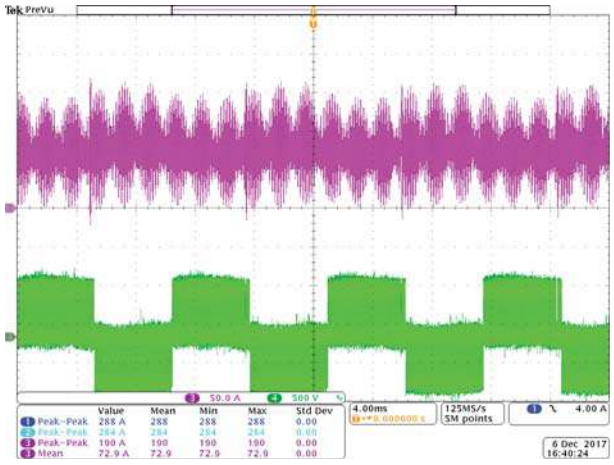


(b) DC circulating current $I_{DC,cir}$ and phase-to-phase voltage V_{ab}.

Fig. 10: PF = 0.866.



(a) Three-phase current and phase-to-phase voltage V_{ab}.



(b) DC circulating current $I_{DC,cir}$ and phase-to-phase voltage V_{ab}.

Fig. 11: PF = 1.

TABLE III: Comparison between theoretical calculation and experimental results

Target PF	Target S_{INV1}	M_1	M_2	θ	Actual S_{INV1}	I_{ph}	$I_{DC,cir}$	P_{cir}	P_{loss}	Actual PF
0	45 kVA	0.7692	0.3813	0°	45.00 kVA	130 A	1.1 A	0.66 kW	3.00 kW	0.048
0.5	45 kVA	0.7692	0.4747	24.122°	45.00 kVA	130 A	39.7 A	23.82 kW	3.00 kW	0.563
0.866	45 kVA	0.7692	0.6662	30.288°	45.34 kVA	131 A	66.0 A	39.60 kW	3.06 kW	0.907
1	45 kVA	0.7692	0.8615	26.765°	45.69 kVA	132 A	72.9 A	43.74 kW	3.12 kW	0.991

calculated according to (7).

$$S_{INV1} = \frac{3}{2} \cdot \frac{U_{DC}}{2} \cdot M_1 \cdot I_{ph} \tag{6}$$

$$P_{cir} = U_{DC} \cdot I_{DC,\,cir} \tag{7}$$

Thus, the theoretical power factor could be verified against the experimental results. The experimental results for 0, 0.5, 0.866, and 1 power factor operation are shown from Fig. 8 to Fig. 11 respectively. It can be seen that the peak-to-peak ripple in phase current is around 20 A, which causes difference between current peak value and amplitude. From averaging point of view, during power calculation, the current amplitude should be used. The comparison of theoretical calculation and experimental results for these four cases is shown in Table. III. The actual power factor can be calculated according to (8). One can assume the power supplied by the DC source is equal to the sum of power loss over two inverters and load inductors. In this way, the power loss on Inverter 1 could be obtained. After analyzing the experimental results, there are several phenomenon worth noting. First, there is some slight DC offset within three-phase current shown in Fig. 8(a) to Fig. 11(a). Second, the phase current amplitude has small error with regard to reference value 130 A under 0.866 and 1 power factor operation scenarios. These two are due to the fact that open loop phase current control is utilized as shown in Fig. 5. A more accurate close loop phase current controller would mitigate the DC offset and static error. Also, the envelop of DC circulating current $I_{DC,cir}$ is three times the fundamental frequency. While the high frequency current ripple is introduced by the switching of the MOSFET. Moreover, higher real power require higher DC current ripple to circulate energy within the system. From Table. III, one can see that the theoretically calculated power factor is matching with the experimental results pretty closely. However, slight error do exist, which is mainly contributed by the parasitic resistance of the load inductors.

$$Actual\ PF = \frac{P_{cir} + 0.5P_{loss}}{S_{INV1}} \tag{8}$$

V. Conclusion and Future Work

From the experimental results shown above, high power level variable power factor operation of the traction inverter can be achieved utilizing back-to-back topology, which eliminate the need for high capacity bidirectional power supply, huge load bank and dynamo-meter setup. Also, no additional communication protocol between two inverters is required to suppress the zero-sequence current, introduced by asynchronous phase angle and carrier wave of the controllers of the two inverters. Appropriate PWM scheme and dead-band time compensation are used to mitigate other sources of zero-sequence current in the system. However, some DC offset between three phase current and static current error do exist. In the future, a variable power factor control scheme utilizing close loop current controller could be developed to address this issue.

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