# NCSU Breakthroughs in SiC Power MOSFET Technology

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Acknowledgements

# Outline

- SiC Power MOSFET Breakthroughs achieved at NCSU
  - PRESiCE: SiC Power Device Manufacturing Technology
  - SiC Power MOSFETs: Inversion Channel & Accumulation Channel
  - The JBSFET: SiC MOSFET with Integrated Schottky Diode
  - Split-Gate (SG) MOSFET: Improved HF-FOM
  - Buffered-Gate (BG) MOSFET: Further Improved HF-FOM
  - The OCTFET: A New Cell Topology with Superior High Frequency Figures-of-Merit
  - The BiDFET: A Monolithic Bi-Directional Field Effect Transistor

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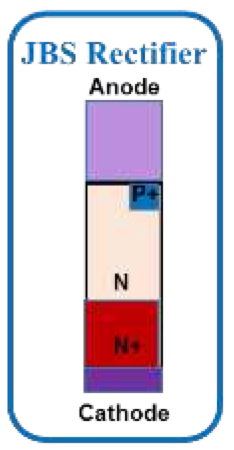
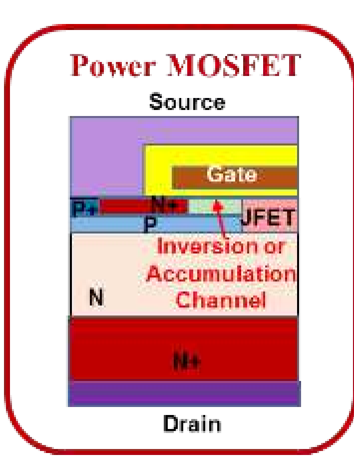
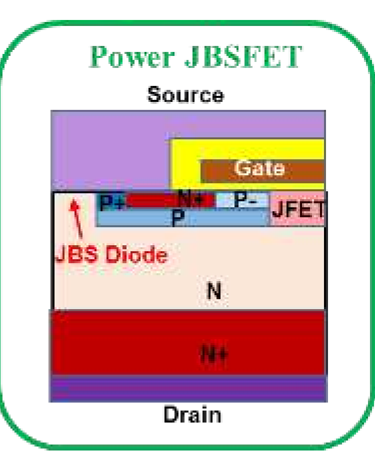
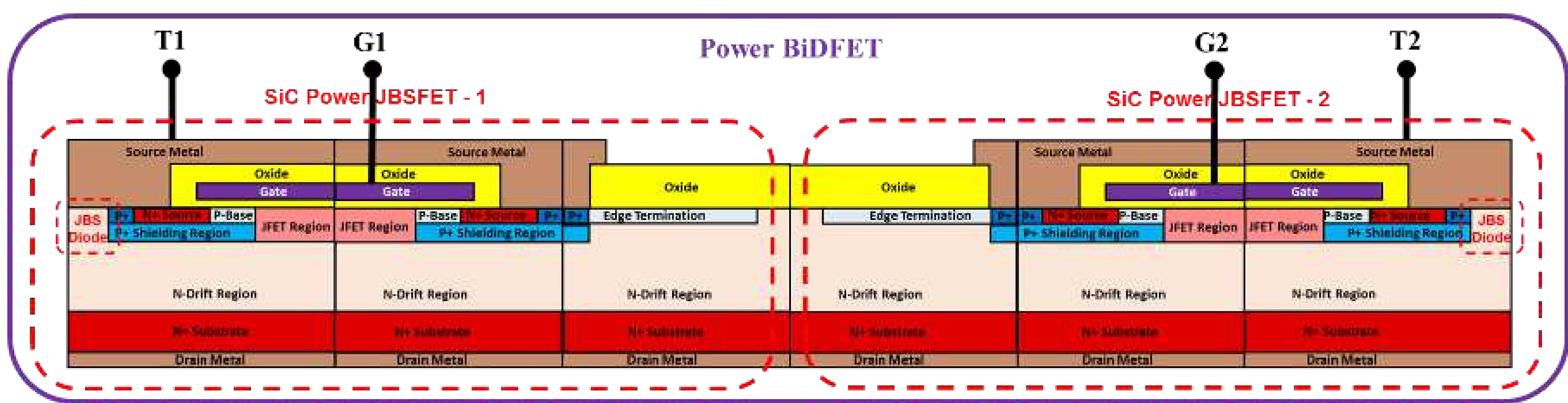
# PRESiCE: PRocess Engineered for manufacturing SiC Electronic-Devices

## SiC Power Electronic-Devices




B.J. Baliga, et al, "PRESiCE™: Process Engineered for manufacturing SiC Electronic-Devices", *Int. Conf. on Silicon Carbide and Related Materials*, Paper MO.CP.10, September 18, 2017.

# PRESiCE: PRocess Engineered for manufacturing SiC Electronic-Devices

**Qualification Procedure:**

(1) Define Process Flow (NCSU) for Manufacturing SiC Power MOSFETs, JBSFETs, and JBS Rectifiers at X-Fab.

(2) Design a Mask Set (NCSU) for Manufacturing SiC Power MOSFETs, JBSFETs, and JBS Rectifiers at X-Fab for Qualifying the process.

(3) Fabricated Three Process Lots at X-Fab.

(4) Obtained Statistical Data (NCSU) on device parameters to confirm tight distribution of parameters from within each wafer, from wafer-to-wafer within each process lot, and from lot-to-lot.

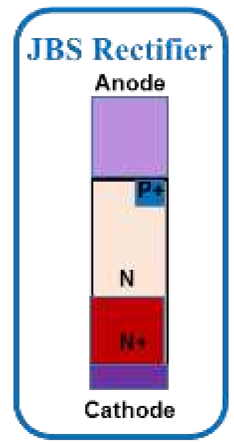
**Data Acquisition Equipment:**

(1) New Semi-Automated Signatone Wafer Prober.
- 6 inch wafer capability
- 3 kV chuck isolation
- High Temp (300 oC)

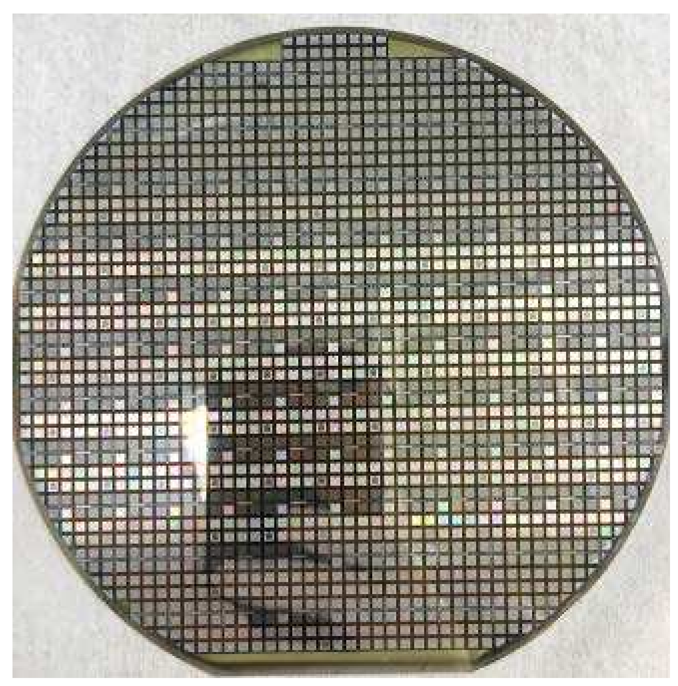
(2) New Keysight Test Equipment.
- Maximum Voltage = 3 kV
- Maximum Current = 20 A

# 1.2 kV JBS Rectifier Process Qualification

- Process Qualification using Three Lots at X-Fab
- Device #2: JBS Rectifier with Nickel Schottky Contact
  - Active Area = 0.046 cm2




W. Sung, K. Han and B.J. Baliga, "Design and Manufacturing of 1200 V SiC JBS Diodes with Low On-State Voltage Drop and Reverse Blocking Leakage Current", *Int. Conf. on Silicon Carbide and Related Materials*, Paper WE.DP.9, September 20, 2017.

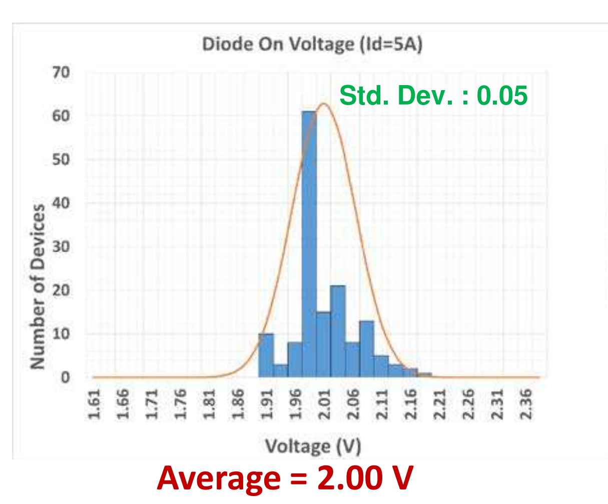


6 inch SiC wafer fabricated at X-Fab

# JBS Rectifier with Nickel Schottky Contact (Within Lot Variation)

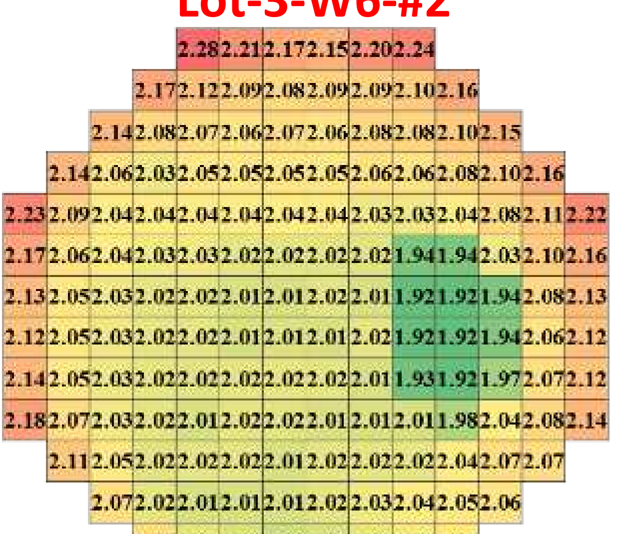
## On-state Voltage Drop [V] @ If = 5A

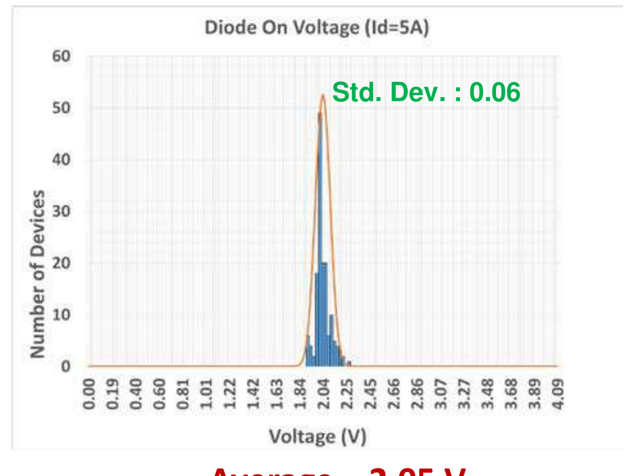
### Lot-3-W3-#2




**Average = 2.00 V**

### Lot-3-W6-#2

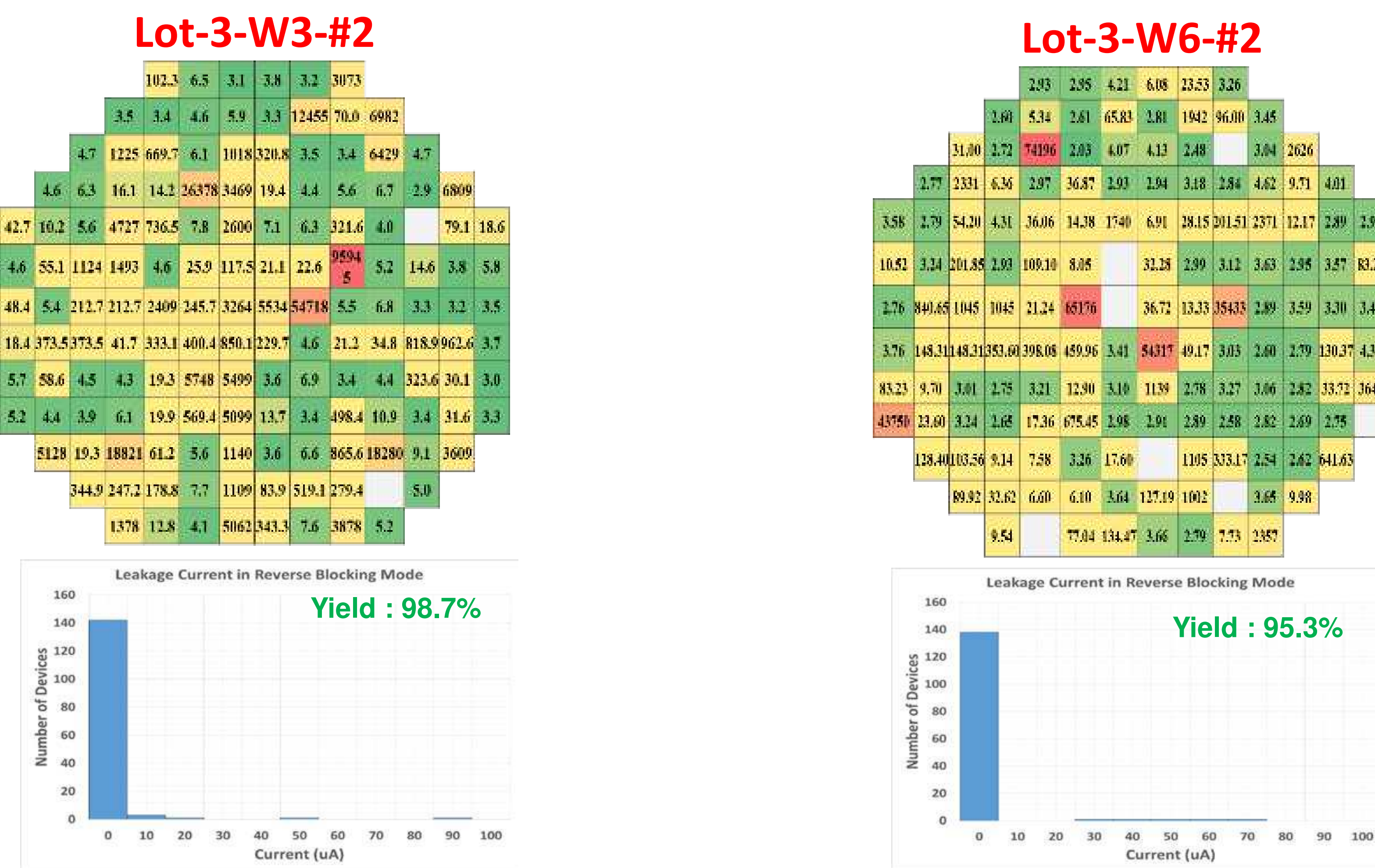



**Average = 2.05 V**

# JBS Rectifier with Nickel Schottky Contact (Within Lot Variation)

## Leakage Current ($I_L$) [nA] @ Vd=1000 V, RT




**<u>Yield based on allowable maximum leakage current of 100 μA</u>**

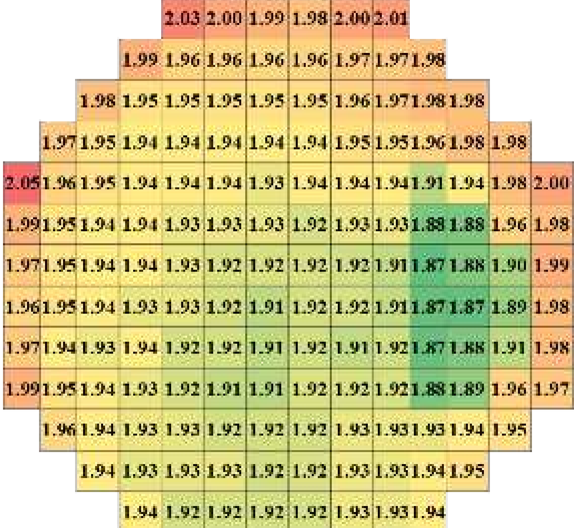
# JBS Rectifier with Nickel Schottky Contact (Lot-to-Lot Variation)

## On-state Voltage Drop [V] @ if = 5A, RT

### Lot-3-W3-#2

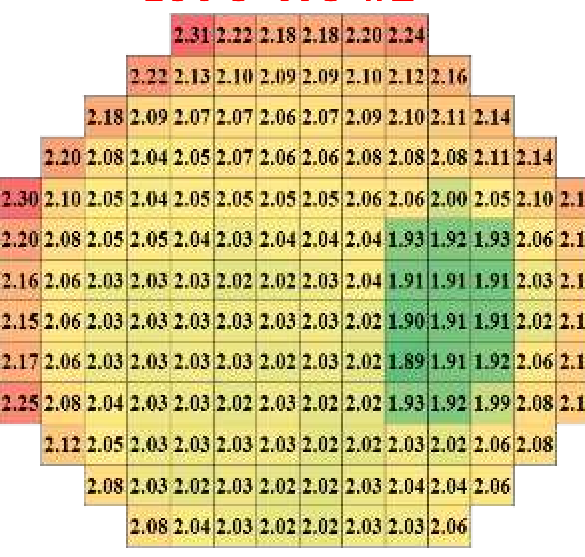
| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 2.18 | 2.12 | 2.08 | 2.09 | 2.11 | 2.15 | | | | |
| | | | 2.10 | 2.05 | 2.03 | 2.01 | 2.02 | 2.04 | 2.05 | 2.09 | | | |
| | | 2.07 | 2.02 | 2.00 | 2.00 | 2.00 | 2.01 | 2.02 | 2.03 | 2.05 | 2.08 | | |
| | 2.07 | 2.02 | 1.98 | 1.98 | 1.98 | 1.98 | 1.99 | 1.99 | 2.01 | 2.03 | 2.05 | 2.08 | |
| 2.14 | 2.03 | 1.99 | 1.98 | 1.98 | 1.98 | 1.97 | 1.98 | 1.98 | 1.98 | 1.99 | 2.03 | 2.06 | 2.13 |
| 2.09 | 2.01 | 1.98 | 1.97 | 1.97 | 1.96 | 1.96 | 1.98 | 1.97 | 1.90 | 1.90 | 1.93 | 2.05 | 2.08 |
| 2.06 | 1.99 | 1.97 | 1.97 | 1.97 | 1.96 | 1.96 | 1.97 | 1.97 | 1.89 | 1.89 | 1.90 | 2.02 | 2.06 |
| 2.05 | 1.99 | 1.97 | 1.96 | 1.96 | 1.96 | 1.96 | 1.96 | 1.97 | 1.89 | 1.89 | 1.90 | 2.01 | 2.06 |
| 2.06 | 1.99 | 1.97 | 1.96 | 1.95 | 1.96 | 1.96 | 1.97 | 1.96 | 1.89 | 1.89 | 1.91 | 2.02 | 2.06 |
| 2.09 | 2.01 | 1.98 | 1.96 | 1.95 | 1.95 | 1.96 | 1.96 | 1.96 | 1.96 | 1.92 | 1.98 | 2.03 | 2.06 |
| | 2.04 | 2.00 | 1.97 | 1.96 | 1.96 | 1.95 | 1.96 | 1.97 | 1.97 | 1.98 | 2.01 | 2.02 | |
| | | 2.01 | 1.98 | 1.96 | 1.96 | 1.96 | 1.97 | 1.98 | 1.98 | 2.00 | 2.01 | | |
| | | | 2.00 | 1.96 | 1.94 | 1.96 | 1.97 | 1.98 | 1.98 | 2.00 | | | |

### Lot-4-W3-#2

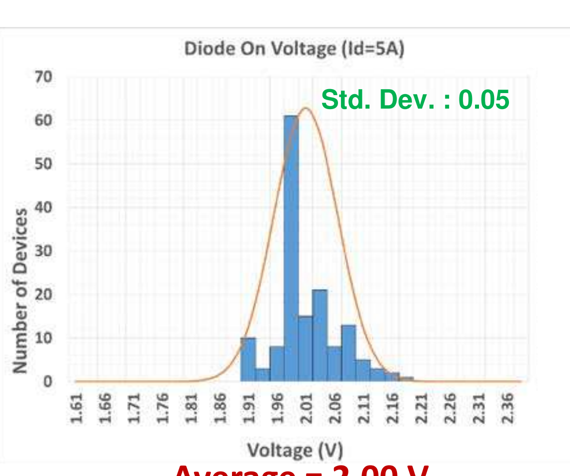


| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 2.03 | 2.00 | 1.99 | 1.98 | 2.00 | 2.01 | | | | |
| | | | 1.99 | 1.96 | 1.96 | 1.96 | 1.96 | 1.97 | 1.97 | 1.98 | | | |
| | | 1.98 | 1.95 | 1.95 | 1.95 | 1.95 | 1.95 | 1.96 | 1.97 | 1.98 | 1.98 | | |
| | 1.97 | 1.95 | 1.94 | 1.94 | 1.94 | 1.94 | 1.94 | 1.95 | 1.95 | 1.96 | 1.98 | 1.98 | |
| 2.05 | 1.96 | 1.95 | 1.94 | 1.94 | 1.94 | 1.93 | 1.94 | 1.94 | 1.94 | 1.91 | 1.94 | 1.98 | 2.00 |
| 1.99 | 1.95 | 1.94 | 1.94 | 1.93 | 1.93 | 1.93 | 1.92 | 1.93 | 1.93 | 1.88 | 1.88 | 1.96 | 1.98 |
| 1.97 | 1.95 | 1.94 | 1.94 | 1.93 | 1.92 | 1.92 | 1.92 | 1.92 | 1.91 | 1.87 | 1.88 | 1.90 | 1.99 |
| 1.96 | 1.95 | 1.94 | 1.93 | 1.93 | 1.92 | 1.91 | 1.92 | 1.92 | 1.91 | 1.87 | 1.87 | 1.89 | 1.98 |
| 1.97 | 1.94 | 1.93 | 1.94 | 1.92 | 1.92 | 1.91 | 1.92 | 1.91 | 1.92 | 1.87 | 1.88 | 1.91 | 1.98 |
| 1.99 | 1.95 | 1.94 | 1.93 | 1.92 | 1.91 | 1.91 | 1.92 | 1.92 | 1.92 | 1.88 | 1.89 | 1.96 | 1.97 |
| | 1.96 | 1.94 | 1.93 | 1.93 | 1.92 | 1.92 | 1.92 | 1.93 | 1.93 | 1.93 | 1.94 | 1.95 | |
| | | 1.94 | 1.93 | 1.93 | 1.93 | 1.92 | 1.92 | 1.93 | 1.93 | 1.94 | 1.95 | | |
| | | | 1.94 | 1.92 | 1.92 | 1.92 | 1.92 | 1.93 | 1.93 | 1.94 | | | |

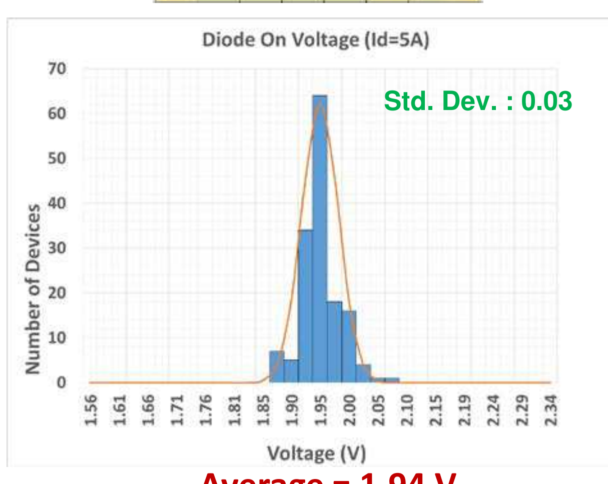
### Lot-5-W3-#2



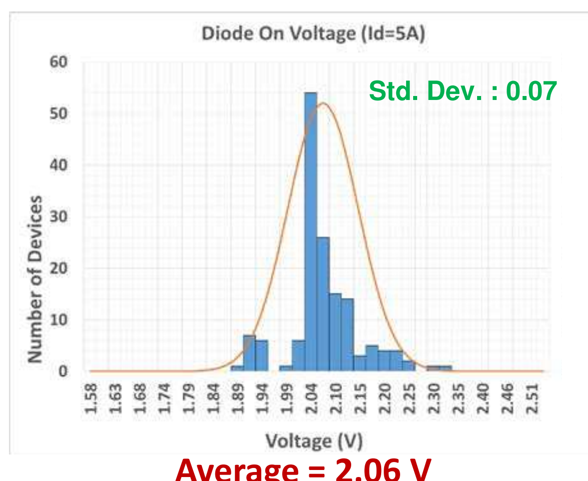
| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 2.31 | 2.22 | 2.18 | 2.18 | 2.20 | 2.24 | | | | |
| | | | 2.22 | 2.13 | 2.10 | 2.09 | 2.09 | 2.10 | 2.12 | 2.16 | | | |
| | | 2.18 | 2.09 | 2.07 | 2.07 | 2.06 | 2.07 | 2.09 | 2.10 | 2.11 | 2.14 | | |
| | 2.20 | 2.08 | 2.04 | 2.05 | 2.07 | 2.06 | 2.06 | 2.08 | 2.08 | 2.08 | 2.11 | 2.14 | |
| 2.30 | 2.10 | 2.05 | 2.04 | 2.05 | 2.05 | 2.05 | 2.05 | 2.06 | 2.06 | 2.00 | 2.05 | 2.10 | 2.17 |
| 2.20 | 2.08 | 2.05 | 2.05 | 2.04 | 2.03 | 2.04 | 2.04 | 2.04 | 1.93 | 1.92 | 1.93 | 2.06 | 2.11 |
| 2.16 | 2.06 | 2.03 | 2.03 | 2.03 | 2.02 | 2.02 | 2.03 | 2.04 | 1.91 | 1.91 | 1.91 | 2.03 | 2.10 |
| 2.15 | 2.06 | 2.03 | 2.03 | 2.03 | 2.03 | 2.03 | 2.03 | 2.02 | 1.90 | 1.91 | 1.91 | 2.02 | 2.10 |
| 2.17 | 2.06 | 2.03 | 2.03 | 2.03 | 2.03 | 2.02 | 2.03 | 2.02 | 1.89 | 1.91 | 1.92 | 2.06 | 2.11 |
| 2.25 | 2.08 | 2.04 | 2.03 | 2.03 | 2.02 | 2.03 | 2.02 | 2.02 | 1.93 | 1.92 | 1.99 | 2.08 | 2.11 |
| | 2.12 | 2.05 | 2.03 | 2.03 | 2.03 | 2.03 | 2.02 | 2.02 | 2.03 | 2.02 | 2.06 | 2.08 | |
| | | 2.08 | 2.03 | 2.02 | 2.03 | 2.02 | 2.02 | 2.03 | 2.04 | 2.04 | 2.06 | | |
| | | | 2.08 | 2.04 | 2.03 | 2.02 | 2.02 | 2.03 | 2.03 | 2.06 | | | |




Average = 2.00 V



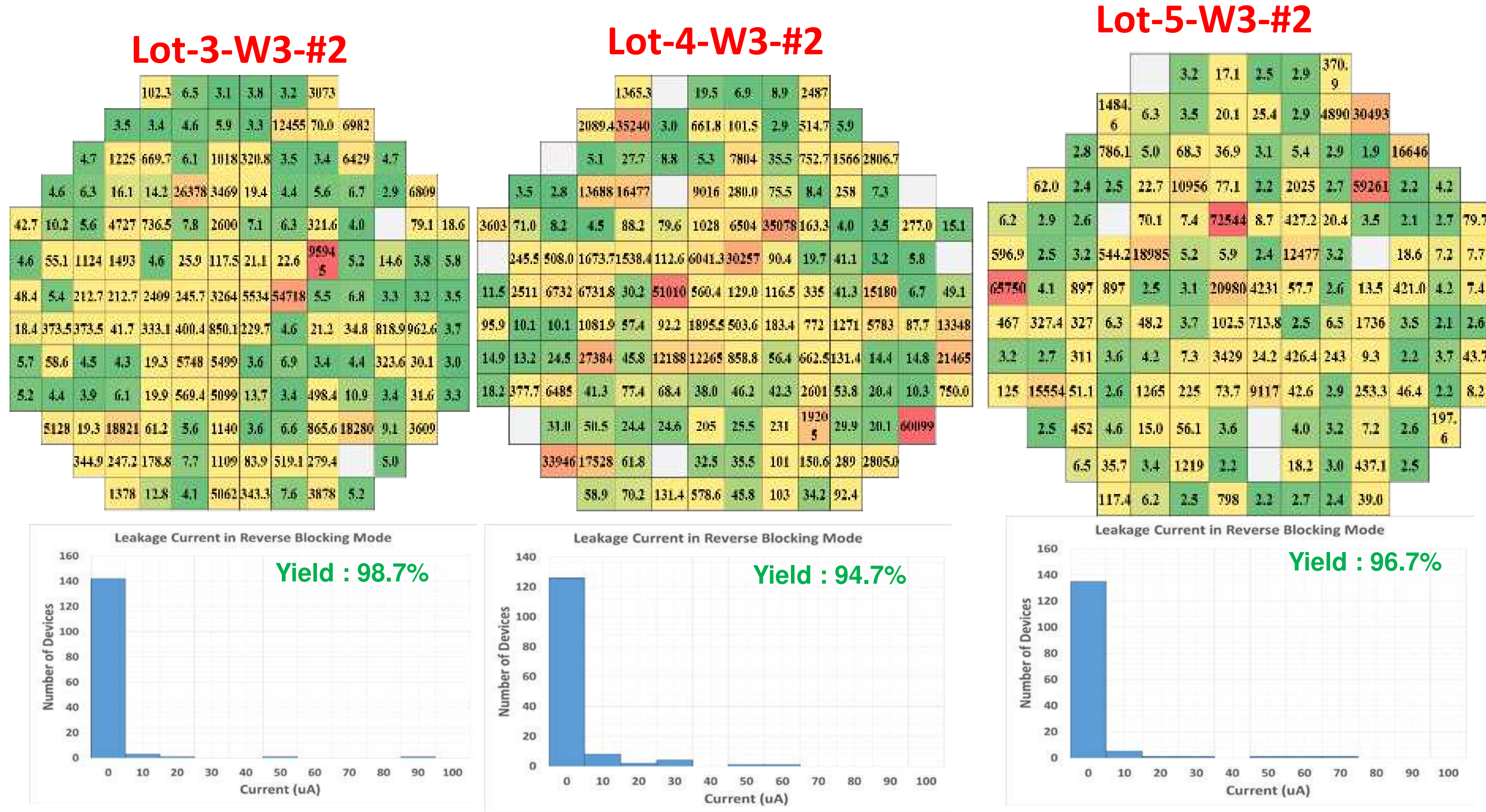

Average = 1.94 V




Average = 2.06 V

# JBS Rectifier with Nickel Schottky Contact (Lot-to-Lot Variation)

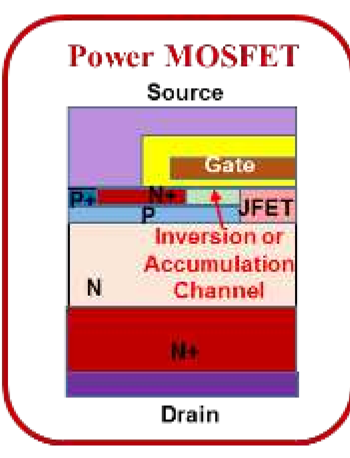
## Leakage Current ($I_L$) [nA] @ Vd=1000 V, RT




**Yield based on allowable maximum leakage current of 100 µA**

# Accumulation Channel MOSFET (ACCUFET)

- Process Qualification using Three Process Lots at X-Fab
- Device #5: Accumulation Channel MOSFET (ACCUFET) with JFET Implant
  - Active Area = 0.045 cm2




W. Sung, K. Han and B.J. Baliga, "A Comparative Study of Channel Designs for SiC MOSFETs: Accumulation-Mode Channel vs Inversion-Mode Channel", *IEEE Int. Symp. On Power Semiconductor Devices and ICs*, Paper SiC-P9, pp. 375-378, June 2017, Sapporo, Japan.

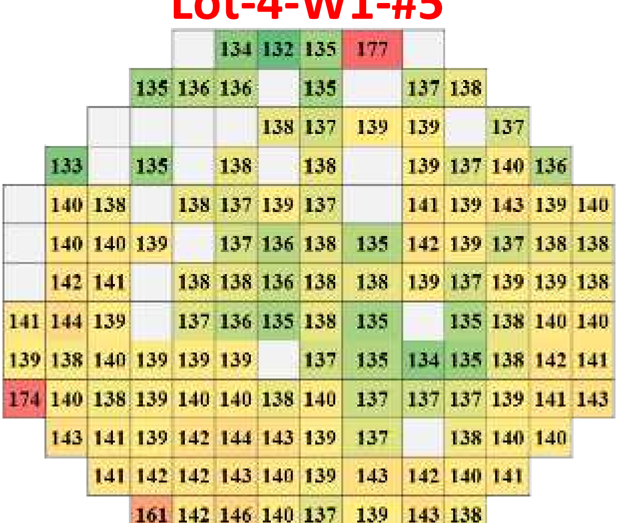
<u>Technical Note</u>:

- The Rds,on values in the Wafer Maps and Statistical Data plots include 35 mΩ of parasitic probe (~ 1 mΩ-cm2) and substrate (~ 1 mΩ-cm2) resistance.
- The Cgd values in Wafer Maps and Statistical data include 0.5 pF of parasitic probe capacitance.

# Accumulation Channel MOSFET (ACCUFET) (Within Lot Variation)

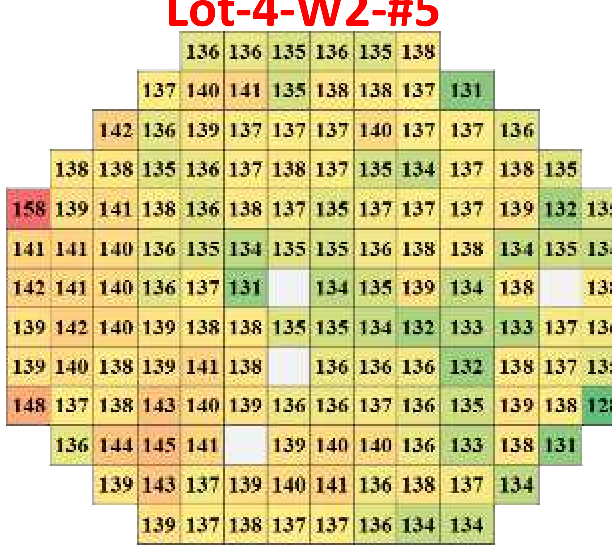
## On-Resistance ($R_{on}$) [mΩ] @ Id=1A, Vg=25V, RT - 6.5 mΩ-cm2

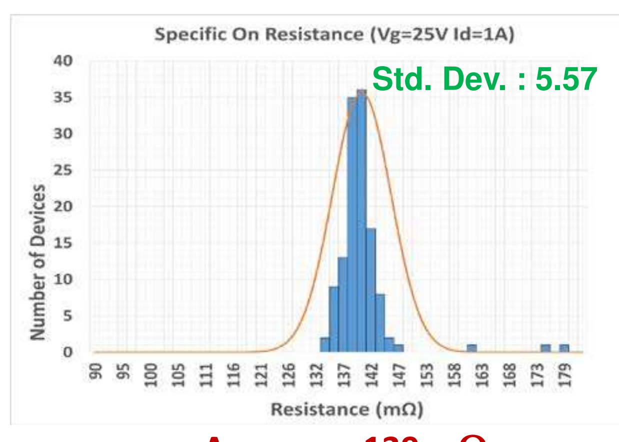
**Lot-4-W1-#5**




☐ Damaged during the BV test w/o Flourinert

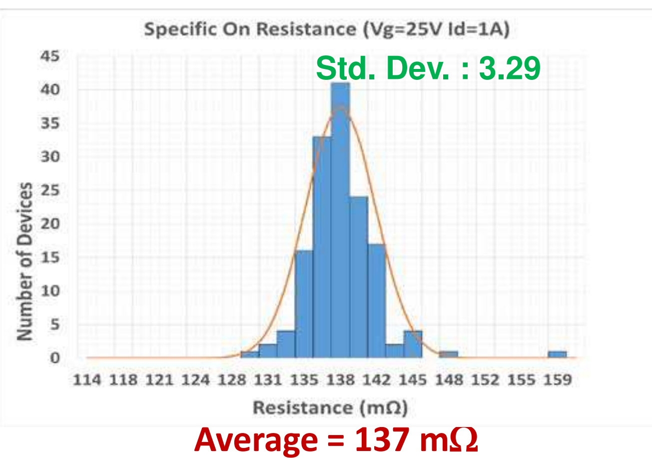
**Lot-4-W2-#5**




Average = 139 mΩ

**Typical value is the Average of All Devices from All Three Lots**



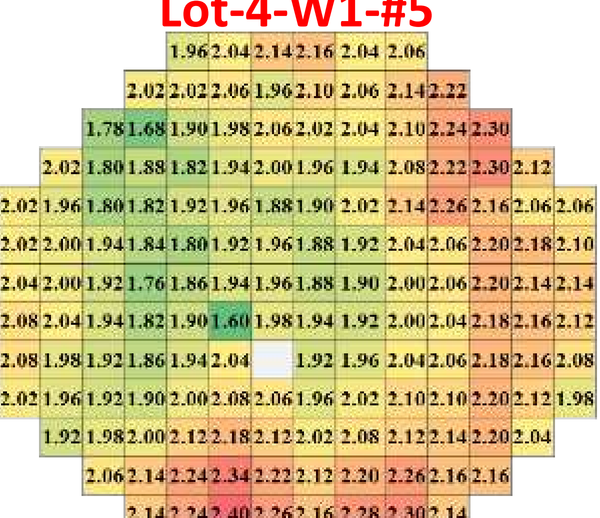

Average = 137 mΩ

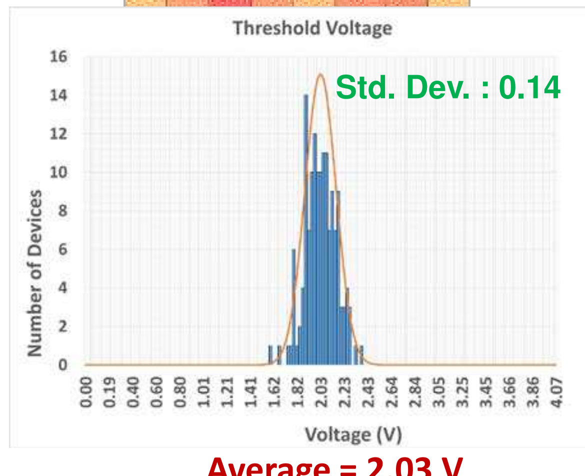
**Typical: 144 mΩ (Allowable Max : 187 mΩ (30 % more)) ➔ All devices meet specifications**

# Accumulation Channel MOSFET (ACCUFET) (Within Lot Variation)

## Threshold Voltage ($V_{th}$) [V] @ Id = 1 mA, Vd = 0.1 V, RT

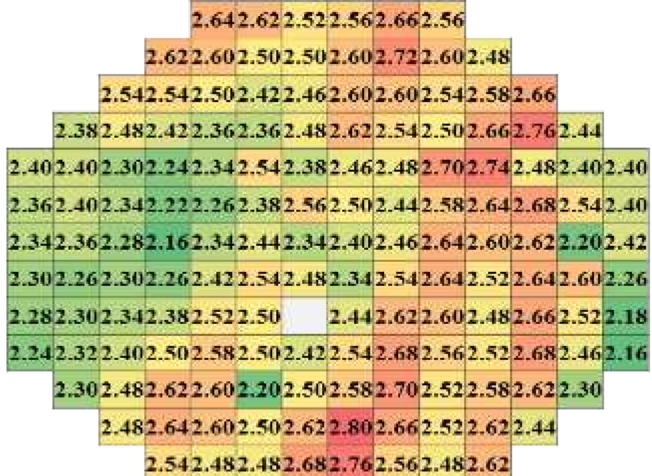
### Lot-4-W1-#5

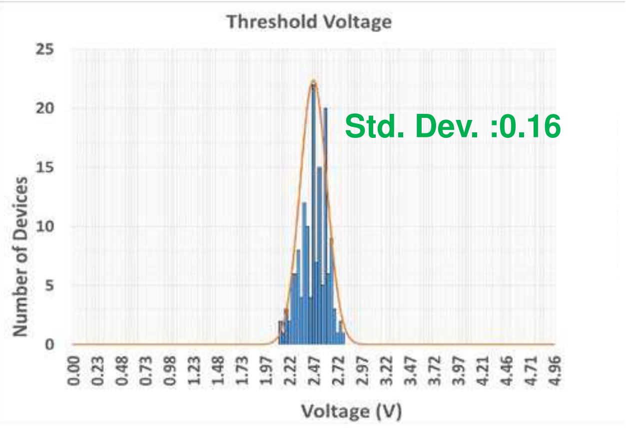



Average = 2.03 V

### Lot-4-W2-#5




Average = 2.48 V

**Typical value is the Average of All Devices from All Three Lots**

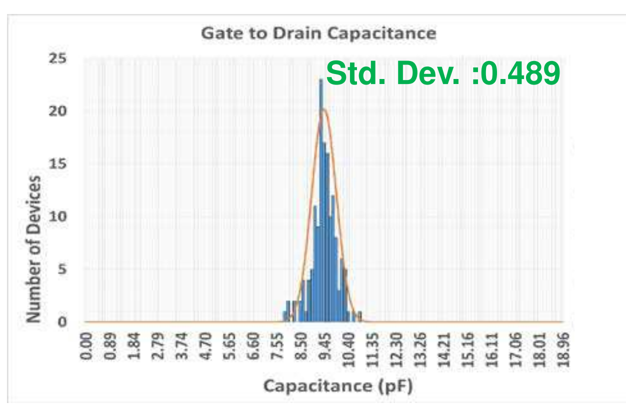
Typical : 2.33 V (Allowable Max : 3.50 V (50 % more)) ➔ All devices meet specifications

# Accumulation Channel MOSFET (ACCUFET) (Within Lot Variation)

## Cgd [pF] @ Vd=1000 V, RT

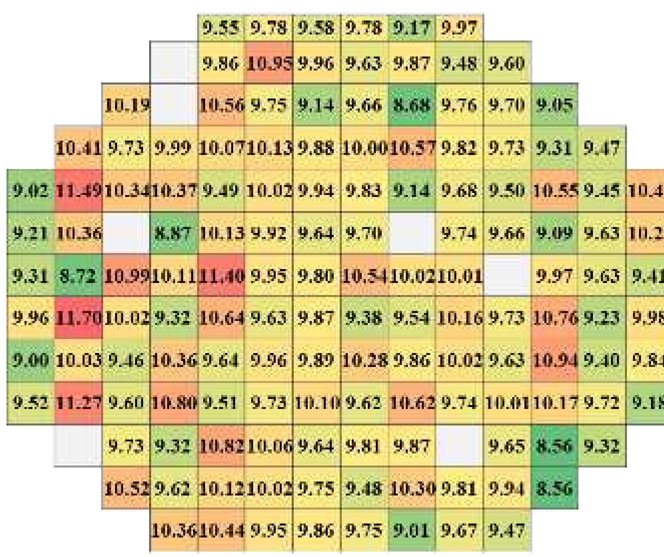
### Lot-5-W1-#5

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 9.36 | 9.68 | 10.02 | 9.38 | 9.77 | | | | | |
| | | | 10.51 | 9.40 | 9.93 | 9.53 | 9.49 | 8.05 | 9.15 | 8.98 | | | |
| | | 9.16 | 9.89 | 9.63 | 9.71 | 9.10 | 9.60 | 9.39 | 9.13 | 9.40 | 9.42 | | |
| | 9.54 | 9.81 | 9.41 | 9.39 | 9.82 | 9.16 | 10.02 | 9.60 | 9.53 | 9.55 | 8.84 | 9.56 | |
| 10.20 | 10.30 | 10.00 | 9.82 | 9.53 | 9.66 | 9.03 | 9.49 | 10.21 | 9.64 | 9.33 | 8.64 | | 8.14 |
| 9.39 | 9.52 | | 10.33 | 9.59 | 9.27 | 9.77 | 9.80 | 9.03 | 10.12 | 9.49 | 10.17 | 9.32 | 9.41 |
| 10.90 | 8.68 | 10.24 | 8.96 | 10.32 | 9.37 | 9.16 | 9.81 | 9.46 | 9.30 | | 9.63 | 9.15 | 8.32 |
| 10.75 | 9.84 | 9.46 | 9.71 | 9.47 | | 9.41 | 9.53 | 9.43 | 9.85 | 9.72 | 8.34 | 9.27 | 8.73 |
| 9.83 | 9.61 | 10.17 | 9.43 | 9.36 | 9.75 | 9.93 | 9.63 | 8.96 | 9.23 | 9.28 | 9.48 | 9.12 | 8.02 |
| 10.05 | 9.90 | 9.56 | 10.35 | 10.13 | 9.86 | 9.00 | 9.41 | 9.92 | 9.24 | 9.37 | 10.25 | 9.16 | 9.62 |
| | 9.72 | 9.38 | 9.96 | 9.73 | 9.67 | 9.40 | 9.61 | 8.59 | 9.25 | 9.38 | 8.55 | 8.95 | |
| | | 9.94 | 9.66 | 9.66 | 9.79 | 9.16 | 10.02 | 9.02 | 9.61 | 9.17 | 9.42 | | |
| | | | 9.41 | 9.97 | | 10.37 | 9.51 | 9.43 | 8.73 | 8.98 | | | |

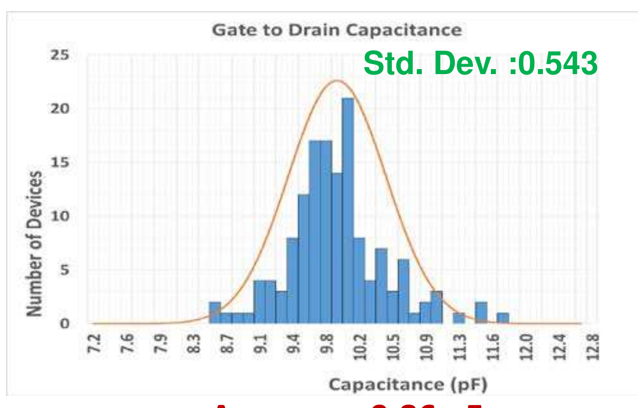



Average = 9.51 pF

### Lot-5-W2-#5



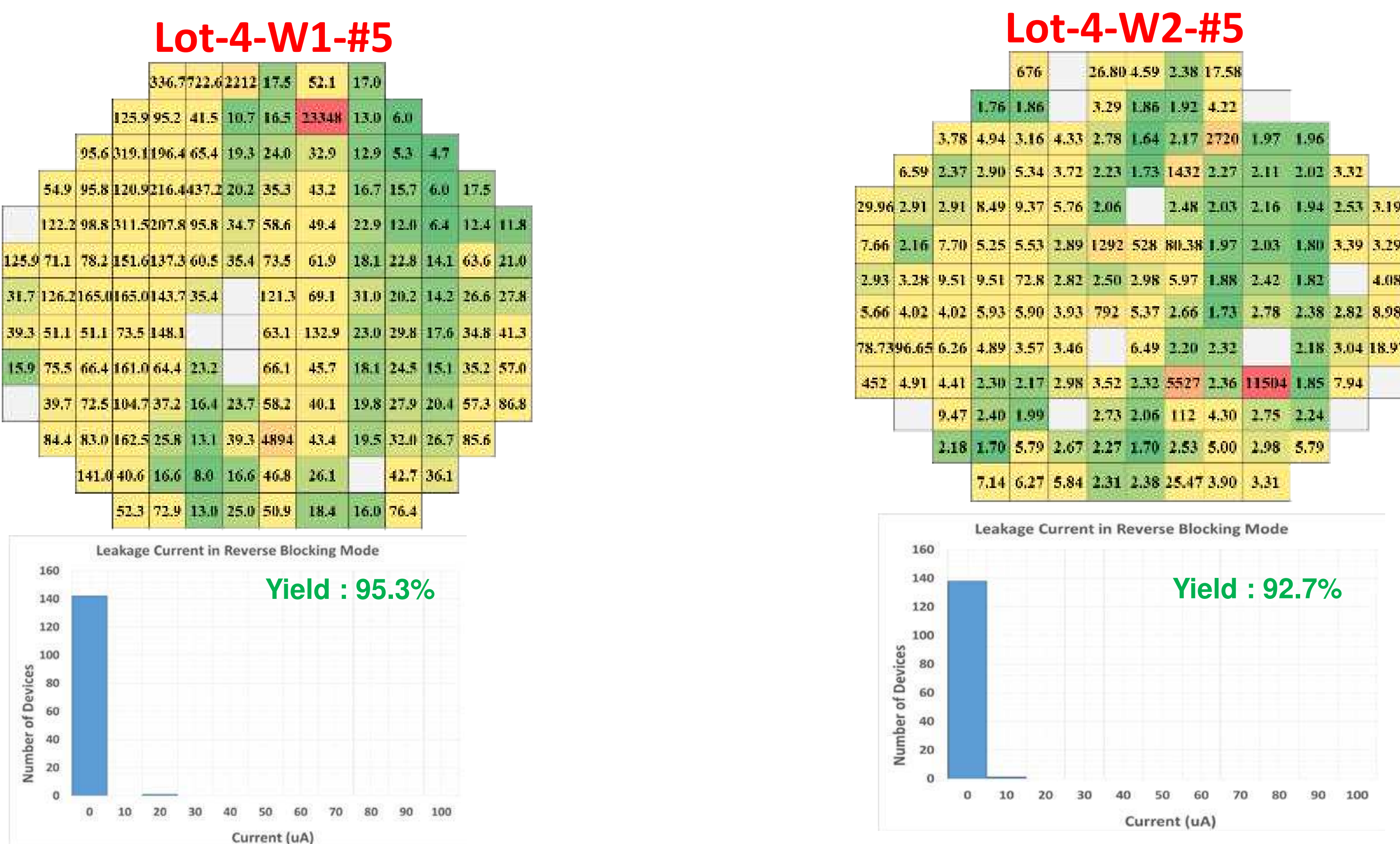
| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 9.55 | 9.78 | 9.58 | 9.78 | 9.17 | 9.97 | | | | |
| | | | | 9.86 | 10.95 | 9.96 | 9.63 | 9.87 | 9.48 | 9.60 | | | |
| | | 10.19 | | 10.56 | 9.75 | 9.14 | 9.66 | 8.68 | 9.76 | 9.70 | 9.05 | | |
| | 10.41 | 9.73 | 9.99 | 10.07 | 10.13 | 9.88 | 10.00 | 10.57 | 9.82 | 9.73 | 9.31 | 9.47 | |
| 9.02 | 11.49 | 10.34 | 10.37 | 9.49 | 10.02 | 9.94 | 9.83 | 9.14 | 9.68 | 9.50 | 10.55 | 9.45 | 10.47 |
| 9.21 | 10.36 | | 8.87 | 10.13 | 9.92 | 9.64 | 9.70 | | 9.74 | 9.66 | 9.09 | 9.63 | 10.23 |
| 9.31 | 8.72 | 10.99 | 10.11 | 11.40 | 9.95 | 9.80 | 10.54 | 10.02 | 10.01 | | 9.97 | 9.63 | 9.41 |
| 9.96 | 11.70 | 10.02 | 9.32 | 10.64 | 9.63 | 9.87 | 9.38 | 9.54 | 10.16 | 9.73 | 10.76 | 9.23 | 9.98 |
| 9.00 | 10.03 | 9.46 | 10.36 | 9.64 | 9.96 | 9.89 | 10.28 | 9.86 | 10.02 | 9.63 | 10.94 | 9.40 | 9.84 |
| 9.52 | 11.27 | 9.60 | 10.80 | 9.51 | 9.73 | 10.10 | 9.62 | 10.62 | 9.74 | 10.01 | 10.17 | 9.72 | 9.18 |
| | | 9.73 | 9.32 | 10.82 | 10.06 | 9.64 | 9.81 | 9.87 | | 9.65 | 8.56 | 9.32 | |
| | | 10.52 | 9.62 | 10.12 | 10.02 | 9.75 | 9.48 | 10.30 | 9.81 | 9.94 | 8.56 | | |
| | | | 10.36 | 10.44 | 9.95 | 9.86 | 9.75 | 9.01 | 9.67 | 9.47 | | | |




Average = 9.86 pF

# Accumulation Channel MOSFET (ACCUFET) (Within Lot Variation)

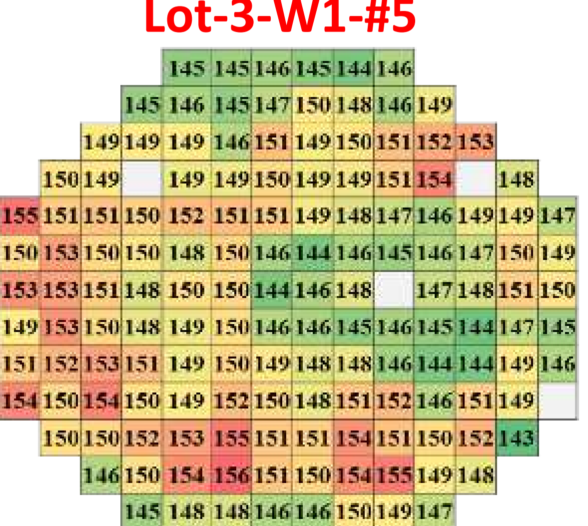
## Leakage Current ($I_L$) [nA] @ Vd=1000 V, RT

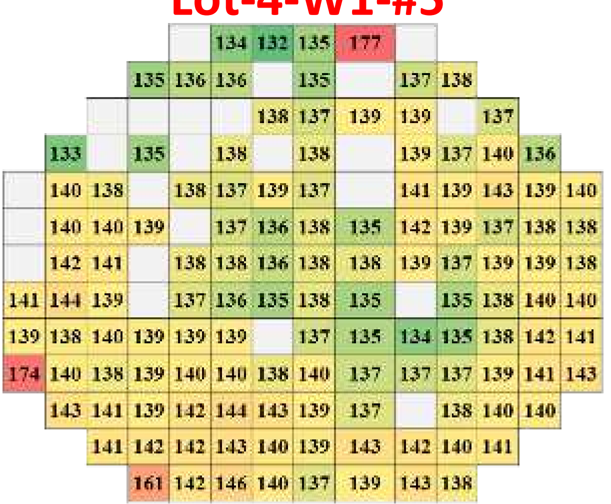


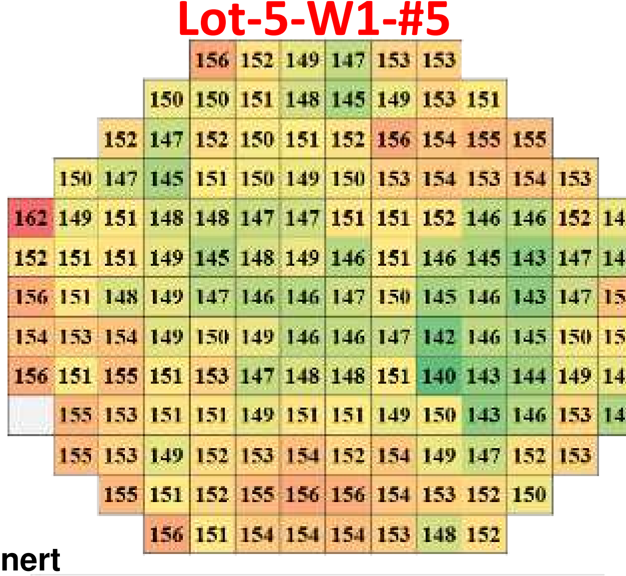

**<u>Yield based on allowable maximum leakage current of 100 μA</u>**

# Accumulation Channel MOSFET (ACCUFET) (Lot-to-Lot Variation)

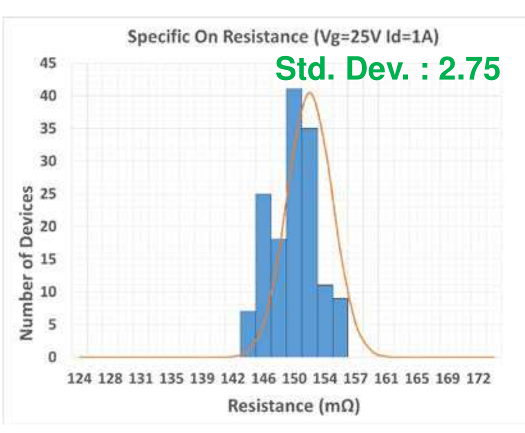
## On-Resistance ($R_{on}$) [mΩ] @ Id=1A, Vg=25V, RT




☐ Damaged during the BV test w/o Flourinert

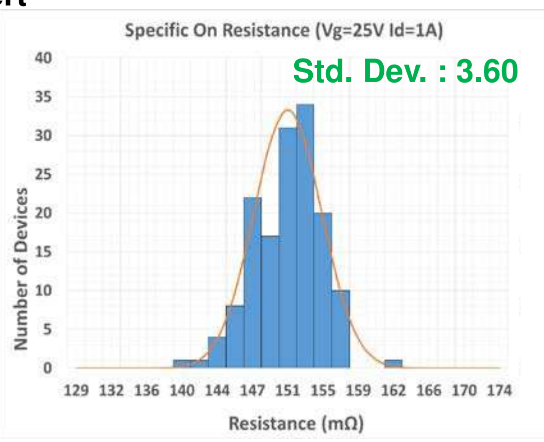



Specific On Resistance (Vg=25V Id=1A)

Std. Dev. : 5.57

Number of Devices

Resistance (mΩ)




Average = 149 mΩ

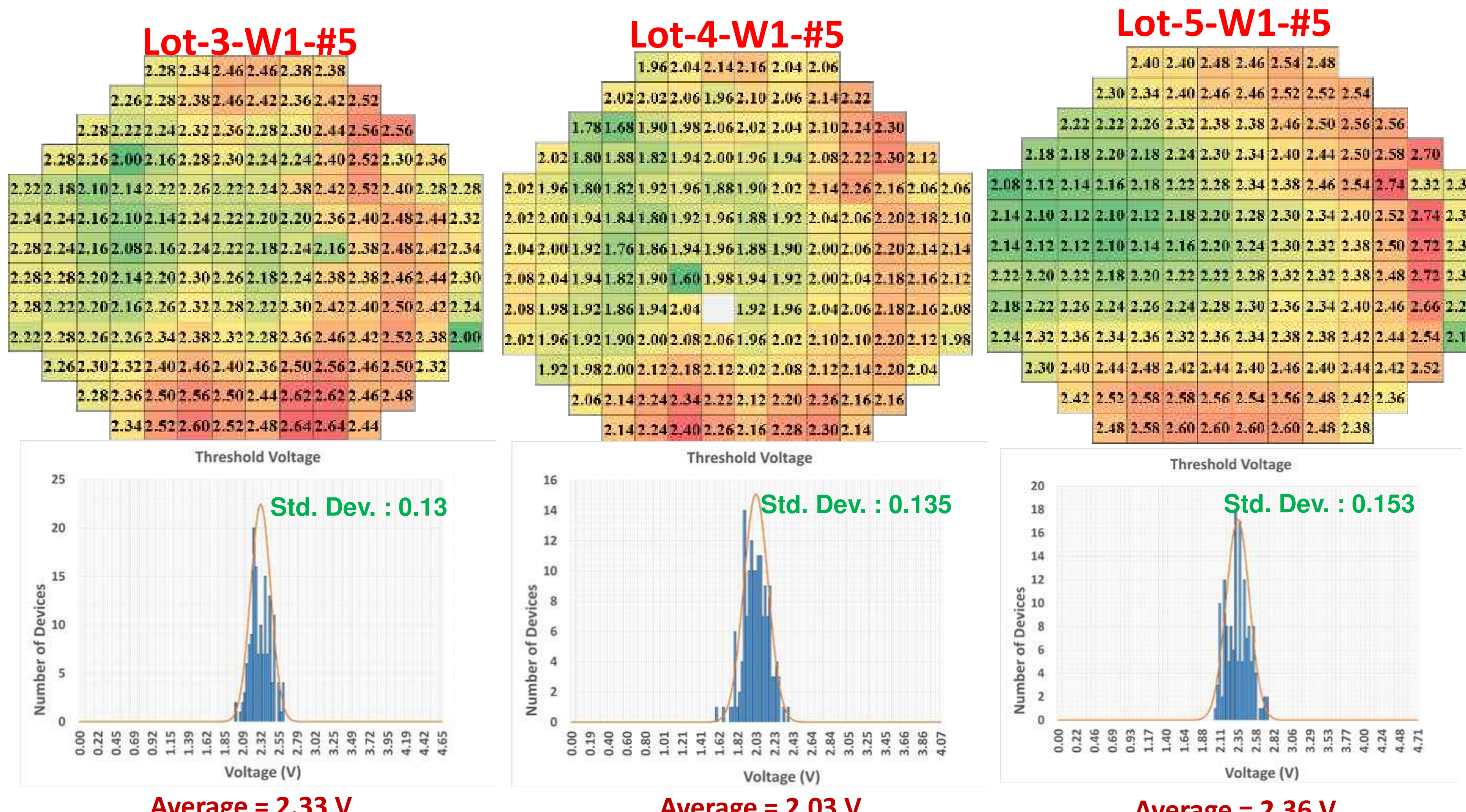
Average = 139 mΩ

Average = 150 mΩ

Typical : 144 mΩ (Allowable Max : 187 mΩ (30 % more)) ➔ All devices meet specifications

# Accumulation Channel MOSFET (ACCUFET) (Lot-to-Lot Variation)

## Threshold Voltage ($V_{th}$) [V] @ Id = 1 mA, Vd = 0.1 V, RT

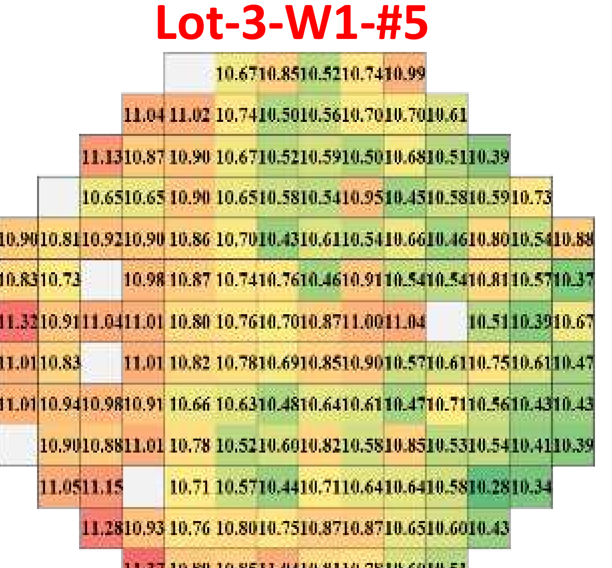



Typical : 2.33 V (Allowable Max : 3.50 V (50 % more)) ➔ All devices meet specifications

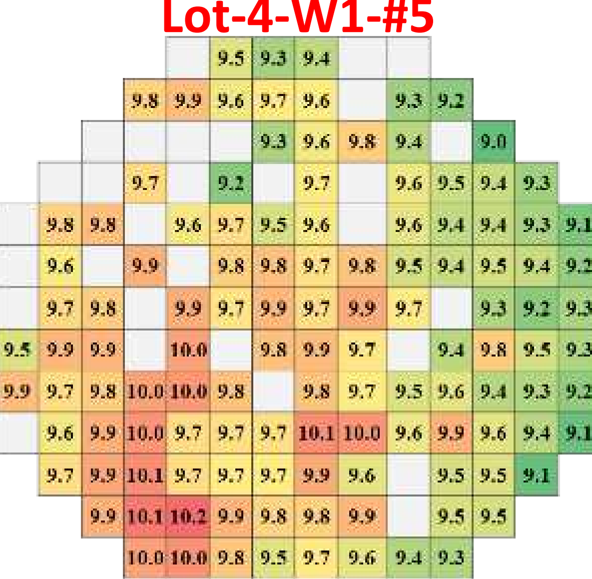
# Accumulation Channel MOSFET (ACCUFET) (Lot-to-Lot Variation)

## Cgd [pF] @ Vd=1000 V, RT

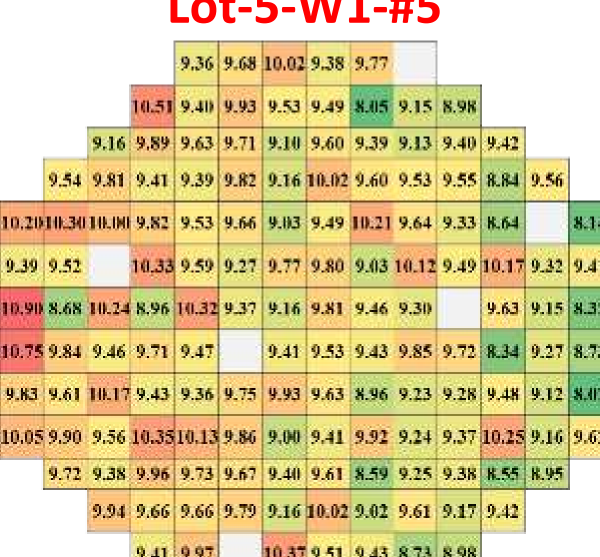
**Lot-3-W1-#5**



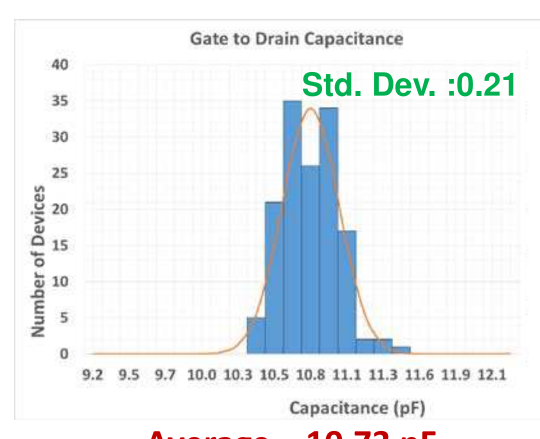
**Lot-4-W1-#5**



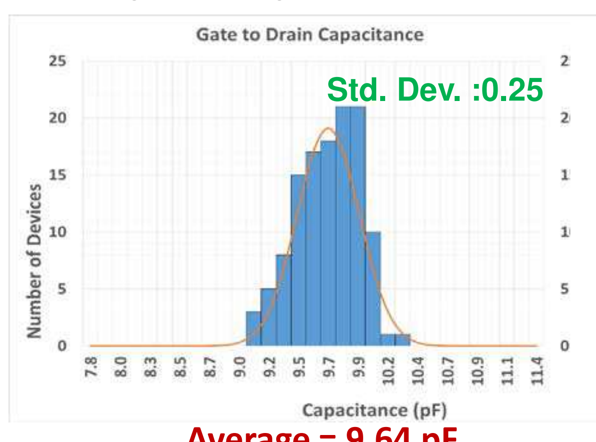
**Lot-5-W1-#5**



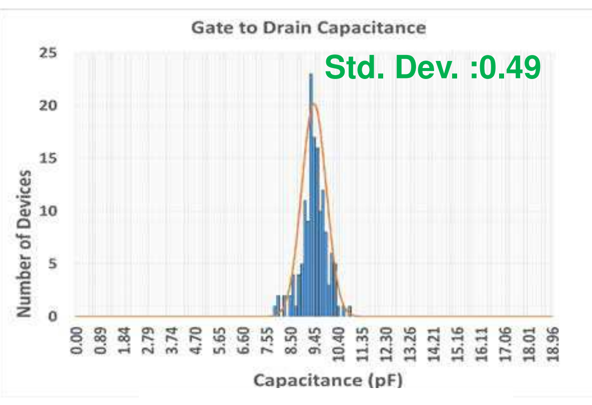
☐ Damaged during the BV test w/o Flourinert




Average = 10.73 pF



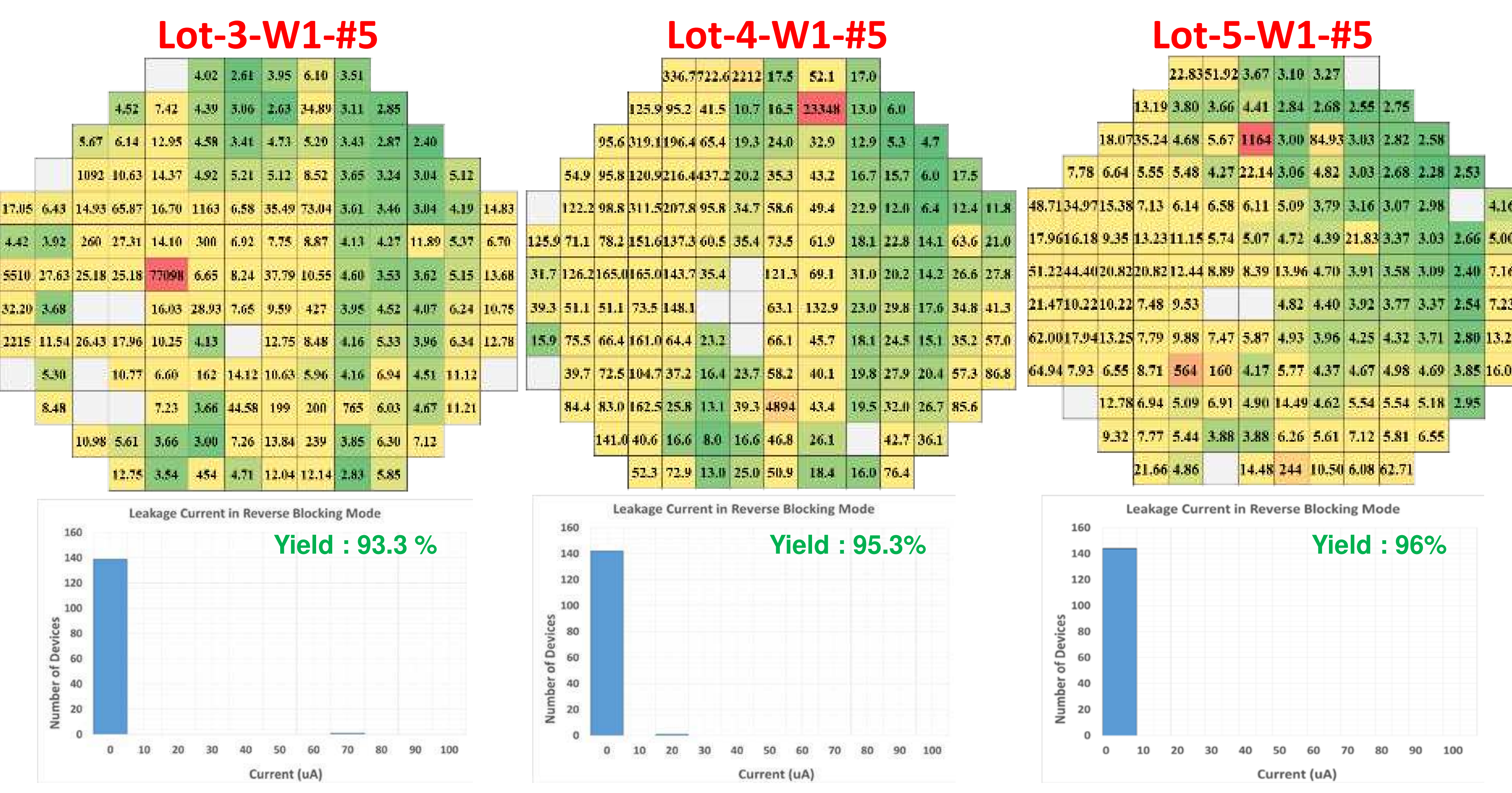

Average = 9.64 pF




Average = 9.51 pF

# Accumulation Channel MOSFET (ACCUFET) (Lot-to-Lot Variation)

## Leakage Current ($I_L$) [nA] @ Vd=1000 V, RT




**Yield based on allowable maximum leakage current of 100 μA**

# Inversion Channel MOSFET (INVFET)

- Process Qualification using Three Process at X-Fab
- Device #5: Inversion Channel MOSFET (INVFET) with JFET Implant
  - Active Area = 0.045 cm2
- Similar Results like Accumulation Channel devices

**PRESiCE Technology is available for licensing from NCSU for manufacturing products at X-Fab**

# Outline

- SiC Power MOSFET Breakthroughs achieved at NCSU
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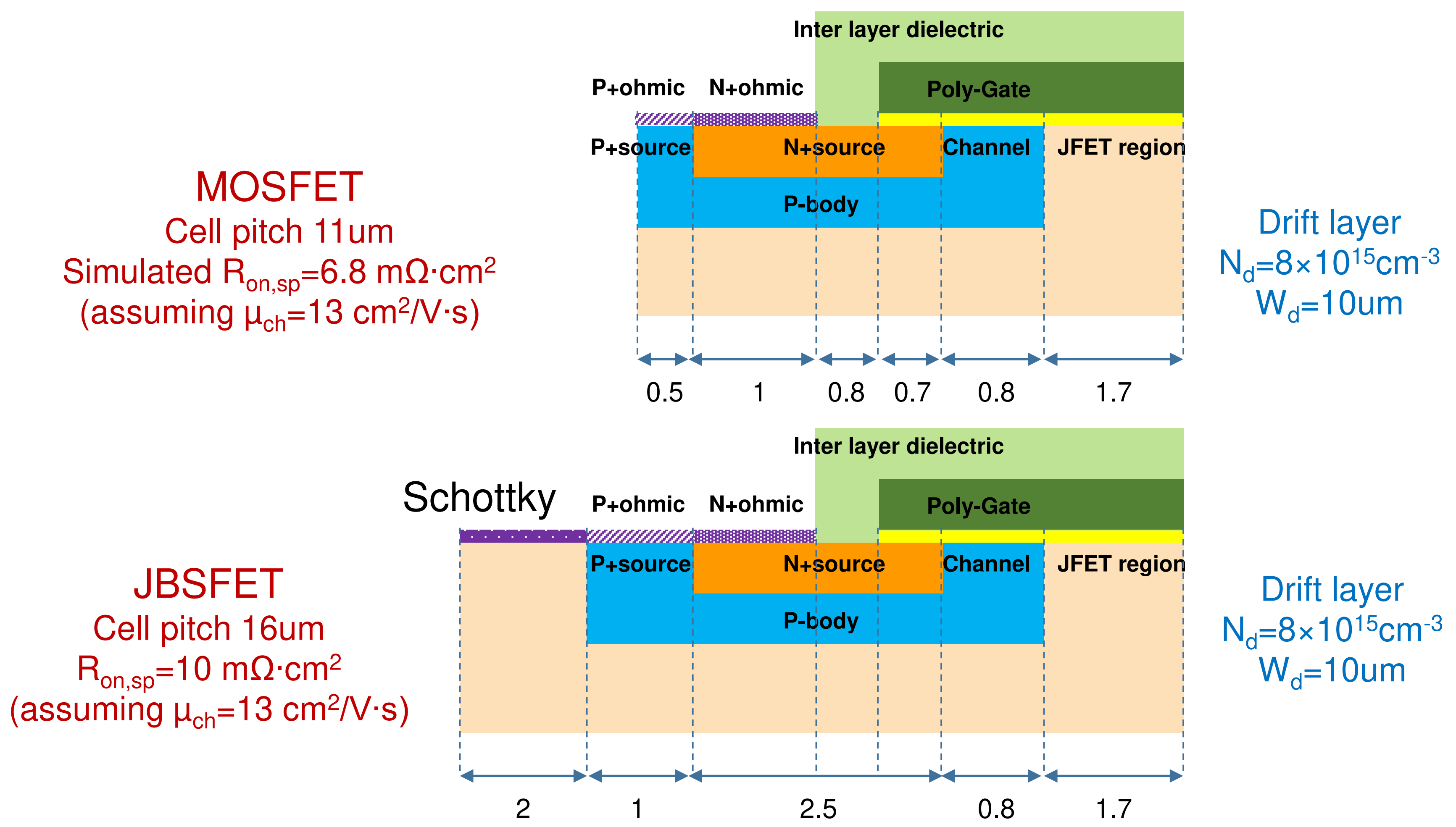
  - The OCTFET: A New Cell Topology with Superior High Frequency Figures-of-Merit
  - The BiDFET: A Monolithic Bi-Directional Field Effect Transistor

# JBSFET: MOSFET with Integrated JBS Diode




**W. Sung and B.J. Baliga, "On Developing One-Chip Integration of 1.2 kV SiC MOSFET and JBS Diode (JBSFET)", *IEEE Transactions on Industrial Electronics*, Vol. 64, pp. 8206-8212, 2017.**

# JBSFET Area Savings Analysis

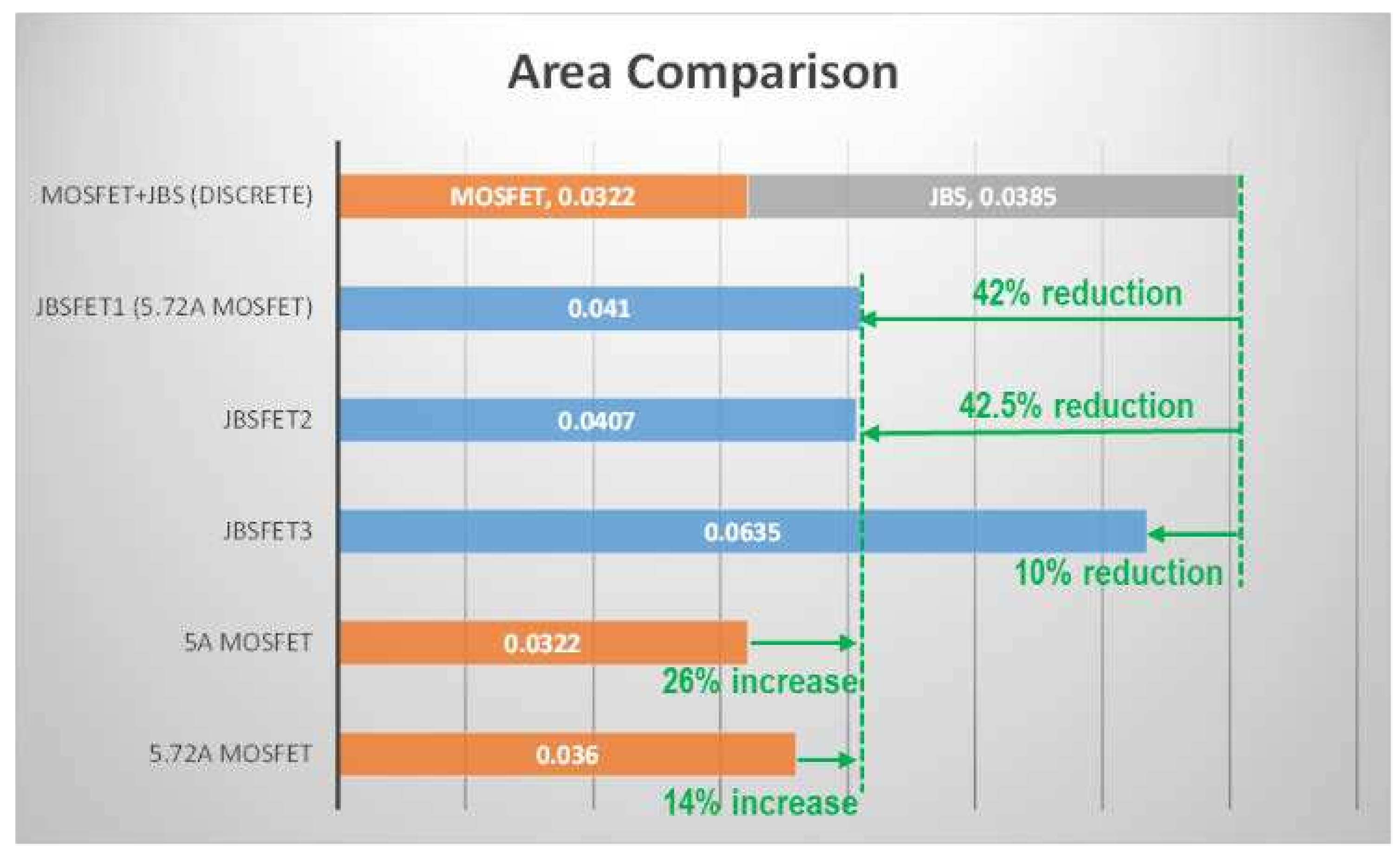
- Layout comparison for 1.2 kV, 5.7 A Devices

| | Approaches | Active area (cm2) | Edge termination And periphery | Total area (cm2) |
|---|---|---|---|---|
| Previous approach | Pure MOS FET + Pure JBS | 0.0212 (MOSFET)<br>0.0263 (JBS) | 0.0110 (MOSFET)<br>0.0122 (JBS) | 0.0322+<br>0.0385 =<br>***0.0707*** |
| PA approach 1<br>JBSEFET1 | JBSFET | 0.0284<br>(5.72A MOSFET*) | 0.0126 | ***0.041*** |
| PA approach 2<br>JBSFET2 | JBSFET | 0.0281 | 0.0126 | ***0.0407*** |
| PA approach 3<br>JBSFET3 | Pure MOS FET<br>Pure JBS | 0.0475 | 0.016 | ***0.0635*** |

Assumptions:

- Edge termination design : 10 floating field rings – 3um wide, total spacing is about 20um, which gives about 50um total width for edge termination
- Periphery : Edge termination to C/S implant – 20um, dicing lane 70um per side, C/S to dicing 30um-> total 120um
- *Comparison with a 5.72A pure MOSFET : 0.0242 active + 0.0117 periphery = 0.036 cm2

# JBSFET Area Savings Analysis

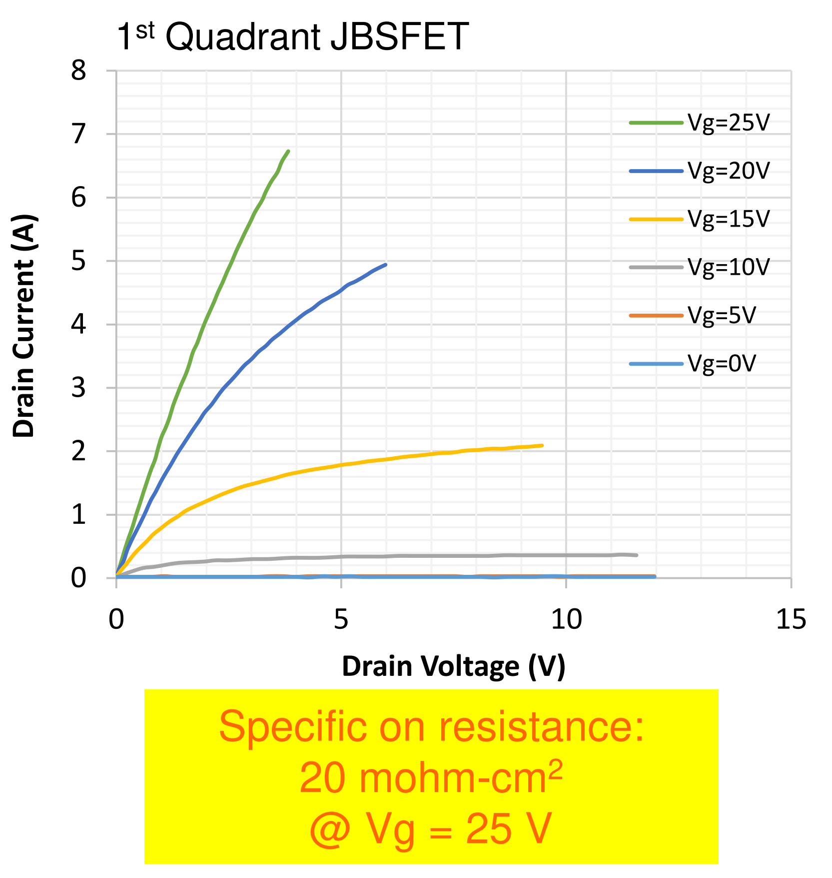


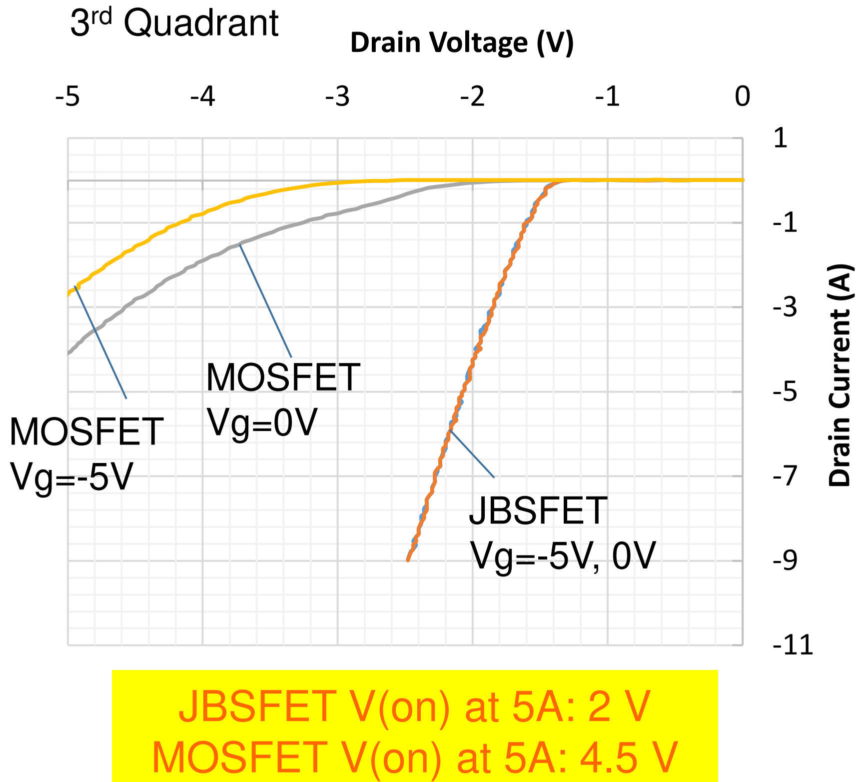

**Conclusion: Area Savings of about 40 % can be achieved with the JBSFET Approach**

**Other Benefits: Cuts package count in half.**
**Reduces switching loss by 40% at elevated temperatures.**

# Measured Data - JBSFET I-V

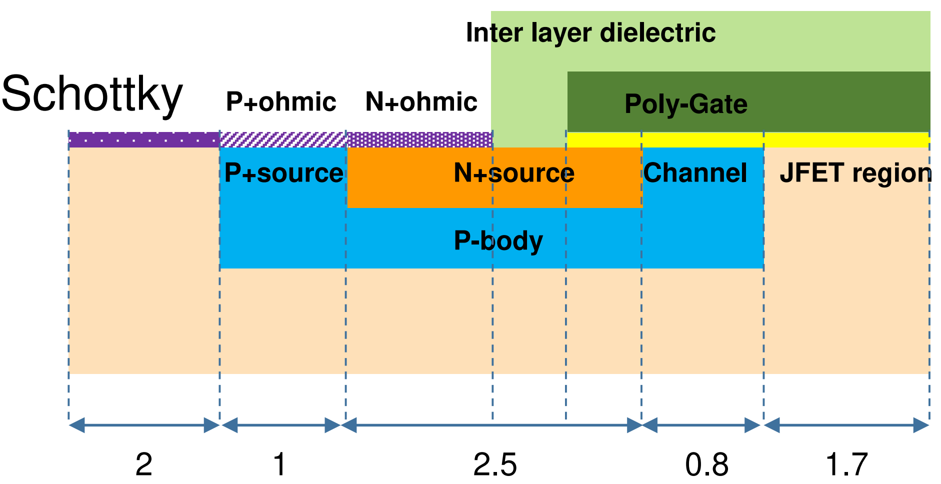
## JBSFET Id-Vd, Active area 4.5mm$^2$



# Accumulation Channel JBSFET

- Process Qualification using Three Process Lots at X-Fab
- Device #7: Accumulation Channel JBSFET with JFET Implant
  - Active Area = 0.045 cm2



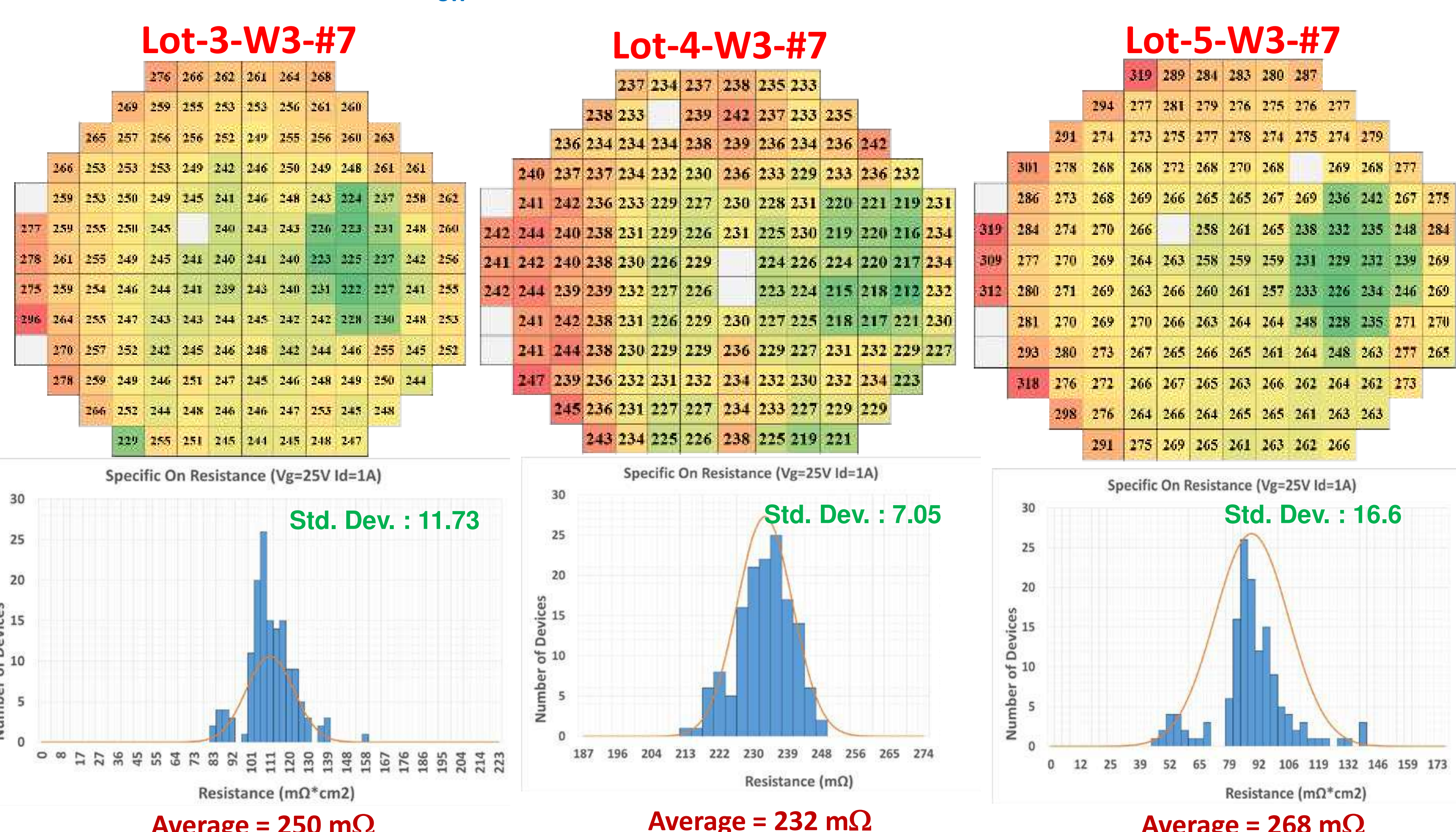

W. Sung and B.J. Baliga, "Monolithically Integrated 4H-SiC MOSFET and JBS Diode (JBSFET) using a Single Ohmic/Schottky Process Scheme", *IEEE Electron Device Letters*, Vol. 37, pp. 1605-1608, 2016.

**Technical Note**:

- The Rds,on values in the Wafer Maps and Statistical Data plots include 35 mΩ of parasitic probe (~ 1 mΩ-cm2) and substrate (~ 1 mΩ-cm2) resistance.
- The Cgd values in Wafer Maps and Statistical data include 0.5 pF of parasitic probe capacitance.

# Accumulation Channel JBSFET (Lot-to-Lot Variation)

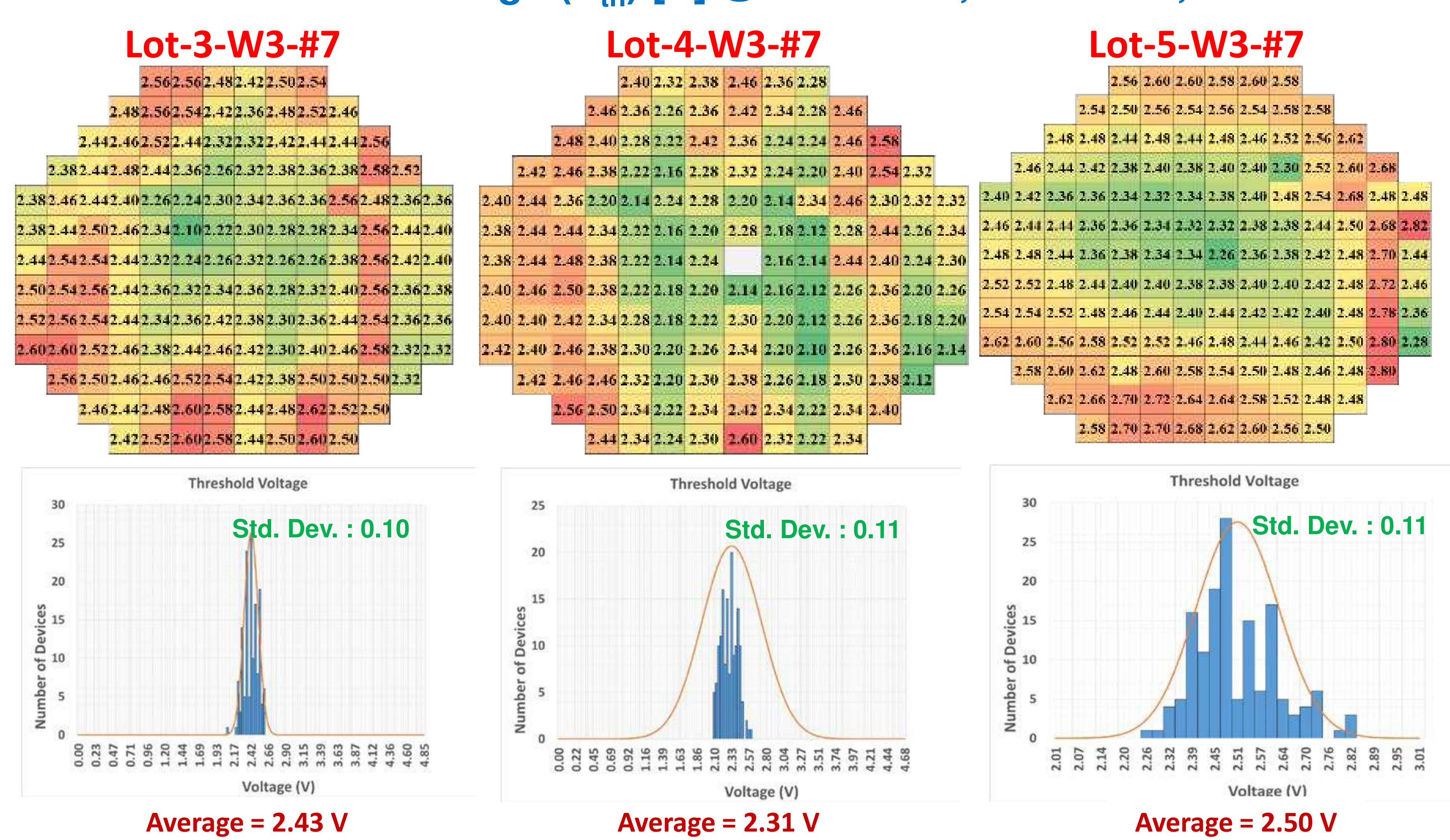
## On-Resistance ($R_{on}$) [mΩ] @ Id=1A, Vg=25V, RT – 11 mΩ-cm2




**Typical : 250 mΩ (Allowable Max : 325 mΩ (30 % more)) ➔ All devices meet specifications**

# Accumulation Channel JBSFET (Lot-to-Lot Variation)

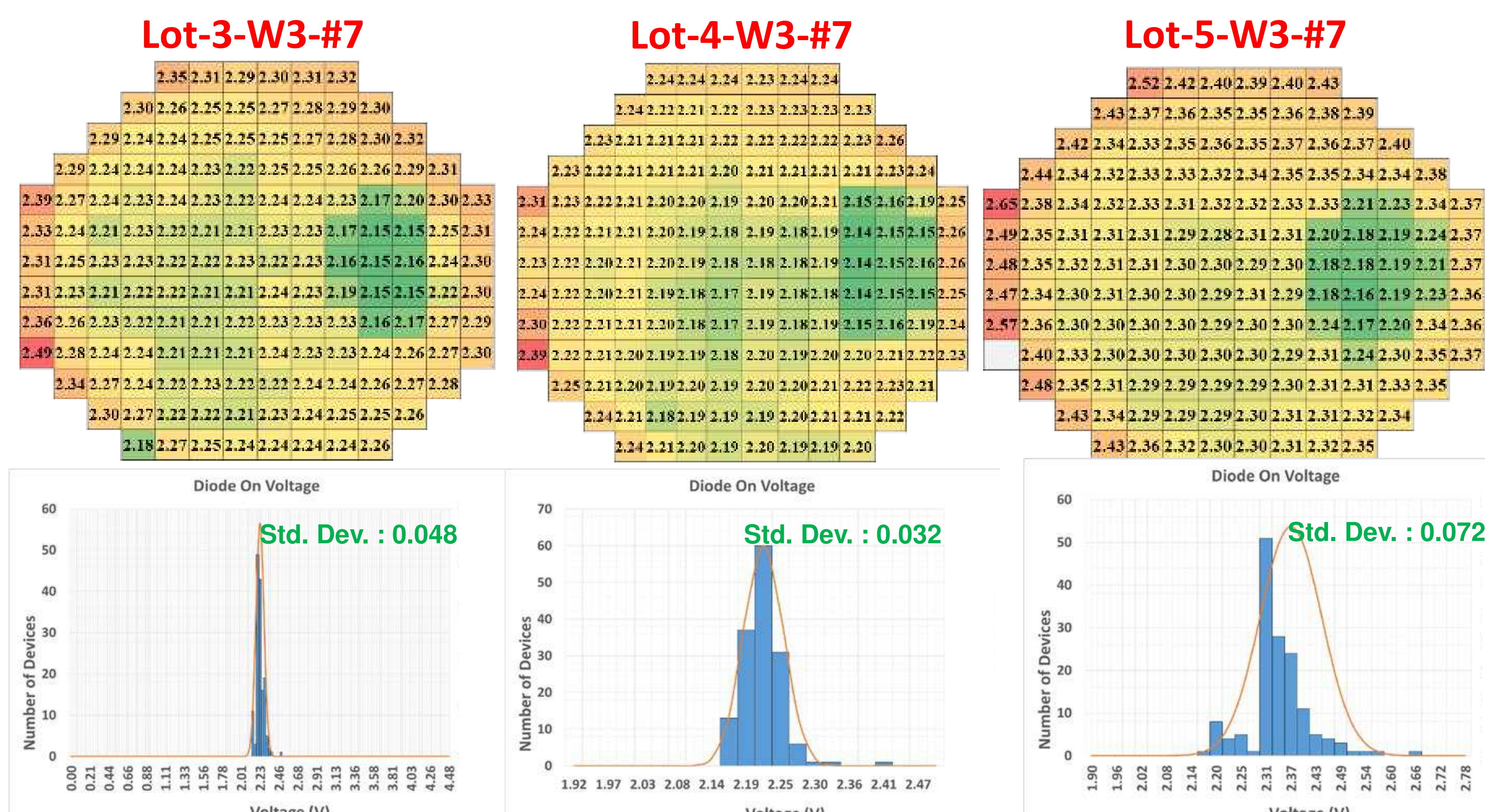
## Threshold Voltage ($V_{th}$) [V] @ Id = 1 mA, Vd = 0.1 V, RT




**Typical : 2.41 V (Allowable Max : 3.62 V (50 % more)) ➔ All devices meet specifications**

# Accumulation Channel JBSFET (Lot-to-Lot Variation)

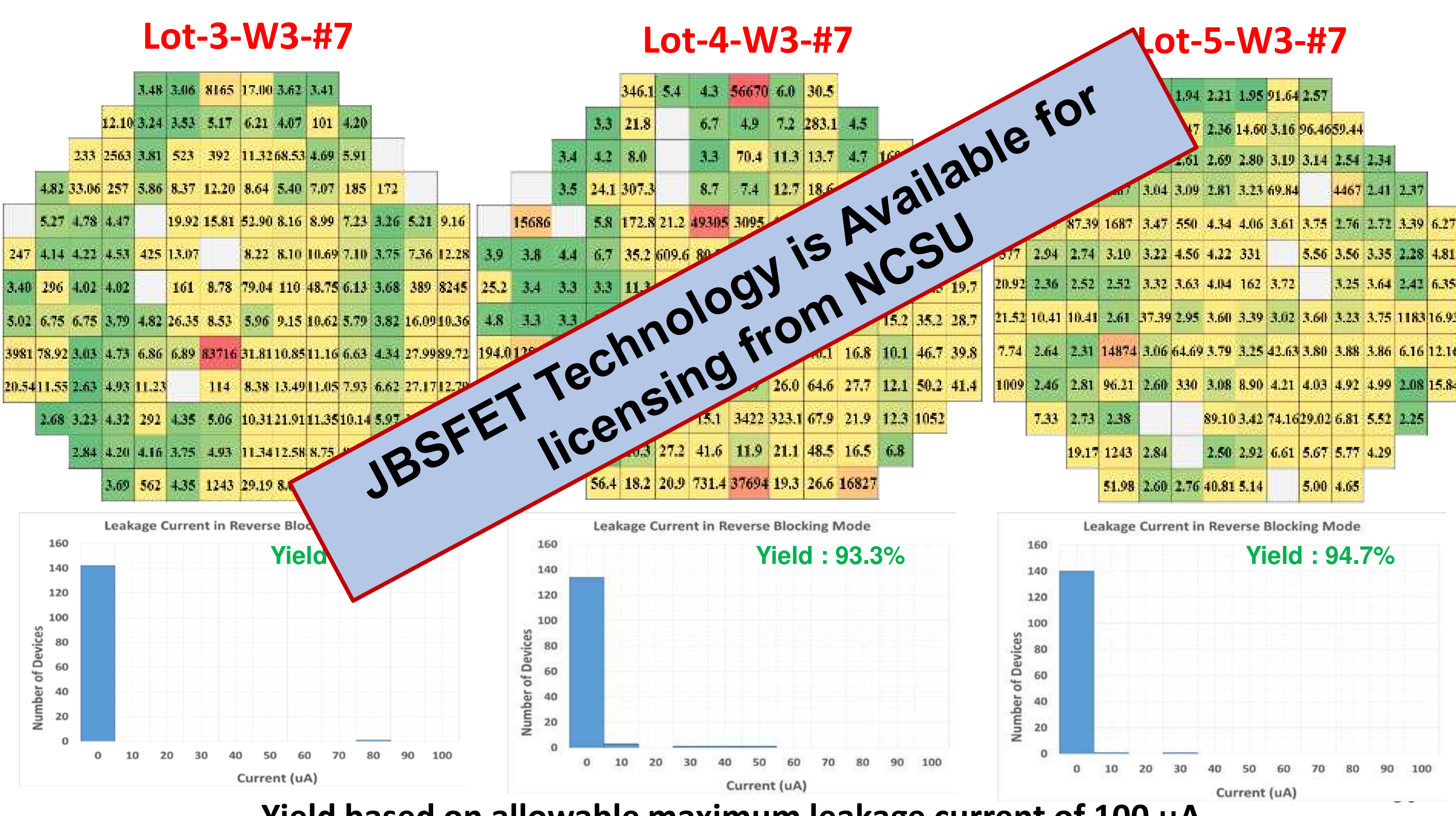
## 3rd Quadrant ($V_f$) [V]@ If = 5A, RT




Average = 2.25 V | Average = 2.21 V | Average = 2.33 V

# Accumulation Channel JBSFET (Lot-to-Lot Variation)

## Leakage Current ($I_L$) [nA] @ Vd=1000 V, RT




**Yield based on allowable maximum leakage current of 100 μA**

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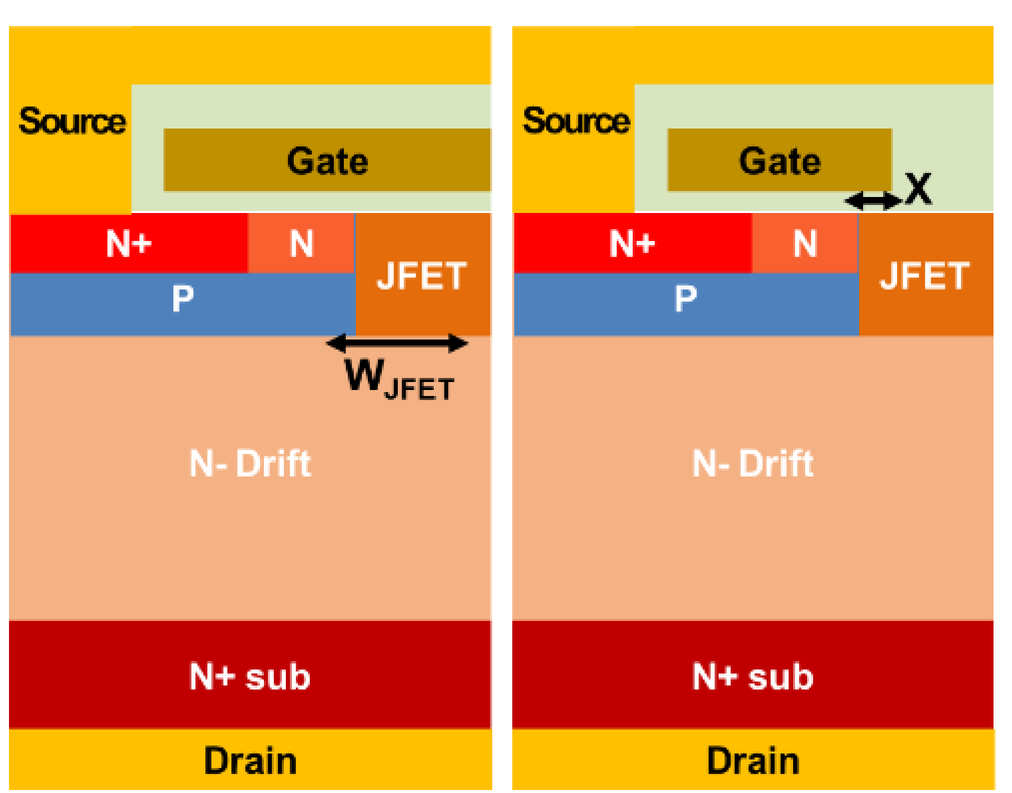
  - The BiDFET: A Monolithic Bi-Directional Field Effect Transistor

# Split-Gate (SG) SiC Power MOSFET




Conventional

Split-Gate

| | MOSFET | SG-MOSFET |
|---|---|---|
| X width | NA | 0.3 μm |
| JFET region width ($W_{JFET}$) | 0.7 μm | 0.9 μm |
| JFET region doping | $3\times10^{16}$ cm$^{-3}$ | |
| N- Drift thickness | 10 μm | |
| N- Drift doping | $8\times10^{15}$ cm$^{-3}$ | |

- The Split-Gate SiC Power MOSFET can be fabricated with the same process as used for the Conventional MOSFET.
- Gate Design is different during device layout.

# Split-Gate (SG) SiC Power MOSFET

Conventional MOSFET

$R_{on,sp}$

Oxide Field

$Q_{gd,sp}$

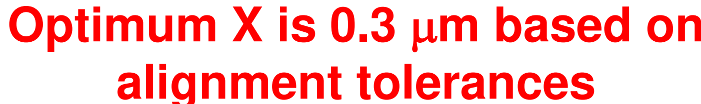
$C_{gd,sp}$

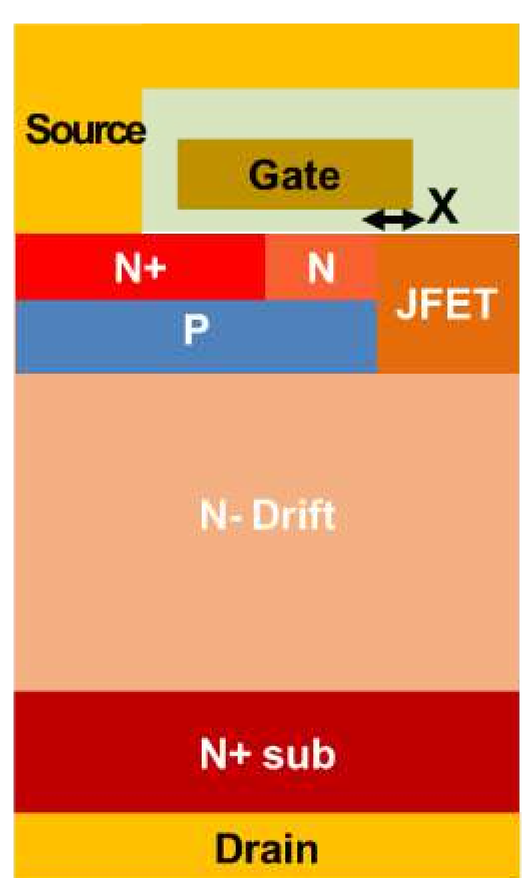
FOM

Qgd,sp (nC/cm2)
Cgd,sp (pF/cm2)
FOM (x0.1 mOhm-nC)

Oxide Field (MV/cm)
Ron,sp (mOhm-cm2)

X width (um)



# Split-Gate (SG) SiC Power MOSFET: Experimental Results

Drain Current (A)
Vg=0~25V, 5V step
SGMOS
MOSFET
Drain Voltage (V)

Drain Current (A)
SGMOS
MOSFET
Drain Voltage (V)

Capacitance (F)
SGMOS
MOSFET
Cgd
Drain Voltage (V)

Gate Voltage (V)
SGMOS
MOSFET
$Q_{gd}$ (for SG-MOS)
$Q_{gd}$ (for MOSFET)
Gate Charge (nC)

# Split-Gate (SG) SiC Power MOSFET: Experimental Results

TABLE I
SUMMARY OF EXPERIMENTAL RESULTS
FOR CONVENTIONAL MOSFET AND SG-MOSFET

| | MOSFET | SG-MOSFET |
|---|---|---|
| Breakdown voltage [V] | 1634 | [illegible] |
| Threshold voltage [V] | 2.00 | [illegible] |
| $R_{on,sp}$ [mΩ-cm2] | 6.35 | [illegible] |
| $C_{gd,sp}$ [pF/cm$^2$] (@$V_d$=0V) | [illegible] | [illegible] |
| $C_{gd,sp}$ [pF/cm$^2$] (@$V_d$=1kV) | [illegible] | 82 |
| $Q_{gd,sp}$ [nC/cm$^2$] | [illegible] | 149 |
| FOM <R×C (@$V_d$=[illegible] | [illegible] | 16520 |
| FOM <R×C [illegible] | 766 | 589 |
| [illegible] | 2230 | 938 |

1.3x Improvement

2.4x Improvement

Technology is Available for licensing from NCSU

K. Han, B.J. Baliga, and W. Sung, "Split-Gate 1.2 kV 4H-SiC MOSFET: Analysis and Experimental Validation", *IEEE Electron Device Letters*, Vol. 38, pp. 1437-1440, October 2017.

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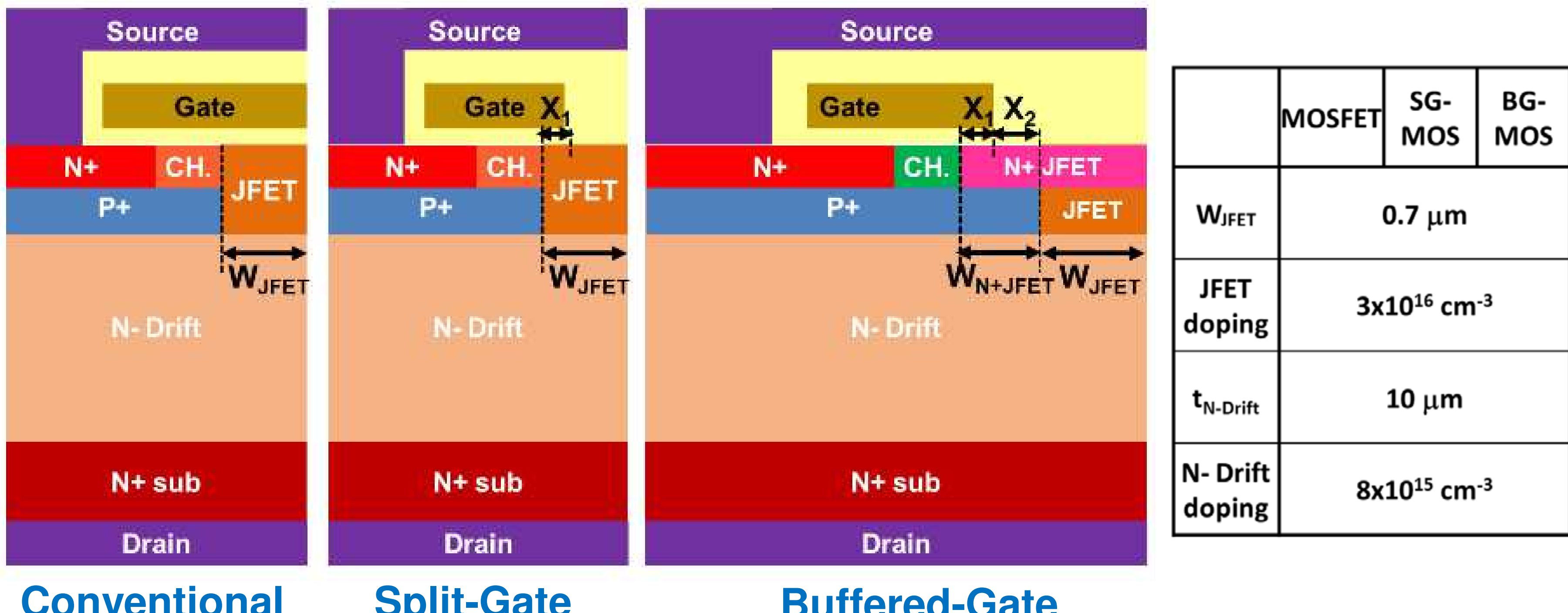
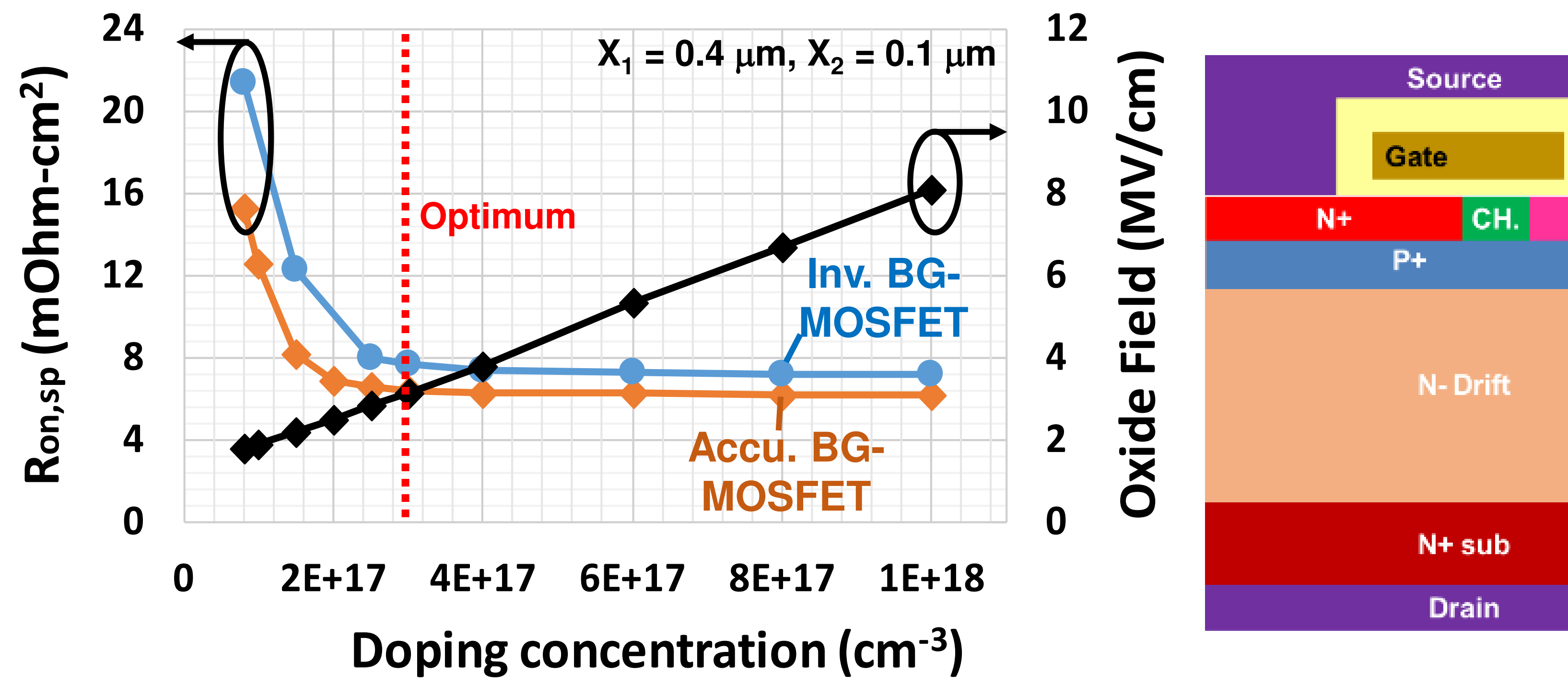
# Buffered-Gate (BG) SiC Power MOSFET




| | MOSFET | SG-MOS | BG-MOS |
|---|---|---|---|
| $W_{JFET}$ | 0.7 μm | | |
| JFET doping | $3\times10^{16}$ cm$^{-3}$ | | |
| $t_{N\text{-}Drift}$ | 10 μm | | |
| N- Drift doping | $8\times10^{15}$ cm$^{-3}$ | | |

- The Buffered-Gate SiC Power MOSFET can be fabricated with one additional (N+ JFET) Step compared with the Conventional MOSFET.
- Gate Design is different during device layout.

# Buffered-Gate (BG) SiC Power MOSFET




- <u>**Optimization of N+ JFET Doping Concentration**</u>

  **3E17 cm-3 is Optimum to:**

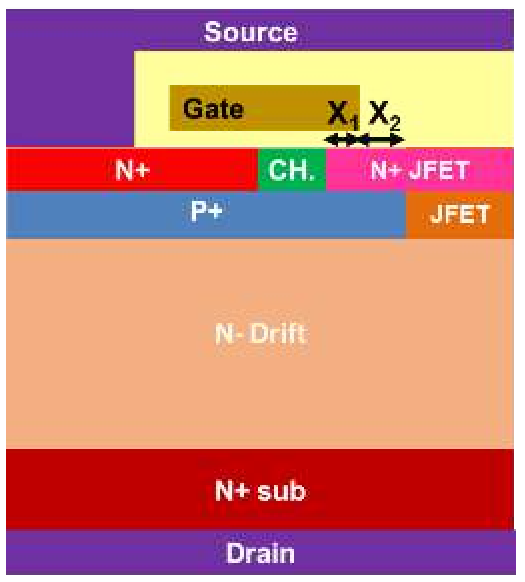
  - **Reduce Specific On-Resistance**
  - **Maintain Low Gate Oxide Electric Field**

# Buffered-Gate (BG) SiC Power MOSFET

X1 = 0. 4 μm

Qgd,sp (nC/cm²) / Cgd,sp (pF/cm²) and Ron,sp (mOhm-cm²) vs. X₂ width (μm): BG-MOSFET; $R_{on,sp}$; $Q_{gd,sp}$; $C_{gd,sp}$

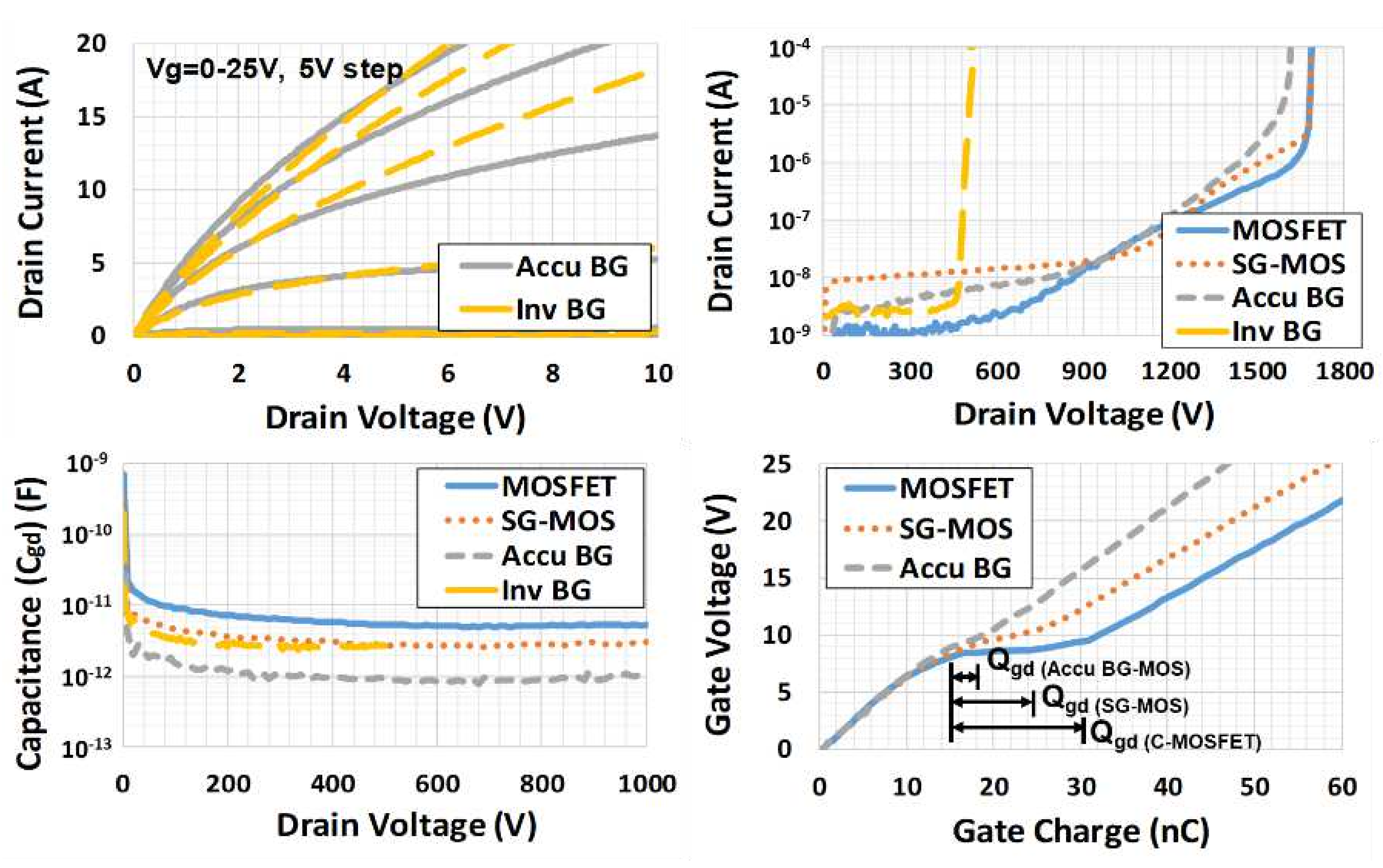
HF-FOM (RxQ) (mΩ-nC) / HF-FOM (RxC) (mΩ-pF) and Oxide Field (MV/cm) vs. X₂ width (μm): BG-MOSFET; Oxide Field; HF-FOM (RxQ); HF-FOM (RxC)




**X2 is P+ Shielding Region Extension beyond Gate Edge**

**Optimum X2 is 0.3 μm based on alignment tolerances**

# Buffered-Gate (BG) SiC Power MOSFET: Experimental Results



# Buffered-Gate (BG) SiC Power MOSFET: Experimental Results

TABLE I
SUMMARY OF EXPERIMENTAL RESULTS
FOR C-MOSFET, SG-MOSFET, AND BG-MOSFETS

| | C-MOSFET | SG-MOSFET | BG-MOSFET_L | BG-MO[illegible] |
|---|---|---|---|---|
| Cell pitch [μm] | 5.6 | 5.6 | 7.0 | [illegible] |
| BV [V] | 1689 | 1688 | [illegible] | [illegible] |
| $V_{th}$ [V] | 1.84 | 1.80 | [illegible] | [illegible] |
| $R_{on,sp}$ [mΩ-cm$^2$] | 5.78 | [illegible] | [illegible] | 8.39 |
| $C_{gd,sp}$ [pF/cm$^2$] | 121 | [illegible] | [illegible] | 23 |
| $Q_{gd,sp}$ [nC/cm$^2$] | [illegible] | [illegible] | 56 | 60 |
| FOM <$R_{on}$×$C_{gd}$> [mΩ-pF] | [illegible] | 406 | 229 | 194 |
| FOM [illegible] [mΩ[illegible] | [illegible] | 1287 | 596 | 503 |

Technology is Available for licensing from NCSU

3.6x Improvement

4.0x Improvement

K. Han, B.J. Baliga, and W. Sung, "A Novel 1.2 kV 4H-SiC Buffered-Gate (BG) MOSFET: Analysis and Experimental Validation", *IEEE Electron Device Letters*, Vol. 39, pp. 248-251, February 2018.

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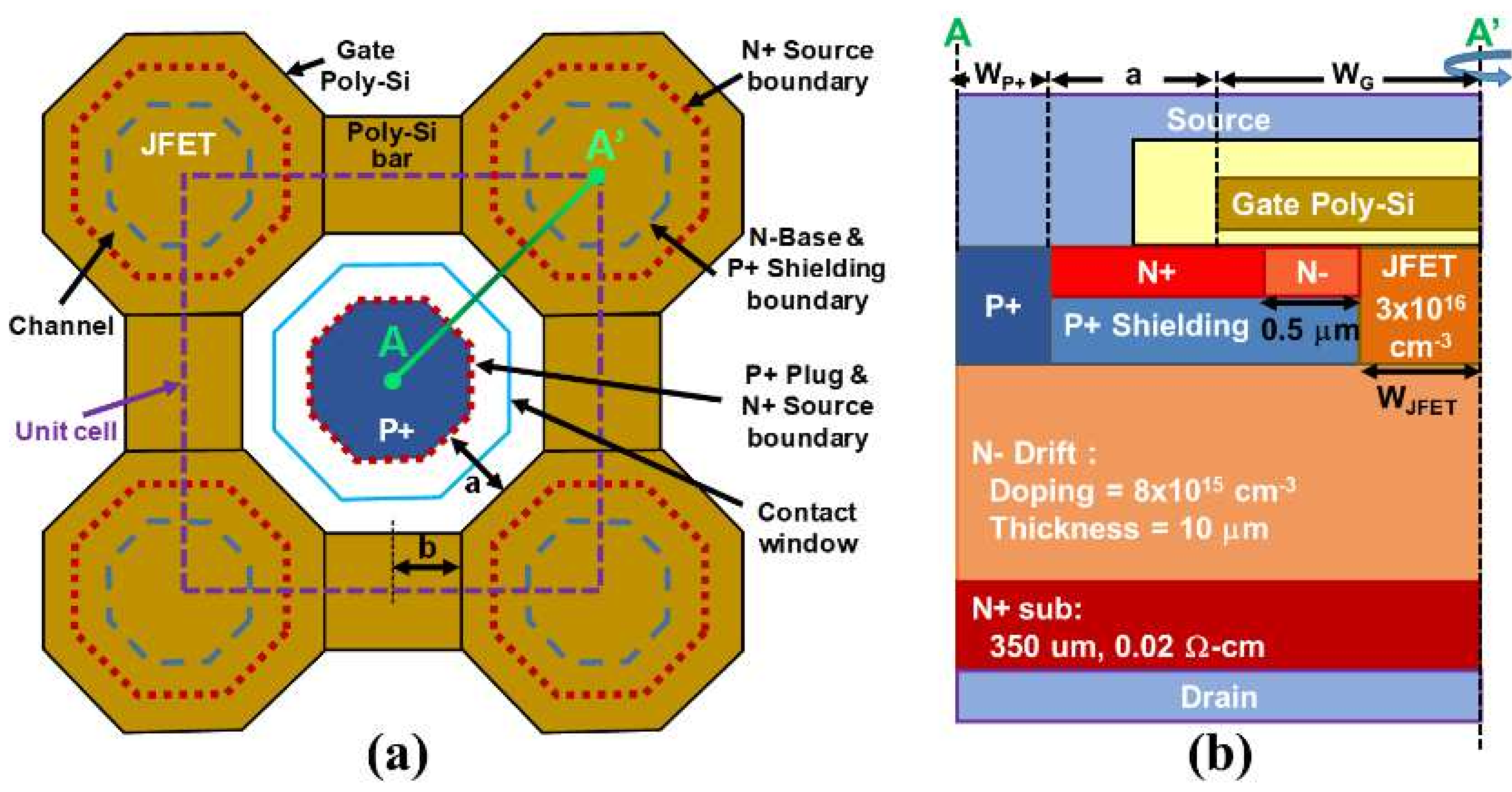
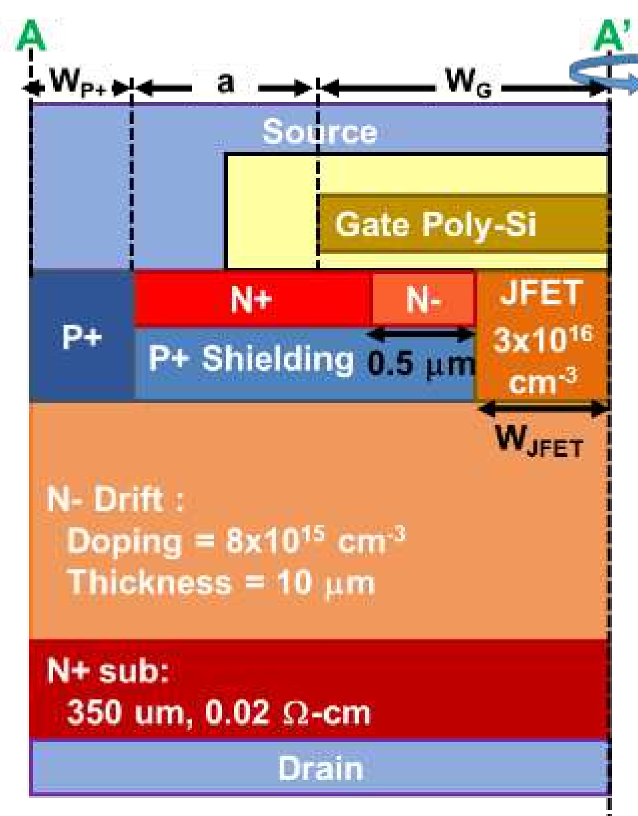
# SiC Power MOSFET: New OCTFET Cell Topology



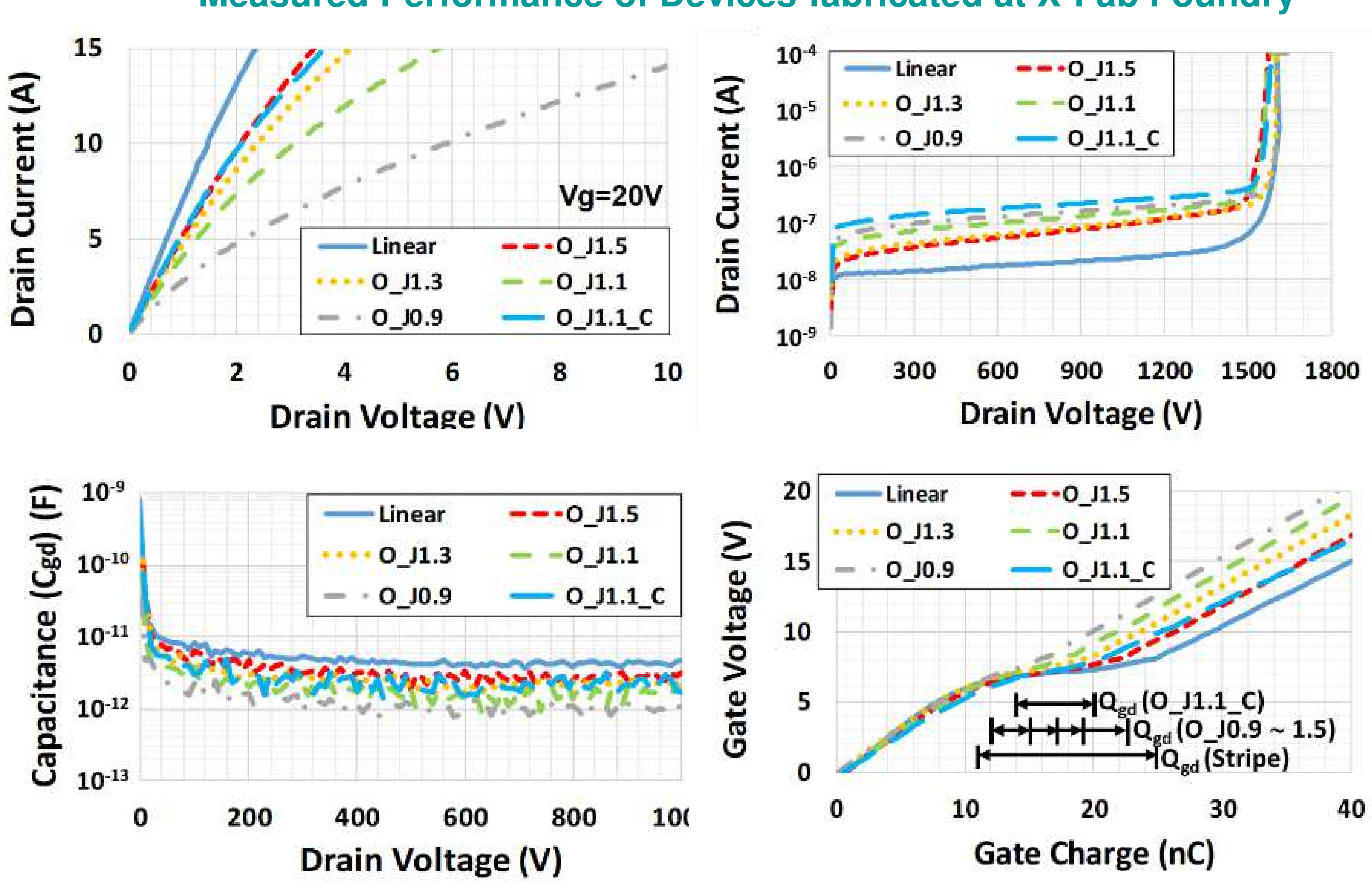

- The New Octagonal Cell Topology for the SiC Power MOSFET (OCTFET) can be fabricated with the same process as the Conventional MOSFET.
- Gate Design is different during device layout.

# SiC Power MOSFET: New OCTFET Cell Topology



# 1.2kV SiC Power OCTFET: Experimental Results

## Measured Performance of Devices fabricated at X-Fab Foundry



# SiC Power MOSFET: New OCTFET Cell Topology

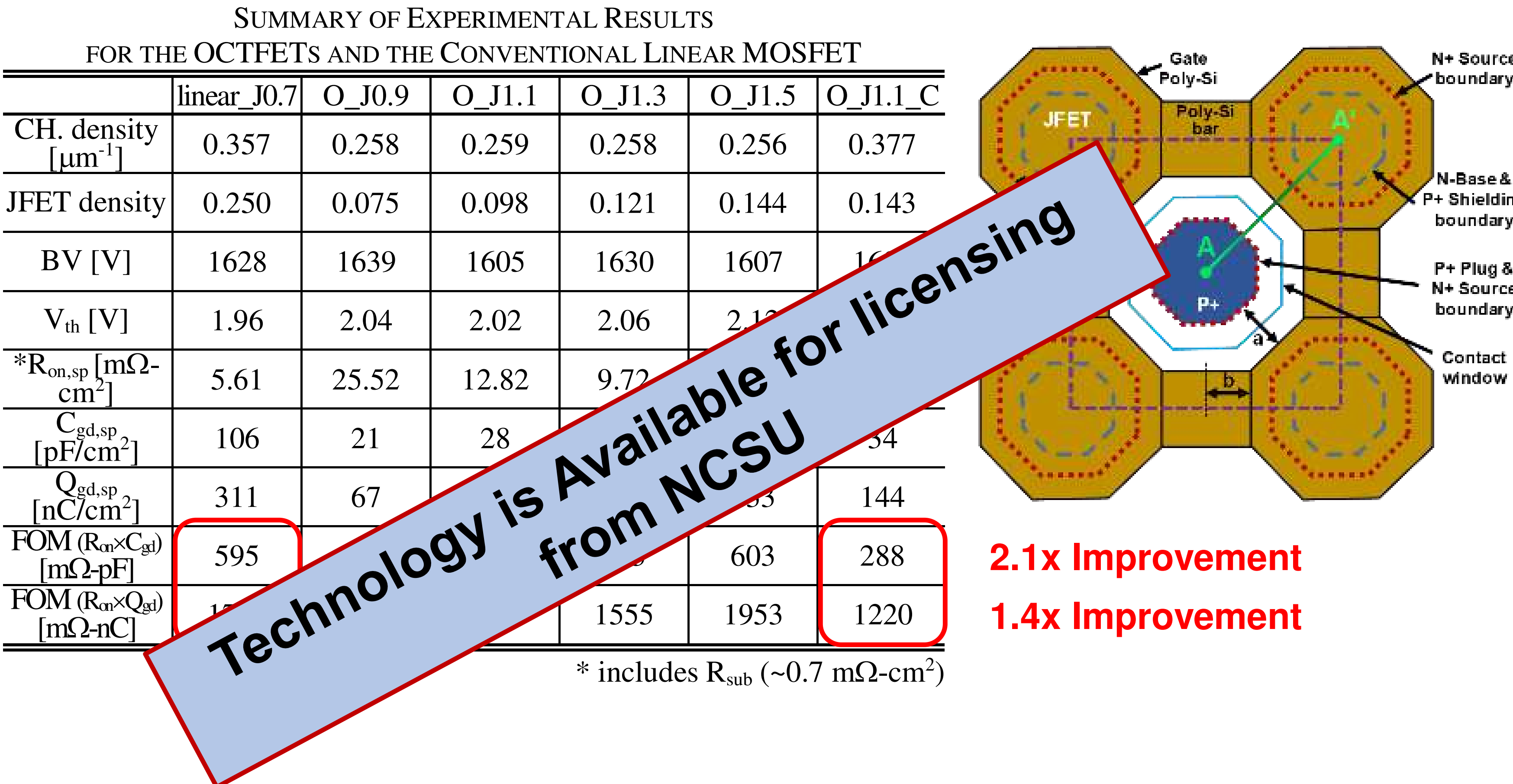


TABLE I
SUMMARY OF EXPERIMENTAL RESULTS
FOR THE OCTFETS AND THE CONVENTIONAL LINEAR MOSFET

| | linear_J0.7 | O_J0.9 | O_J1.1 | O_J1.3 | O_J1.5 | O_J1.1_C |
|---|---|---|---|---|---|---|
| CH. density [$\mu m^{-1}$] | 0.357 | 0.258 | 0.259 | 0.258 | 0.256 | 0.377 |
| JFET density | 0.250 | 0.075 | 0.098 | 0.121 | 0.144 | 0.143 |
| BV [V] | 1628 | 1639 | 1605 | 1630 | 1607 | [illegible] |
| $V_{th}$ [V] | 1.96 | 2.04 | 2.02 | 2.06 | [illegible] | [illegible] |
| *$R_{on,sp}$ [m$\Omega$-cm$^2$] | 5.61 | 25.52 | 12.82 | 9.72 | [illegible] | [illegible] |
| $C_{gd,sp}$ [pF/cm$^2$] | 106 | 21 | 28 | [illegible] | [illegible] | [illegible] |
| $Q_{gd,sp}$ [nC/cm$^2$] | 311 | 67 | [illegible] | [illegible] | [illegible] | 144 |
| FOM ($R_{on}$×$C_{gd}$) [m$\Omega$-pF] | 595 | [illegible] | [illegible] | [illegible] | 603 | 288 |
| FOM ($R_{on}$×$Q_{gd}$) [m$\Omega$-nC] | [illegible] | [illegible] | [illegible] | 1555 | 1953 | 1220 |

* includes $R_{sub}$ (~0.7 m$\Omega$-cm$^2$)



K. Han and B.J. Baliga, “The 1.2 kV 4H-SiC OCTFET: A New Cell Topology with Improved High-Frequency Figures-of-Merit", *IEEE Electron Device Letters*, Vol. 40, pp. 299-302, February 2019.

# Outline

- SiC Power MOSFET Breakthroughs achieved at NCSU
  - PRESiCE: SiC Power Device Manufacturing Technology
  - SiC Power MOSFETs: Inversion Channel & Accumulation Channel
  - The JBSFET: SiC MOSFET with Integrated Schottky Diode
  - Split-Gate (SG) MOSFET: Improved HF-FOM
  - Buffered-Gate (BG) MOSFET: Further Improved HF-FOM
  - The OCTFET: A New Cell Topology with Superior High Frequency Figures-of-Merit
  - The BiDFET: A Monolithic Bi-Directional Field Effect Transistor

# BiDFET: Monolithic Bi-Directional FET

**Cycloconverters or matrix converters require power devices with bi-directional voltage blocking and current conduction capability.**

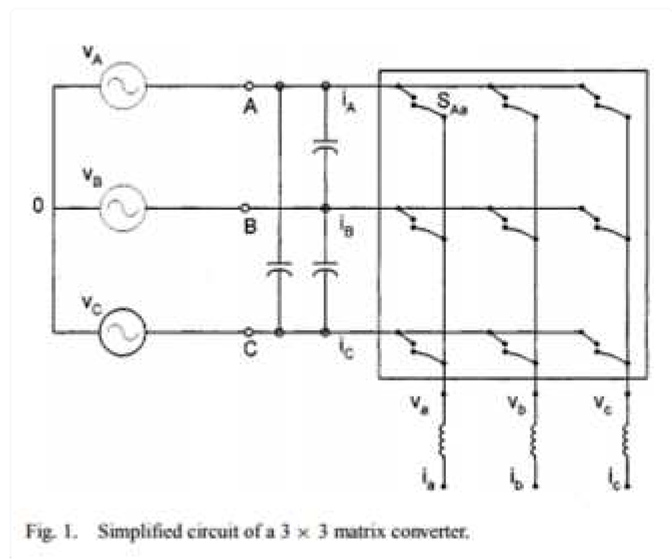
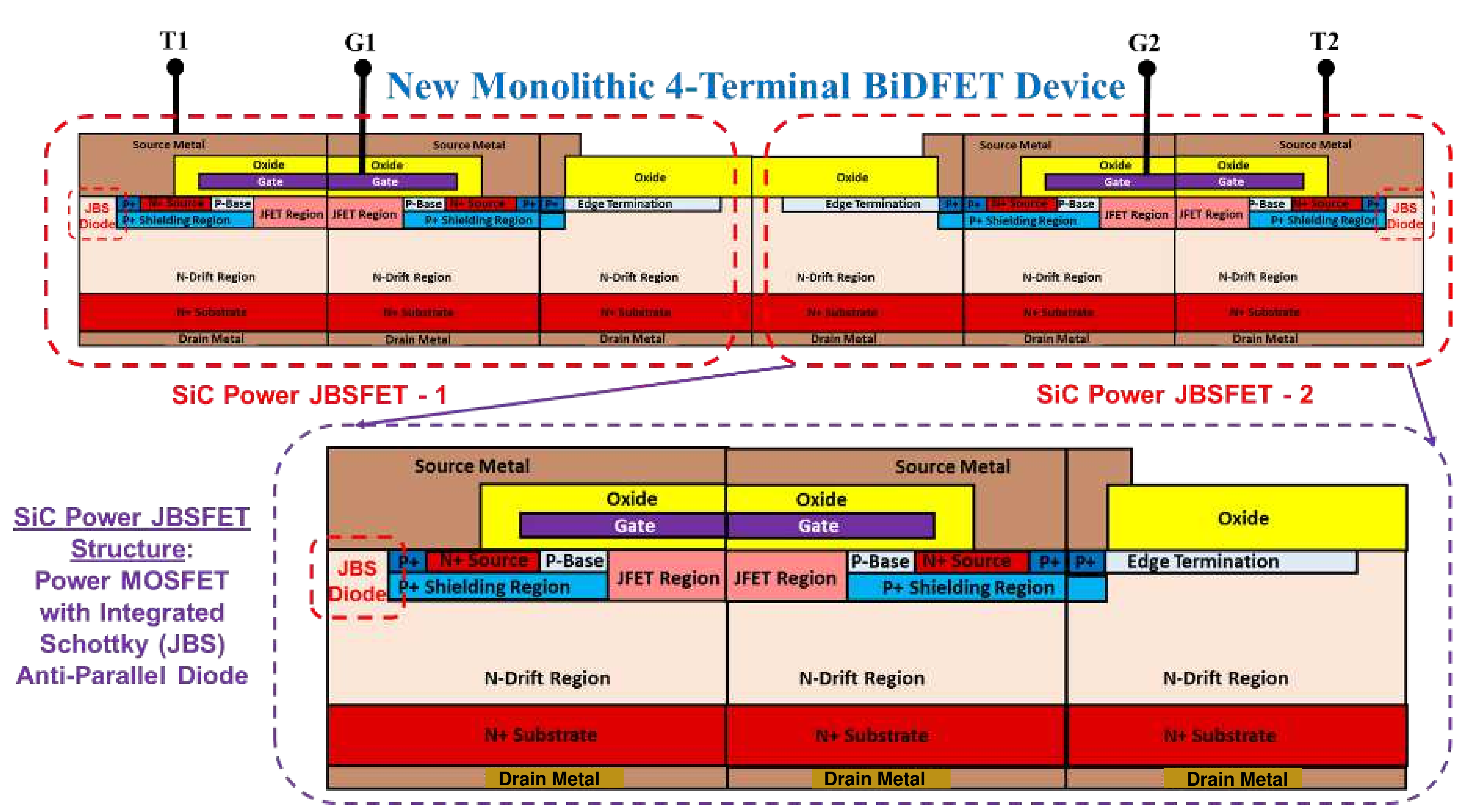



Fig. 1. Simplified circuit of a 3 × 3 matrix converter.

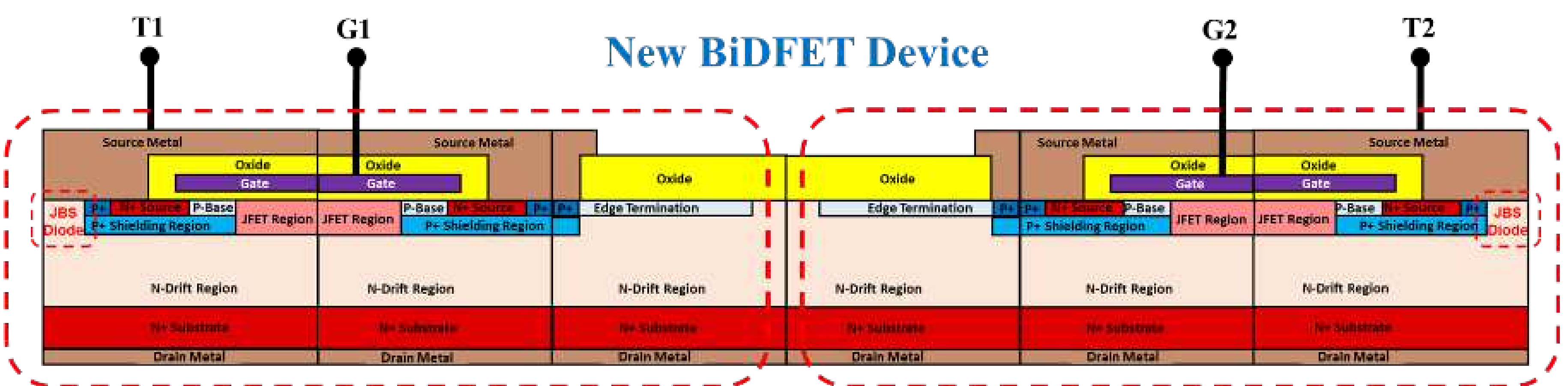
- A Matrix Converter creates a variable output voltage with unrestricted frequency using an array of fully-controlled four-quadrant bidirectional switches as the main power elements.
- It does not need any large energy storage elements and DC-link circuit.
- "Unfortunately, there were no such devices available."
- "Consequently, multiple discrete devices had to be used to construct suitable switch cells."

P.W. Wheeler, J. Rodriguez, J.C. Clare, L. Empringham, and A. Weinstein, "Matrix Converters: A Technology Review", *IEEE Trans. Industrial Electronics*, vol. 49, no. 2, pp. 276–288, April 2002.

# Proposed SiC Bi-Directional FET – BiDFET



# BiDFET: Experimental Results




SiC Power JBSFET - 1

SiC Power JBSFET - 2

## Operation in First Quadrant

- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- JBSFET-1 Blocks Voltage if V(G1-T1) = 0
- Blocking Voltage = 1650 V
- Low leakage current in spite of Schottky Contact

W. Sung and B.J. Baliga, “Monolithically Integrated 4H-SiC MOSFET and JBS Diode (JBSFET) using a Single Ohmic/Schottky Process Scheme” IEEE Electron Device Letters, Vol. 37, No. 7, pp. 1605-1608, Oct. 2016

BV = 1650 V

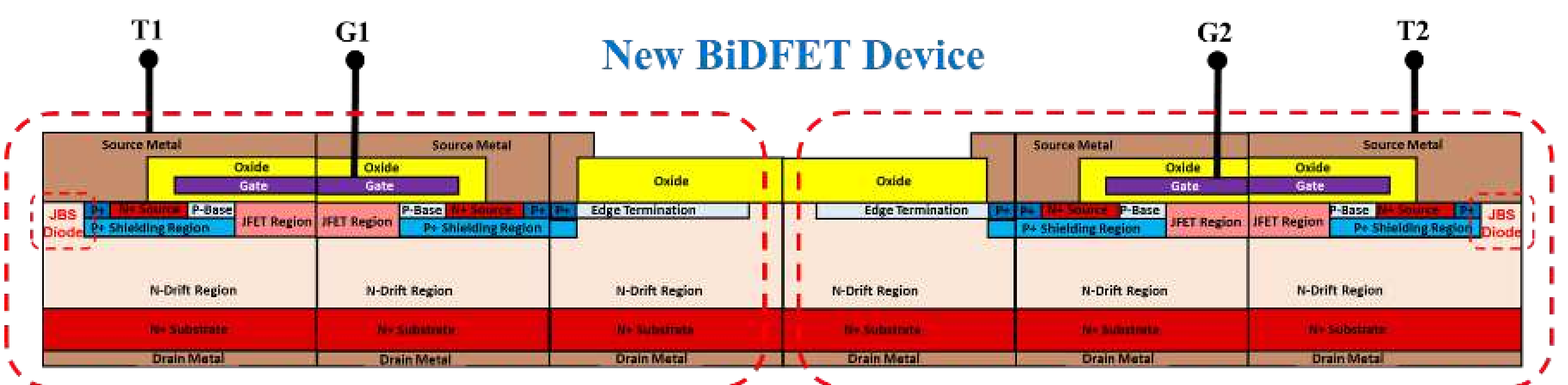
Low Leakage

Terminal T2 Current (Amps): $10^{-4}$, $10^{-5}$, $10^{-6}$, $10^{-7}$, $10^{-8}$, $10^{-9}$

Terminal T2 Voltage (Volts): 0, 300, 600, 900, 1200, 1500, 1800

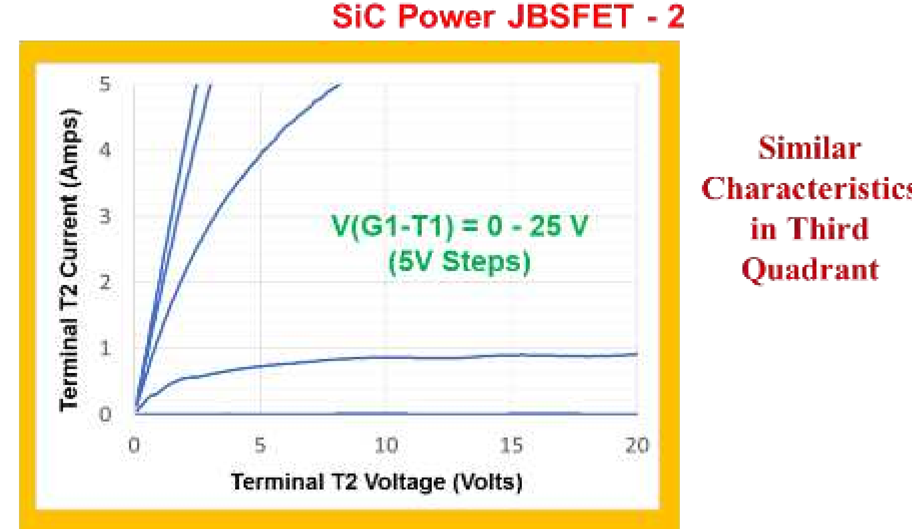
Similar Characteristics in Third Quadrant

# BiDFET: Experimental Results




SiC Power JBSFET - 1

SiC Power JBSFET - 2

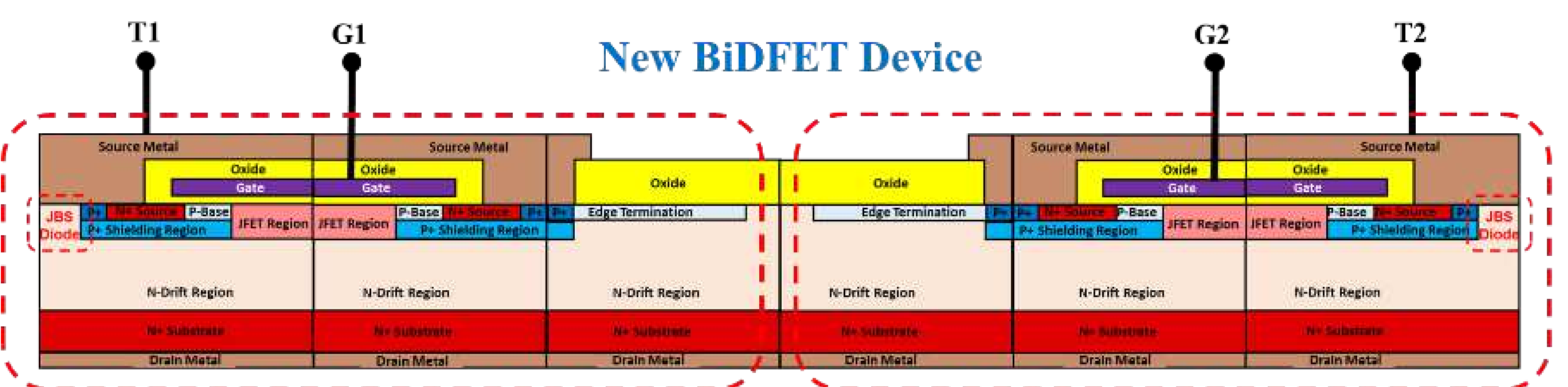



Similar Characteristics in Third Quadrant

## Operation in First Quadrant

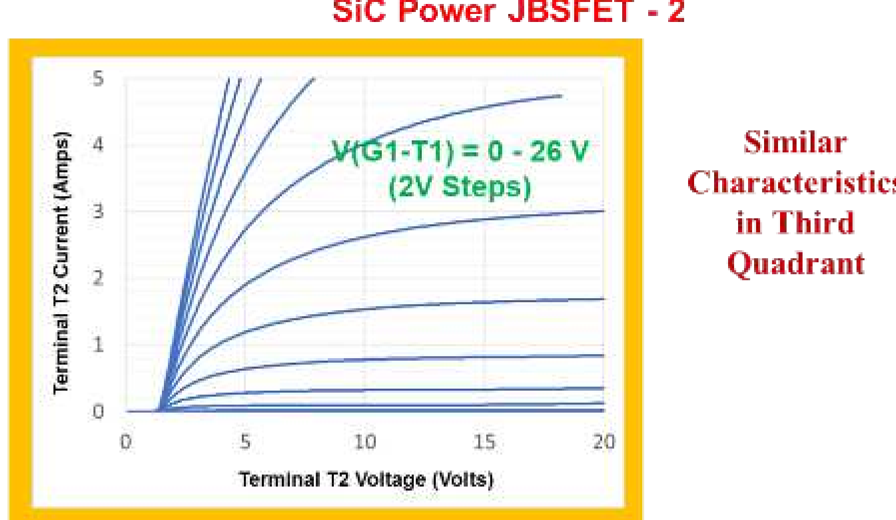
- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- Gate Bias for JBSFET-2: V(G2-T2) = 25 V
- Current flows through channel within JBSFET-2
- Gate Bias for JBSFET-1 Varied (5 V steps to 25 V)
- On-state Resistance = 0.5 Ω – Can be reduced with larger active area.
- Current Saturation with good Safe-Operating-Area

# BiDFET: Experimental Results




## Operation in First Quadrant

- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- Gate Bias for JBSFET-2: V(G2-T2) = 0 V
- Current flows through JBS Diode within JBSFET-2
- Gate Bias for JBSFET-1 Varied (2 V steps to 26 V)
- Knee is observed at 1.5 V in output characteristics.
- Current Saturation with good Safe-Operating-Area




Similar Characteristics in Third Quadrant

# BiDFET: Comparison with Prior Art

| AC Switch Option | | | Number of Devices & Packages per Leg | On-State Voltage Drop |
|---|---|---|---|---|
| | Si Devices | Case (a) | 5 | 5.0 V |
| | Si Devices | Case (b) | 4 | 3.5 V |
| | Si Devices | Case (c) | 2 | 2.5 V |
| | SiC Devices | Case (d) | 4 | 1.75 V |
| | SiC Devices | Case (e) | 4 | 1.75 V |
| | SiC BiDFET | | 1 | 0.5 V |

- **Assumptions:**
- Si Diode On-State Voltage Drop = 1.5 V
- Si Asymmetric IGBT On-State Voltage Drop = 2.0 V
- Si Symmetric (RB) IGBT On-State Voltage Drop = 2.5 V
- SiC Diode On-State Voltage Drop = 1.5 V
- SiC MOSFET On-State Voltage Drop = 0.25 V

# BiDFET: Monolithic Bi-Directional FET

- A Novel Monolithic 4-Terminal Bi-Directional Field Effect Transistor (BiDFET) based up on SiC Technology has been proposed and demonstrated for application to Matrix Converters.
- The key attributes of the device are:
  - High blocking voltage in first and third quadrants
  - Current conduction in first and third quadrants with low on-resista
  - Current saturation with gate bias control in first and third qua
  - Fast switching capability of SiC power MOSFETs
  - Large SOA with ruggedness of SiC power MOSFETs
- Advantages when compared with previous appro
  - Single device
  - Only one package
  - Low on-state resistance and
  - Can be Manufactured in foundry

**Technology is Available for licensing from NCSU**

G2
T1
T2

The authors wish to a of the PowerAmerica Institute.
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B.J. Baliga and K. Han, "Monolithic SiC Bi-Directional Field Effect Transistor (BiDFET): Concept, Implementation, and Electrical Characteristics ", *GOMACTech 2018*, Paper 3.2, pp. 32-35, March 13, 2018.

# Conclusion

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