NCSU Breakthroughs in SiC Power MOSFET Technology
Progress Energy Distinguished University Professor
Jay Baliga

April 11, 2019

Acknowledgements
SiC Power MOSFET Breakthroughs achieved at NCSU

- **PRESiCE**: SiC Power Device Manufacturing Technology
- **SiC Power MOSFETs**: Inversion Channel & Accumulation Channel
- **The JBSFET**: SiC MOSFET with Integrated Schottky Diode
- **Split-Gate (SG) MOSFET**: Improved HF-FOM
- **Buffered-Gate (BG) MOSFET**: Further Improved HF-FOM
- **The OCTFET**: A New Cell Topology with Superior High Frequency Figures-of-Merit
- **The BiDFET**: A Monolithic Bi-Directional Field Effect Transistor
Outline

- SiC Power MOSFET Breakthroughs achieved at NCSU
  - PRESiCE: SiC Power Device Manufacturing Technology
  - SiC Power MOSFETs: Inversion Channel & Accumulation Channel
  - The JBSFET: SiC MOSFET with Integrated Schottky Diode
  - Split-Gate (SG) MOSFET: Improved HF-FOM
  - Buffered-Gate (BG) MOSFET: Further Improved HF-FOM
  - The OCTFET: A New Cell Topology with Superior High Frequency Figures-of-Merit
  - The BiDFET: A Monolithic Bi-Directional Field Effect Transistor
PRESiCE: PRocess Engineered for manufacturing SiC Electronic-Devices

SiC Power Electronic-Devices

Qualification Procedure:
(1) Define Process Flow (NCSU) for Manufacturing SiC Power MOSFETs, JBSFETs, and JBS Rectifiers at X-Fab.
(2) Design a Mask Set (NCSU) for Manufacturing SiC Power MOSFETs, JBSFETs, and JBS Rectifiers at X-Fab for Qualifying the process.
(3) Fabricated Three Process Lots at X-Fab.
(4) Obtained Statistical Data (NCSU) on device parameters to confirm tight distribution of parameters from within each wafer, from wafer-to-wafer within each process lot, and from lot-to-lot.

Data Acquisition Equipment:
  - 6 inch wafer capability
  - 3 kV chuck isolation
  - High Temp (300 oC)
(2) New Keysight Test Equipment.
  - Maximum Voltage = 3 kV
  - Maximum Current = 20 A
1.2 kV JBS Rectifier Process Qualification

- Process Qualification using Three Lots at X-Fab
- Device #2: JBS Rectifier with Nickel Schottky Contact
- Active Area = 0.046 cm²


6 inch SiC wafer fabricated at X-Fab
On-state Voltage Drop [V] @ If = 5A

JBS Rectifier with Nickel Schottky Contact (Within Lot Variation)

Lot-3-W3-#2

Average = 2.00 V

Std. Dev. : 0.05

Lot-3-W6-#2

Average = 2.05 V

Std. Dev. : 0.06
JBS Rectifier with Nickel Schottky Contact (Within Lot Variation)

Leakage Current ($I_L$) [nA] @ $V_d=1000$ V, RT

Lot-3-W3-#2

Yield : 98.7%

Yield based on allowable maximum leakage current of 100 µA

Lot-3-W6-#2

Yield : 95.3%
JBS Rectifier with Nickel Schottky Contact (Lot-to-Lot Variation)

On-state Voltage Drop [V] @ if = 5A, RT

Lot-3-W3-#2 - Average = 2.00 V
Lot-4-W3-#2 - Average = 1.94 V
Lot-5-W3-#2 - Average = 2.06 V

Std. Dev. : 0.05
Std. Dev. : 0.03
Std. Dev. : 0.07

Average = 2.00 V
Average = 1.94 V
Average = 2.06 V
**JBS Rectifier with Nickel Schottky Contact (Lot-to-Lot Variation)**

### Leakage Current ($I_L$) [nA] @ Vd=1000 V, RT

**Lot-3-W3-#2**

<table>
<thead>
<tr>
<th>Leakage Current [nA]</th>
<th>Frequency Distribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>58.9</td>
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<tr>
<td>3.0</td>
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<tr>
<td>4.0</td>
<td>578.6</td>
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<tr>
<td>4.5</td>
<td>54.8</td>
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<tr>
<td>5.0</td>
<td>103.0</td>
</tr>
<tr>
<td>5.5</td>
<td>342.2</td>
</tr>
<tr>
<td>6.0</td>
<td>92.4</td>
</tr>
</tbody>
</table>

Yield: 98.7%

**Lot-4-W3-#2**

<table>
<thead>
<tr>
<th>Leakage Current [nA]</th>
<th>Frequency Distribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5</td>
<td>2.8</td>
</tr>
<tr>
<td>3.0</td>
<td>13688.1</td>
</tr>
<tr>
<td>2.5</td>
<td>9016.0</td>
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<tr>
<td>2.0</td>
<td>280.0</td>
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<tr>
<td>1.5</td>
<td>75.5</td>
</tr>
<tr>
<td>1.0</td>
<td>258.7</td>
</tr>
</tbody>
</table>

Yield: 94.7%

**Lot-5-W3-#2**

<table>
<thead>
<tr>
<th>Leakage Current [nA]</th>
<th>Frequency Distribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.2</td>
<td>17.1</td>
</tr>
<tr>
<td>3.5</td>
<td>20.1</td>
</tr>
<tr>
<td>2.5</td>
<td>25.4</td>
</tr>
<tr>
<td>2.0</td>
<td>2.9</td>
</tr>
<tr>
<td>1.5</td>
<td>4890.0</td>
</tr>
<tr>
<td>1.0</td>
<td>30493.9</td>
</tr>
</tbody>
</table>

Yield: 96.7%

Yield based on allowable maximum leakage current of 100 µA
Accumulation Channel MOSFET (ACCUFET)

- Process Qualification using Three Process Lots at X-Fab
- Device #5: Accumulation Channel MOSFET (ACCUFET) with JFET Implant
  - Active Area = 0.045 cm²

Technical Note:
- The $R_{ds,on}$ values in the Wafer Maps and Statistical Data plots include 35 mΩ of parasitic probe (~1 mΩ-cm²) and substrate (~1 mΩ-cm²) resistance.
- The $C_{gd}$ values in Wafer Maps and Statistical data include 0.5 pF of parasitic probe capacitance.

Accumulation Channel MOSFET (ACCUFET) (Within Lot Variation)

**On-Resistance ($R_{on}$) [mΩ] @ $I_d=1A$, $V_g=25V$, RT - 6.5 mΩ-cm²**

**Lot-4-W1-#5**

- Average = 137 mΩ
- Std. Dev.: 3.29

**Lot-4-W2-#5**

- Damaged during the BV test w/o Flourinert
- Average = 139 mΩ
- Std. Dev.: 5.57

Typical value is the Average of All Devices from All Three Lots

- Typical: 144 mΩ (Allowable Max: 187 mΩ (30% more)) ➞ All devices meet specifications
Accumulation Channel MOSFET (ACCUFET) (Within Lot Variation)

Threshold Voltage ($V_{\text{th}}$) [V] @ $I_d = 1$ mA, $V_d = 0.1$ V, RT

Lot-4-W1-#5

Average = 2.03 V

Std. Dev. : 0.14

Typical value is the Average of All Devices from All Three Lots

Lot-4-W2-#5

Average = 2.48 V

Std. Dev. : 0.16

Typical : 2.33 V (Allowable Max : 3.50 V (50 % more)) ➞ All devices meet specifications
Accumulation Channel MOSFET (ACCUFET) (Within Lot Variation)

Cgd [pF] @ Vd=1000 V, RT

Lot-5-W1-#5

Lot-5-W2-#5

Average = 9.51 pF

Average = 9.86 pF

Std. Dev. :0.489

Std. Dev. :0.543

Gate to Drain Capacitance

Gate to Drain Capacitance
Accumulation Channel MOSFET (ACCUFET) (Within Lot Variation)

Leakage Current ($I_L$) \[\text{[nA]}\] @ $V_d=1000$ V, RT

<table>
<thead>
<tr>
<th>Lot-4-W1-#5</th>
<th>Lot-4-W2-#5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yield : 95.3%</td>
<td>Yield : 92.7%</td>
</tr>
</tbody>
</table>

Yield based on allowable maximum leakage current of 100 $\mu$A
Accumulation Channel MOSFET (ACCUFET) (Lot-to-Lot Variation)

On-Resistance ($R_{on}$) [mΩ] @ Id=1A, Vg=25V, RT

Lot-3-W1-#5

- Average = 149 mΩ
- Std. Dev. : 2.75

Lot-4-W1-#5

- Average = 139 mΩ
- Std. Dev. : 5.57

Lot-5-W1-#5

- Average = 150 mΩ
- Std. Dev. : 3.60

- Damaged during the BV test w/o Flourinert

Typical : 144 mΩ (Allowable Max : 187 mΩ (30 % more)) ➔ All devices meet specifications
Accumulation Channel MOSFET (ACCUFET) (Lot-to-Lot Variation)

Threshold Voltage ($V_{th}$) [V] @ $I_d = 1$ mA, $V_d = 0.1$ V, RT

Lot-3-W1-#5

Average = 2.33 V

Typical : 2.33 V (Allowable Max : 3.50 V (50 % more)) ➞ All devices meet specifications

Lot-4-W1-#5

Average = 2.03 V

Lot-5-W1-#5

Average = 2.36 V

Std. Dev. : 0.13

Std. Dev. : 0.135

Std. Dev. : 0.153
Accumulation Channel MOSFET (ACCUFET) (Lot-to-Lot Variation)

Lot-3-W1-#5
Lot-4-W1-#5
Lot-5-W1-#5

□ Damaged during the BV test w/o Flourinert

Cgd [pF] @ Vd=1000 V, RT

Lot-3-W1-#5
Lot-4-W1-#5
Lot-5-W1-#5

Average = 10.73 pF
Average = 9.64 pF
Average = 9.51 pF

Std. Dev. : 0.21
Std. Dev. : 0.25
Std. Dev. : 0.49
Accumulation Channel MOSFET (ACCUFET) (Lot-to-Lot Variation)

Leakage Current ($I_L$) [nA] @ $V_d=1000$ V, RT

Lot-3-W1-#5
- Yield: 93.3%
- Leakage Current ($I_L$) [nA]: 4.02, 7.42, 4.39, 3.06, 2.63, 24.89, 3.11, 2.85, 6.77, 6.14, 12.95, 4.58, 3.41, 4.73, 5.20, 3.43, 2.87, 2.40, 1.992, 10.63, 14.37, 4.92, 5.12, 8.52, 3.65, 3.24, 3.04, 5.12, 17.08, 6.43, 14.93, 65.87, 16.70, 1163, 6.58, 35.49, 73.04, 3.61, 3.46, 3.04, 4.19, 14.83, 4.42, 3.92, 2.60, 27.31, 14.10, 300, 6.92, 7.75, 8.87, 4.13, 4.27, 11.89, 5.37, 6.70, 5510, 27.63, 25.18, 25.18, 77098, 6.65, 8.24, 37.79, 10.59, 4.60, 3.53, 3.62, 5.18, 13.68, 32.20, 3.68, 16.03, 28.93, 7.65, 9.59, 427, 3.95, 4.52, 4.07, 6.24, 10.75, 2215, 11.54, 26.43, 17.39, 10.25, 4.13, 12.75, 8.48, 8.16, 533, 3.96, 6.34, 12.78, 5.30, 10.77, 6.60, 162, 14.12, 10.63, 5.96, 4.16, 3.94, 6.94, 4.51, 11.12, 8.48, 7.23, 3.68, 44.88, 199, 200, 765, 6.03, 4.87, 11.21, 10.98, 5.61, 3.66, 3.00, 7.26, 13.84, 239, 3.85, 6.30, 7.12, 12.75, 3.54, 454, 4.71, 12.04, 12.14, 2.83, 5.85

Lot-4-W1-#5
- Yield: 95.3%
- Leakage Current ($I_L$) [nA]: 336.772, 62212, 17.5, 521, 17.0, 125.9, 95.2, 41.5, 10.7, 16.3, 233.48, 13.0, 6.0, 54.9, 95.8, 126.9, 216.4, 443.7, 20.2, 353, 43.2, 16.7, 15.7, 6.0, 17.5, 122.8, 98.3, 311.5, 207.8, 95.8, 34.7, 58.6, 49.4, 22.9, 12.0, 6.4, 12.4, 11.8, 125.9, 71.1, 78.2, 151.6, 137.3, 60.5, 35.4, 73.5, 61.9, 18.1, 22.8, 14.1, 63.6, 21.0, 31.7, 126.2, 165.8, 165.8, 143.7, 35.4, 121.3, 69.1, 31.9, 20.2, 14.2, 26.6, 27.8, 39.3, 51.1, 51.1, 73.5, 148.1, 631, 132.9, 23.8, 29.8, 17.6, 34.8, 41.3, 15.9, 75.5, 66.4, 161.0, 64.4, 23.3, 66.1, 45.7, 18.1, 24.5, 15.1, 35.2, 57.0, 39.7, 72.5, 104.7, 37.2, 16.4, 23.7, 58.2, 40.1, 19.8, 27.9, 20.4, 57.3, 86.8, 84.4, 83.0, 162.5, 25.8, 13.1, 39.3, 4984, 43.4, 19.5, 32.0, 26.7, 85.6, 141.4, 40.6, 16.6, 8.0, 16.6, 46.8, 26.1, 42.7, 36.1, 52.3, 72.9, 13.0, 25.0, 50.9, 18.4, 16.0, 76.4

Lot-5-W1-#5
- Yield: 96%
- Leakage Current ($I_L$) [nA]: 22.851, 92.367, 3.10, 3.27, 7.78, 6.64, 5.58, 5.48, 4.27, 22.14, 3.06, 4.81, 3.03, 2.68, 2.28, 2.53, 18.07, 35.24, 4.68, 5.67, 1164, 3.00, 84.93, 3.03, 3.28, 2.58, 48.71, 34.97, 15.38, 7.13, 6.14, 6.58, 6.11, 5.09, 3.79, 3.16, 3.07, 2.98, 4.16, 17.96, 16.18, 9.35, 13.23, 11.15, 5.74, 5.07, 4.72, 4.39, 21.83, 3.37, 3.03, 2.66, 5.00, 51.2, 44.40, 40.22, 8.48, 8.99, 13.96, 4.70, 3.91, 3.58, 3.09, 2.40, 7.16, 21.47, 10.22, 10.22, 7.48, 9.53, 4.82, 4.40, 3.82, 3.77, 3.37, 2.54, 7.23, 62.08, 17.94, 13.25, 7.79, 9.88, 7.47, 5.87, 4.93, 3.96, 4.25, 4.32, 3.71, 2.80, 13.22, 64.94, 9.73, 6.55, 8.71, 5.64, 160, 4.17, 5.77, 4.37, 4.67, 4.98, 4.69, 3.85, 16.05, 12.78, 6.94, 5.09, 6.91, 4.90, 14.49, 4.62, 5.54, 5.54, 5.18, 2.95, 9.32, 7.77, 5.44, 3.88, 3.88, 6.26, 5.61, 7.12, 5.81, 6.55, 21.86, 4.86, 14.48, 24.10, 15.50, 6.08, 62.71

Yield based on allowable maximum leakage current of 100 μA
Inversion Channel MOSFET (INVFET)

- Process Qualification using Three Process at X-Fab
- Device #5: Inversion Channel MOSFET (INVFET) with JFET Implant
  - Active Area = 0.045 cm²
- Similar Results like Accumulation Channel devices

PRESiCE Technology is available for licensing from NCSU for manufacturing products at X-Fab
SiC Power MOSFET Breakthroughs achieved at NCSU

- **PRESiCE**: SiC Power Device Manufacturing Technology
- **SiC Power MOSFETs**: Inversion Channel & Accumulation Channel
- **The JBSFET**: SiC MOSFET with Integrated Schottky Diode
- **Split-Gate (SG) MOSFET**: Improved HF-FOM
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JBSFET: MOSFET with Integrated JBS Diode

MOSFET
Cell pitch 11um
Simulated $R_{on,sp}=6.8 \text{ m}\Omega\cdot\text{cm}^2$
(assuming $\mu_{ch}=13 \text{ cm}^2/\text{V} \cdot \text{s}$)

JBSFET
Cell pitch 16um
$R_{on,sp}=10 \text{ m}\Omega\cdot\text{cm}^2$
(assuming $\mu_{ch}=13 \text{ cm}^2/\text{V} \cdot \text{s}$)

Drift layer
$N_d=8 \times 10^{15} \text{ cm}^{-3}$
$W_d=10\text{um}$

# JBSFET Area Savings Analysis

## Layout comparison for 1.2 kV, 5.7 A Devices

<table>
<thead>
<tr>
<th>Approaches</th>
<th>Active area (cm²)</th>
<th>Edge termination And periphery</th>
<th>Total area (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Previous approach</td>
<td>0.0212 (MOSFET) 0.0263 (JBS)</td>
<td>0.0110 (MOSFET) 0.0122 (JBS)</td>
<td>0.0322+ 0.0385 = <strong>0.0707</strong></td>
</tr>
<tr>
<td>PA approach 1 JBSFET1</td>
<td>0.0284 (5.72A MOSFET*)</td>
<td>0.0126</td>
<td><strong>0.041</strong></td>
</tr>
<tr>
<td>PA approach 2 JBSFET2</td>
<td>0.0281</td>
<td>0.0126</td>
<td><strong>0.0407</strong></td>
</tr>
<tr>
<td>PA approach 3 JBSFET3</td>
<td>0.0475</td>
<td>0.016</td>
<td><strong>0.0635</strong></td>
</tr>
</tbody>
</table>

**Assumptions:**
- Edge termination design: 10 floating field rings – 3um wide, total spacing is about 20um, which gives about 50um total width for edge termination
- Periphery: Edge termination to C/S implant – 20um, dicing lane 70um per side, C/S to dicing 30um-> total 120um
- *Comparison with a 5.72A pure MOSFET: 0.0242 active + 0.0117 periphery = 0.036 cm²
Conclusion: Area Savings of about 40% can be achieved with the JBSFET Approach

Other Benefits: Cuts package count in half.
Reduces switching loss by 40% at elevated temperatures.
Measured Data - JBSFET I-V

JBSFET Id-Vd, Active area 4.5mm²

Specific on resistance: 20 mohm-cm² @ Vg = 25 V

JBSFET V(on) at 5A: 2 V
MOSFET V(on) at 5A: 4.5 V
Accumulation Channel JBSFET

- Process Qualification using Three Process Lots at X-Fab
- Device #7: Accumulation Channel JBSFET with JFET Implant
- Active Area = 0.045 cm²

Technical Note:

- The R_{ds,on} values in the Wafer Maps and Statistical Data plots include 35 mΩ of parasitic probe (≈ 1 mΩ-cm²) and substrate (≈ 1 mΩ-cm²) resistance.
- The C_{gd} values in Wafer Maps and Statistical data include 0.5 pF of parasitic probe capacitance.

Accumulation Channel JBSFET (Lot-to-Lot Variation)

On-Resistance ($R_{on}$) [mΩ] @ $I_d=1A$, $V_g=25V$, $R_T$ – 11 mΩ-cm²

Lot-3-W3-#7

Lot-4-W3-#7

Lot-5-W3-#7

Typical: 250 mΩ (Allowable Max: 325 mΩ (30% more)) ➞ All devices meet specifications
Accumulation Channel JBSFET (Lot-to-Lot Variation)

**Threshold Voltage** ($V_{\text{th}}$) [V] @ $I_d = 1$ mA, $V_d = 0.1$ V, RT

**Lot-3-W3-#7**
- Average = 2.43 V
- Std. Dev. : 0.10

**Lot-4-W3-#7**
- Average = 2.31 V
- Std. Dev. : 0.11

**Lot-5-W3-#7**
- Average = 2.50 V
- Std. Dev. : 0.11

Typical : 2.41 V (Allowable Max : 3.62 V (50 % more)) ➔ All devices meet specifications
Accumulation Channel JBSFET (Lot-to-Lot Variation)

3rd Quadrant ($V_f$) [V]@ If = 5A, RT

Lot-3-W3-#7

Lot-4-W3-#7

Lot-5-W3-#7

Average = 2.25 V

Average = 2.21 V

Average = 2.33 V

Std. Dev. : 0.048

Std. Dev. : 0.032

Std. Dev. : 0.072
Accumulation Channel JBSFET (Lot-to-Lot Variation)

Leakage Current ($I_L$) [nA] @ $V_d=1000$ V, RT

Lot-3-W3-#7

Lot-4-W3-#7

Lot-5-W3-#7

JBSFET Technology is Available for licensing from NCSU

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  - **The OCTFET**: A New Cell Topology with Superior High Frequency Figures-of-Merit
  - **The BiDFET**: A Monolithic Bi-Directional Field Effect Transistor
The Split-Gate SiC Power MOSFET can be fabricated with the same process as used for the Conventional MOSFET.

Gate Design is different during device layout.
Split-Gate (SG) SiC Power MOSFET

Conventional MOSFET

Optimum X is 0.3 µm based on alignment tolerances
Split-Gate (SG) SiC Power MOSFET: Experimental Results
<table>
<thead>
<tr>
<th></th>
<th>MOSFET</th>
<th>SG-MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown voltage [V]</td>
<td>1634</td>
<td>1626</td>
</tr>
<tr>
<td>Threshold voltage [V]</td>
<td>2.00</td>
<td></td>
</tr>
<tr>
<td>(R_{on,sp} ) [m(\Omega)-cm(^2)]</td>
<td>6.35</td>
<td>6.30</td>
</tr>
<tr>
<td>(C_{gd,sp} ) [pF/cm(^2)] (@(V_d)=0V)</td>
<td></td>
<td>15890</td>
</tr>
<tr>
<td>(C_{gd,sp} ) [pF/cm(^2)] (@(V_d)=1kV)</td>
<td></td>
<td>110</td>
</tr>
<tr>
<td>(Q_{gd,sp} ) [nC/cm(^2)]</td>
<td></td>
<td>351</td>
</tr>
<tr>
<td>FOM &lt;(R\times C) (@(V_d)=0V)</td>
<td>100890</td>
<td>16520</td>
</tr>
<tr>
<td>FOM &lt;(R\times C) (@(V_d)=1kV)</td>
<td>766</td>
<td>589</td>
</tr>
<tr>
<td></td>
<td>2230</td>
<td>938</td>
</tr>
</tbody>
</table>

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The Buffered-Gate SiC Power MOSFET can be fabricated with one additional (N+ JFET) Step compared with the Conventional MOSFET.

Gate Design is different during device layout.
Optimization of N+ JFET Doping Concentration

3E17 cm-3 is Optimum to:

- Reduce Specific On-Resistance
- Maintain Low Gate Oxide Electric Field
Buffered-Gate (BG) SiC Power MOSFET

\[ X_1 = 0.4 \, \mu m \]

X2 is P+ Shielding Region Extension beyond Gate Edge

Optimum X2 is 0.3 \( \mu m \) based on alignment tolerances
Buffered-Gate (BG) SiC Power MOSFET: Experimental Results
### TABLE I
SUMMARY OF EXPERIMENTAL RESULTS
FOR C-MOSFET, SG-MOSFET, AND BG-MOSFETs

<table>
<thead>
<tr>
<th></th>
<th>C-MOSFET</th>
<th>SG-MOSFET</th>
<th>BG-MOSFET</th>
<th>BG-MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell pitch [µm]</td>
<td>5.6</td>
<td>5.6</td>
<td>7.0</td>
<td>7.0</td>
</tr>
<tr>
<td>BV [V]</td>
<td>1689</td>
<td>1688</td>
<td>1623</td>
<td>1617</td>
</tr>
<tr>
<td>Vth [V]</td>
<td>1.84</td>
<td>1.80</td>
<td>1.72</td>
<td>2.04</td>
</tr>
<tr>
<td>R_{on,sp} [mΩ-cm²]</td>
<td>5.78</td>
<td>5.96</td>
<td>10.73</td>
<td>8.39</td>
</tr>
<tr>
<td>C_{gd,sp} [pF/cm²]</td>
<td>121</td>
<td>21</td>
<td>68</td>
<td>21</td>
</tr>
<tr>
<td>Q_{gd,sp} [nC/cm²]</td>
<td>347</td>
<td>216</td>
<td>56</td>
<td>60</td>
</tr>
<tr>
<td>FOM &lt;R_{on}×C_{gd}&gt;</td>
<td>406</td>
<td>229</td>
<td>194</td>
<td></td>
</tr>
<tr>
<td>[mΩ-pF]</td>
<td></td>
<td></td>
<td></td>
<td>194</td>
</tr>
<tr>
<td>FOM &lt;R_{on}×Q_{gd}&gt;</td>
<td>1287</td>
<td>596</td>
<td>503</td>
<td></td>
</tr>
<tr>
<td>[mΩ-nC]</td>
<td></td>
<td></td>
<td></td>
<td>503</td>
</tr>
</tbody>
</table>

Outline

- **SiC Power MOSFET Breakthroughs achieved at NCSU**
  - **PRESiCE**: SiC Power Device Manufacturing Technology
  - **SiC Power MOSFETs**: Inversion Channel & Accumulation Channel
  - **The JBSFET**: SiC MOSFET with Integrated Schottky Diode
  - **Split-Gate (SG) MOSFET**: Improved HF-FOM
  - **Buffered-Gate (BG) MOSFET**: Further Improved HF-FOM
  - **The OCTFET**: A New Cell Topology with Superior High Frequency Figures-of-Merit
  - **The BiDFET**: A Monolithic Bi-Directional Field Effect Transistor
SiC Power MOSFET: New OCTFET Cell Topology

- The New Octagonal Cell Topology for the SiC Power MOSFET (OCTFET) can be fabricated with the same process as the Conventional MOSFET.
- Gate Design is different during device layout.
SiC Power MOSFET: New OCTFET Cell Topology
1.2kV SiC Power OCTFET: Experimental Results

Measured Performance of Devices fabricated at X-Fab Foundry

- Drain Current vs Drain Voltage
- Capacitance (Cgd) vs Drain Voltage
- Drain Current vs Drain Voltage
- Gate Voltage vs Gate Charge

Sweep parameters:
- Vg = 20V

Graphs show the performance of devices with different channel lengths and channel widths.
### TABLE I
SUMMARY OF EXPERIMENTAL RESULTS FOR THE OCTFETs AND THE CONVENTIONAL LINEAR MOSFET

<table>
<thead>
<tr>
<th></th>
<th>linear J0.7</th>
<th>O_J0.9</th>
<th>O_J1.1</th>
<th>O_J1.3</th>
<th>O_J1.5</th>
<th>O_J1.1_C</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH. density [µm²]</td>
<td>0.357</td>
<td>0.258</td>
<td>0.259</td>
<td>0.258</td>
<td>0.256</td>
<td>0.377</td>
</tr>
<tr>
<td>JFET density</td>
<td>0.250</td>
<td>0.075</td>
<td>0.098</td>
<td>0.121</td>
<td>0.144</td>
<td>0.143</td>
</tr>
<tr>
<td>BV [V]</td>
<td>1628</td>
<td>1639</td>
<td>1605</td>
<td>1630</td>
<td>1607</td>
<td>16</td>
</tr>
<tr>
<td>Vth [V]</td>
<td>1.96</td>
<td>2.04</td>
<td>2.02</td>
<td>2.06</td>
<td>2.12</td>
<td></td>
</tr>
<tr>
<td>*R_{on,sp} [mΩ-cm²]</td>
<td>5.61</td>
<td>25.52</td>
<td>12.82</td>
<td>9.72</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{gd,sp} [pF/cm²]</td>
<td>106</td>
<td>21</td>
<td>28</td>
<td></td>
<td>34</td>
<td></td>
</tr>
<tr>
<td>Q_{gd,sp} [nC/cm²]</td>
<td>311</td>
<td>67</td>
<td></td>
<td>93</td>
<td>144</td>
<td></td>
</tr>
<tr>
<td>FOM (R_{on}×C_{gd}) [mΩ-pF]</td>
<td>595</td>
<td></td>
<td>603</td>
<td>288</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FOM (R_{on}×Q_{gd}) [mΩ-nC]</td>
<td>595</td>
<td></td>
<td>1555</td>
<td>1953</td>
<td>1220</td>
<td></td>
</tr>
</tbody>
</table>

* includes R_{sub} (~0.7 mΩ-cm²)

---

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BiDFET: Monolithic Bi-Directional FET

Cycloconverters or matrix converters require power devices with bi-directional voltage blocking and current conduction capability.

- A Matrix Converter creates a variable output voltage with unrestricted frequency using an array of fully-controlled four-quadrant bidirectional switches as the main power elements.
- It does not need any large energy storage elements and DC-link circuit.
- “Unfortunately, there were no such devices available.”
- “Consequently, multiple discrete devices had to be used to construct suitable switch cells.”

Proposed SiC Bi-Directional FET – BiDFET

New Monolithic 4-Terminal BiDFET Device

SiC Power JBSFET - 1

SiC Power JBSFET - 2

**SiC Power JBSFET Structure:**
Power MOSFET with Integrated Schottky (JBS) Anti-Parallel Diode
**BiDFET: Experimental Results**

*New BiDFET Device*

**SiC Power JBSFET - 1**

**Operation in First Quadrant**

- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- JBSFET-1 Blocks Voltage if \( V(G1-T1) = 0 \)
- Blocking Voltage = 1650 V
- Low leakage current in spite of Schottky Contact


---

**SiC Power JBSFET - 2**

Similar Characteristics in Third Quadrant
BiDFET: Experimental Results

SiC Power JBSFET - 1

Operation in First Quadrant

- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- Gate Bias for JBSFET-2: $V(G2-T2) = 25$ V
- Current flows through channel within JBSFET-2
- Gate Bias for JBSFET-1 Varied (5 V steps to 25 V)
- On-state Resistance = 0.5 $\Omega$ – Can be reduced with larger active area.
- Current Saturation with good Safe-Operating-Area

SiC Power JBSFET - 2

Similar Characteristics in Third Quadrant
BiDFET: Experimental Results

Operation in First Quadrant

- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- Gate Bias for JBSFET-2: \( V(G2-T2) = 0 \) V
- Current flows through JBS Diode within JBSFET-2
- Gate Bias for JBSFET-1 Varied (2 V steps to 26 V)
- Knee is observed at 1.5 V in output characteristics.
- Current Saturation with good Safe-Operating-Area
BiDFET: Comparison with Prior Art

<table>
<thead>
<tr>
<th>AC Switch Option</th>
<th>Number of Devices &amp; Packages per Leg</th>
<th>On-State Voltage Drop</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si Devices</td>
<td>Case (a)</td>
<td>5</td>
</tr>
<tr>
<td>Si Devices</td>
<td>Case (b)</td>
<td>4</td>
</tr>
<tr>
<td>Si Devices</td>
<td>Case (c)</td>
<td>2</td>
</tr>
<tr>
<td>SiC Devices</td>
<td>Case (d)</td>
<td>4</td>
</tr>
<tr>
<td>SiC Devices</td>
<td>Case (e)</td>
<td>4</td>
</tr>
<tr>
<td>SiC BiDFET</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

- **Assumptions:**
  - Si Diode On-State Voltage Drop = 1.5 V
  - Si Asymmetric IGBT On-State Voltage Drop = 2.0 V
  - Si Symmetric (RB) IGBT On-State Voltage Drop = 2.5 V
  - SiC Diode On-State Voltage Drop = 1.5 V
  - SiC MOSFET On-State Voltage Drop = 0.25 V
BiDFET: Monolithic Bi-Directional FET

- A Novel Monolithic 4-Terminal Bi-Directional Field Effect Transistor (BiDFET) based up on SiC Technology has been proposed and demonstrated for application to Matrix Converters.
- The key attributes of the device are:
  - High blocking voltage in first and third quadrants
  - Current conduction in first and third quadrants with low on-resistance
  - Current saturation with gate bias control in first and third quadrants
  - Fast switching capability of SiC power MOSFETs
  - Large SOA with ruggedness of SiC power MOSFETs
- Advantages when compared with previous approaches:
  - Single device
  - Only one package
  - Low on-state resistance and voltage drop
  - Can be Manufactured in a single integrated circuit foundry

The authors wish to acknowledge the support of the PowerAmerica Institute. This work was supported by the Department of Energy Advanced Manufacturing Office under Cooperative Agreement DE-EE0006521.

Conclusion

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