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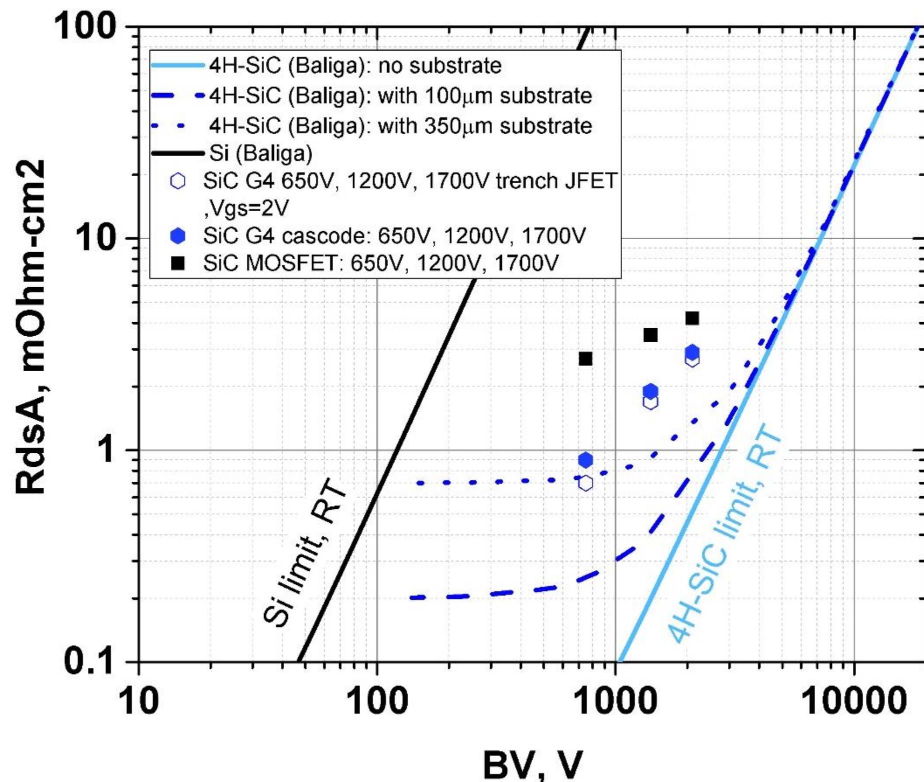
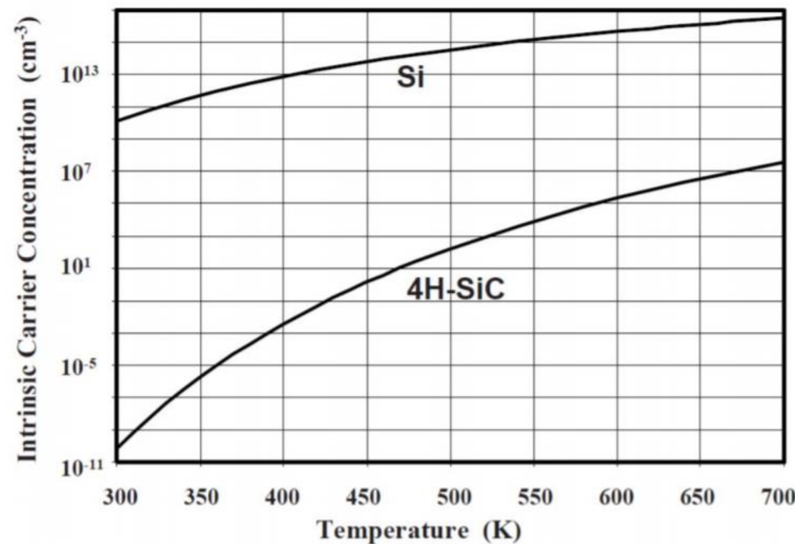
SiC JFETs for Circuit Protection

Why SiC?

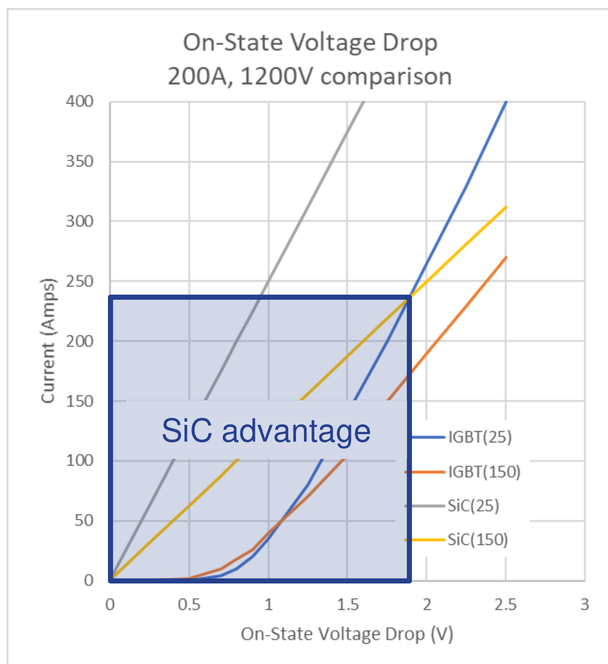


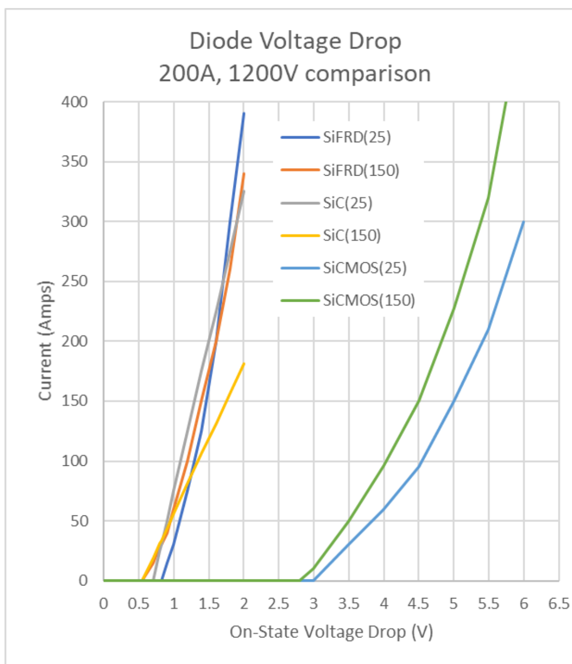


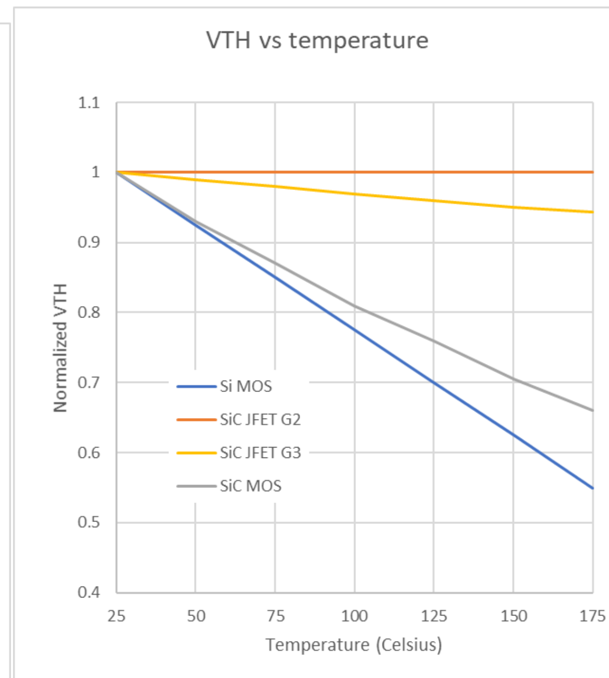
Key properties

- Low RdsA for a given BV for unipolar devices, due to 10X higher E_{CRIT}
- High peak operating temperatures
- 3X Higher thermal conductivity than Si
- Ability to handle 4X energy to failure than Si per unit area

SiC FET Advantages ≥ 1200V







- Normally-on SiC JFETs offer lowest RdsA
- IGBTs – great at high currents, but knee voltage leads to unwanted losses in most operating conditions
- Normally-off FET created using stack cascode, Si MOSFET on SiC JFET
  - Si MOSFET adds Rds, but operates at a positive Vgs
  - Excellent reverse conduction characteristic, similar to Si diode
  - No gate oxide degradation issues
- Normally-on JFET Vth is insensitive to temperature – more thermally stable

1200V SiC Stack Cascode Example

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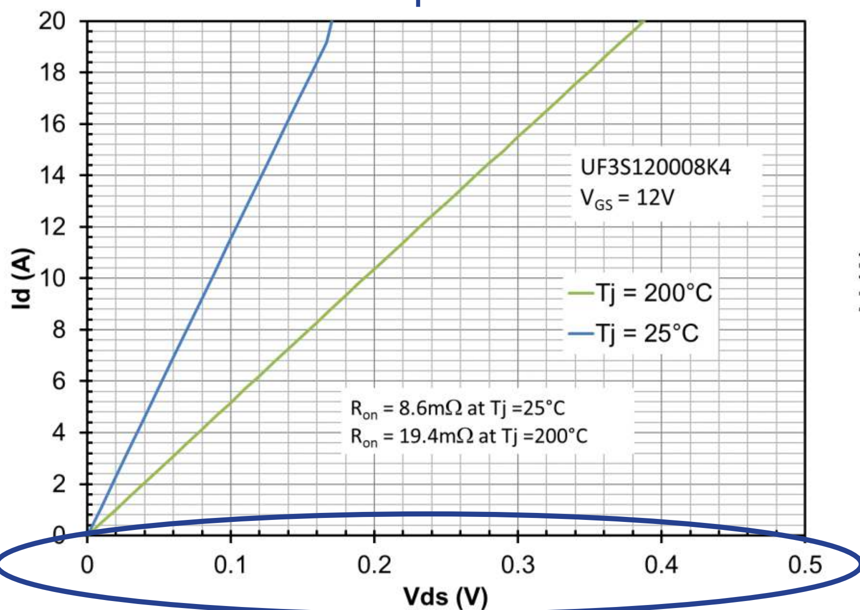
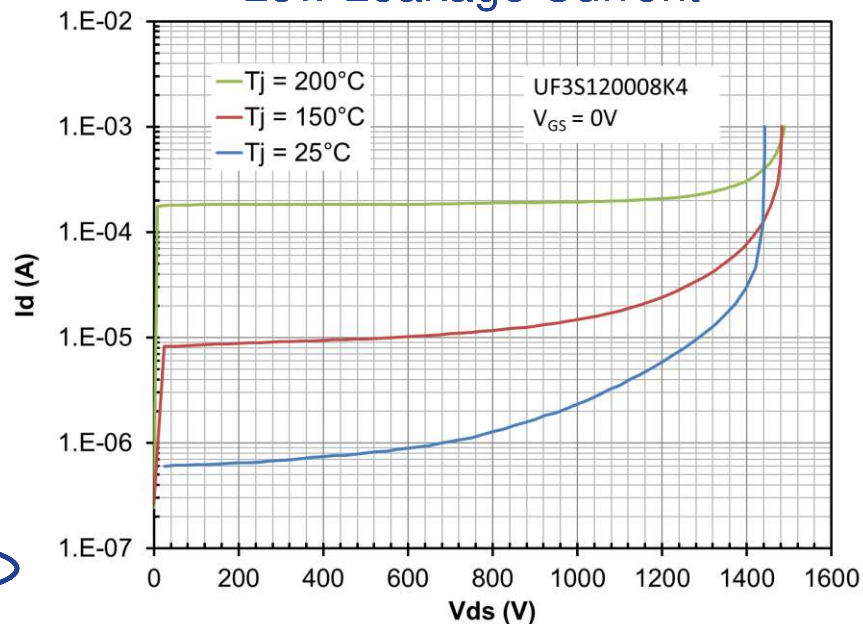
Excellent Output Characteristic

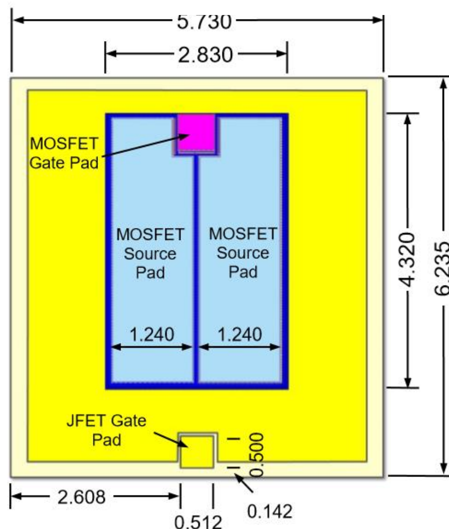


No knee voltage

Low Leakage Current



8mΩ, 1200V Gen3 FET using stack cascode die



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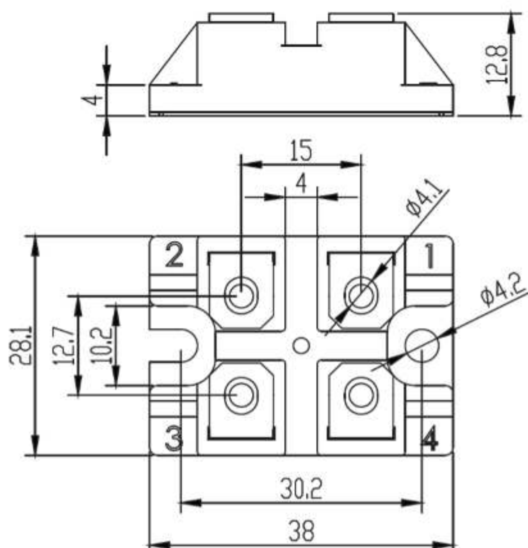
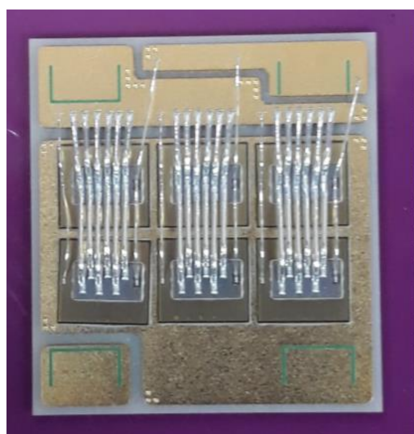
2mΩ, 1200V SOT-227 SiC FET

NSF



Unit: mm

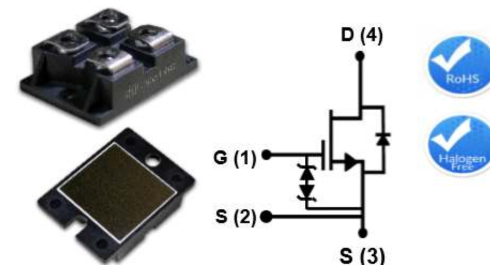


xJ SiC Series | 1.8mΩ - 1200V SiC Cascode | UF3SC120002SNS

Datasheet

Description

United Silicon Carbide's cascode products co-package its high-performance F3 SiC fast JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This device is ideally suited for circuit breaker, solid state switch and synchronous rectification applications, using a standard gate drive, and providing very high current capability in the familiar SOT227 footprint. The baseplateless construction with advanced internal packaging provides very low thermal impedence.



Part Number	Package	Marking
UF3SC120002SNS	SOT-227	UF3SC120002SNS

Features

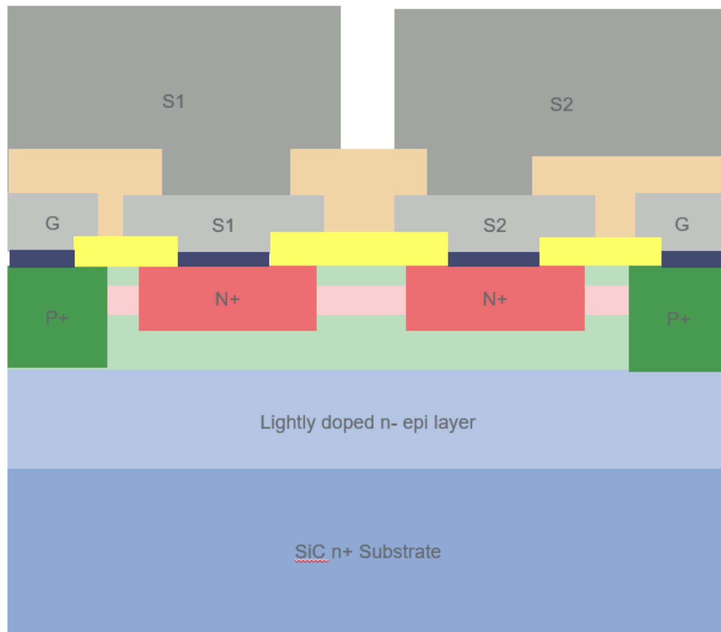
- Typical on-resistance $R_{DS(on,typ}$ of 1.8mΩ
- Standard 12V gate drive
- Maximum operating temperature of 175°C
- Excellent Reverse Recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected, HBM class 2
- SOT227 package for high current handling

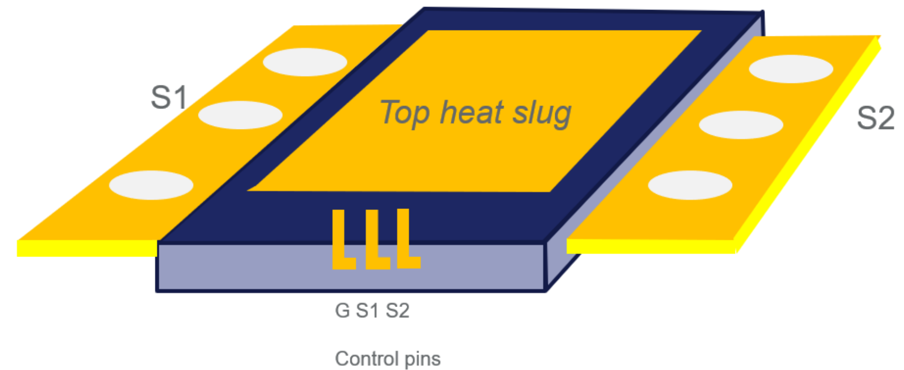
Typical Applications

- EV charging
- Synchronous rectifiers
- Solid state circuit breakers
- Solid state load switch
- Motor drives
- Induction heating

- *AlN for improved RthJC*
- *Ag sinter interfaces*
- *Au plated bottom*
- *Package can be sintered to heat sink*

Lateral SiC JFET for 28V Breakers





- *For very low voltages and bidirectional circuit breakers, this lateral structure eliminates substrate resistance*
- *With state-of-the-art packaging, 1mΩ, 100V 3x6mm^2 chips can be paralleled to form high current breakers with resistances < 0.1mΩ*

Active Mode Stable Operation

UnitedSiC G2 Normally-on JFET

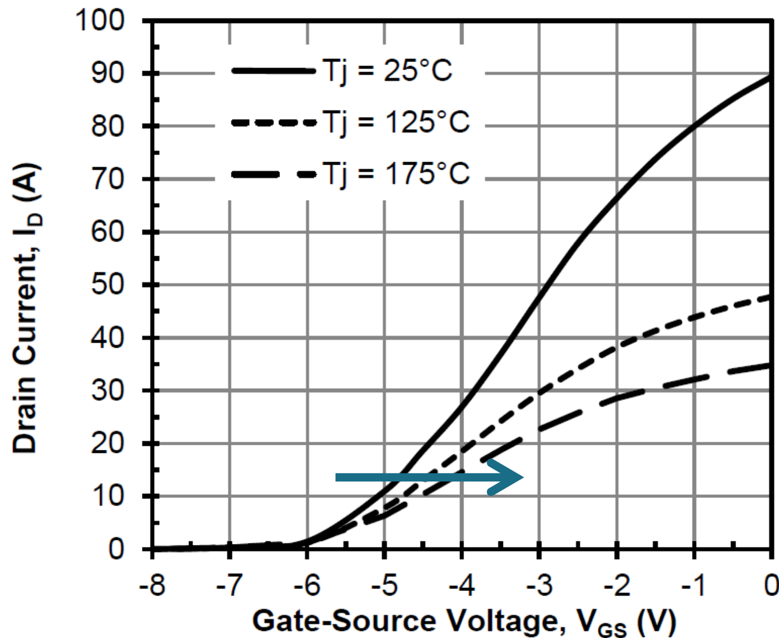


Figure 6 Typical transfer characteristics at V_{DS} = 5V

Typical SiC MOSFET

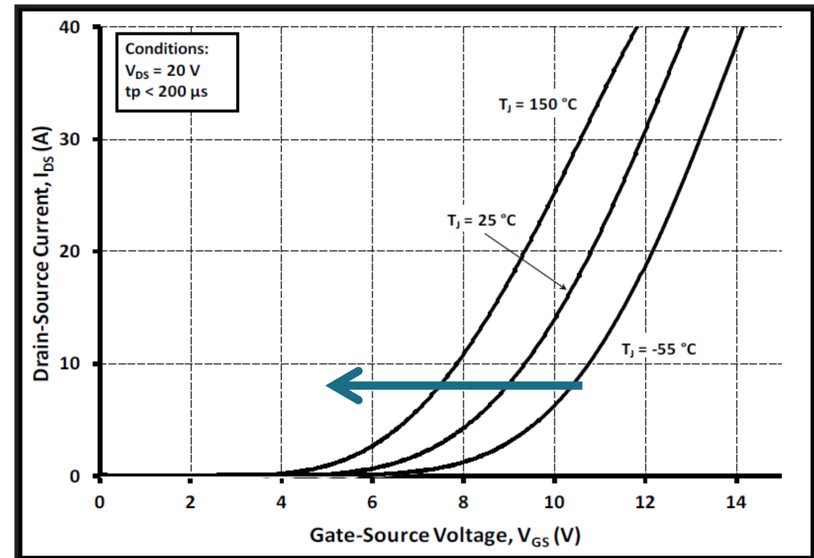
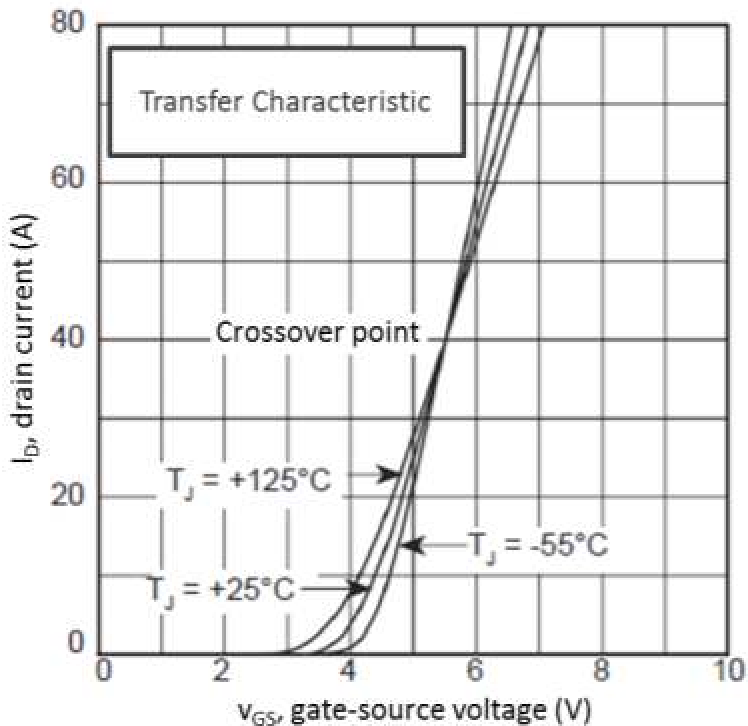
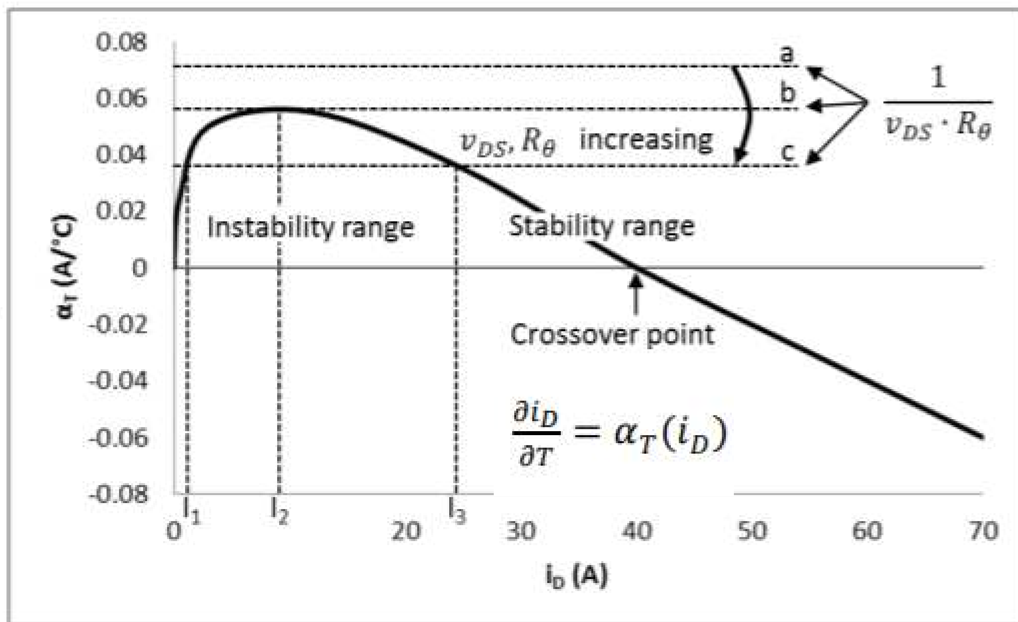


Figure 7. Transfer Characteristic for Various Junction Temperatures

Unlike SiC or Si MOSFETs, JFETs can be held stably in active mode, since the V_{GS} needed to sustain a given current increases with temperature, even down to relatively low currents

MOSFET Hot Spot in Active Mode





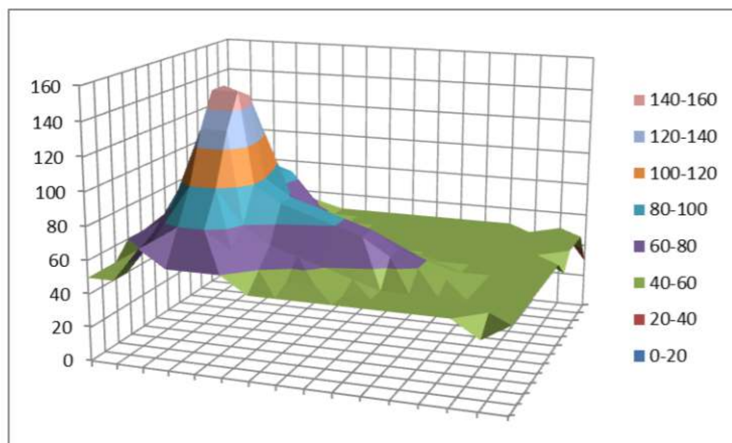


Figure 2 Representation of 5x5 mm power MOS temperature distribution (°C) in [1] clearly showing hot spot phenomenon

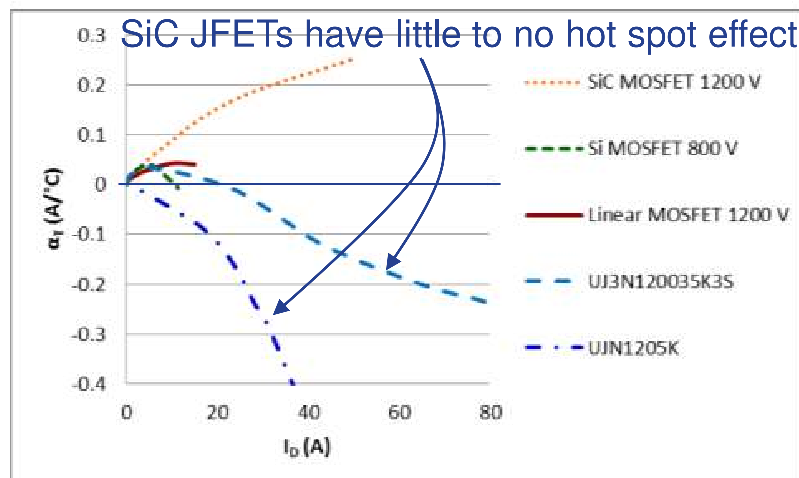
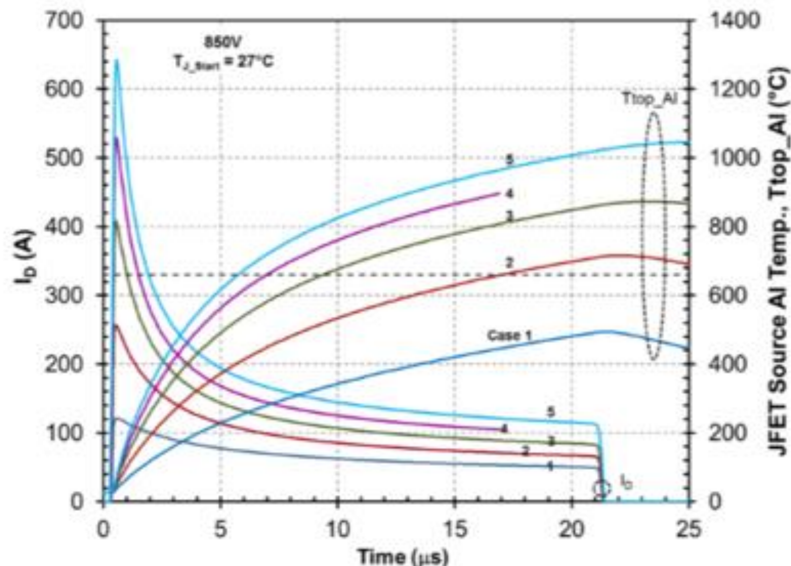
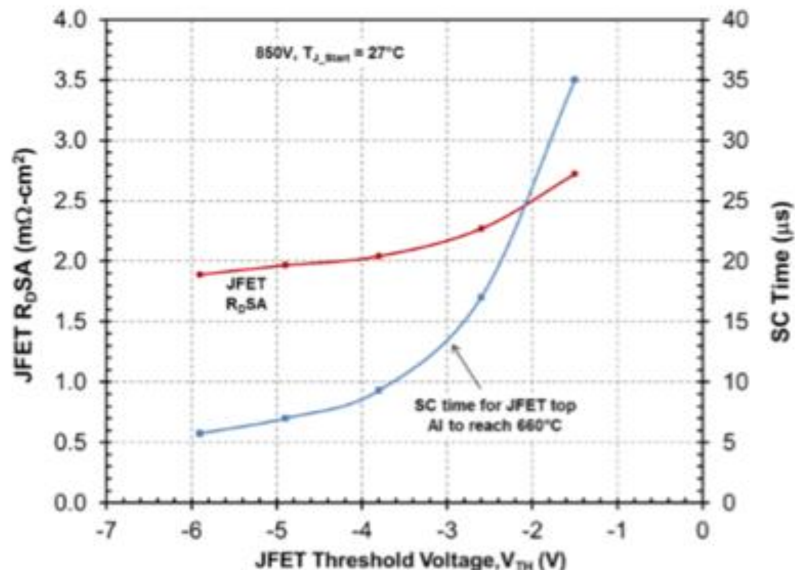


Figure 5 $\alpha_T(i_D)$ versus drain current for various device types

SiC JFET/Cascode Short Circuit





- *RdsA tradeoff for trench SiC JFETs (UJC1206K)*
- *Peak saturation current can be decreased with little Rdson penalty*

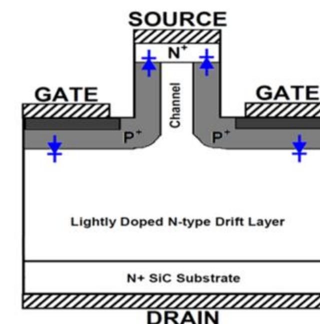
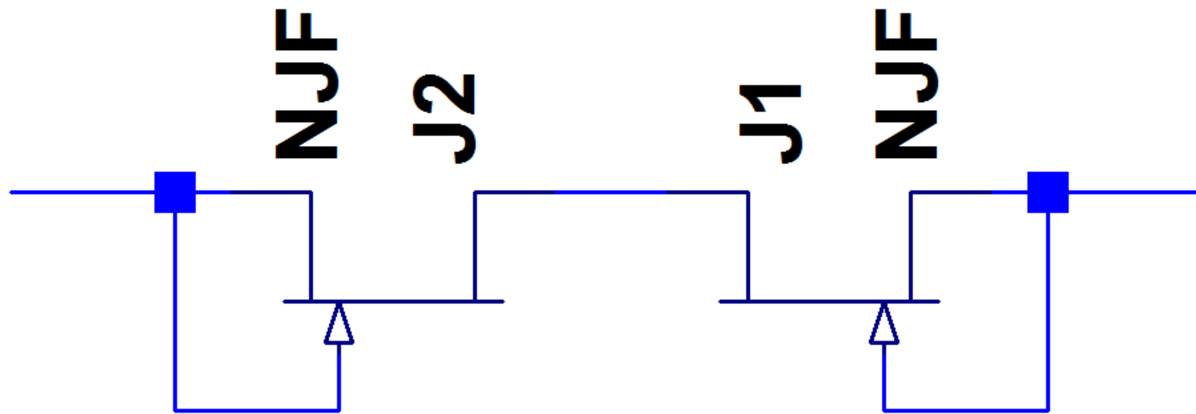
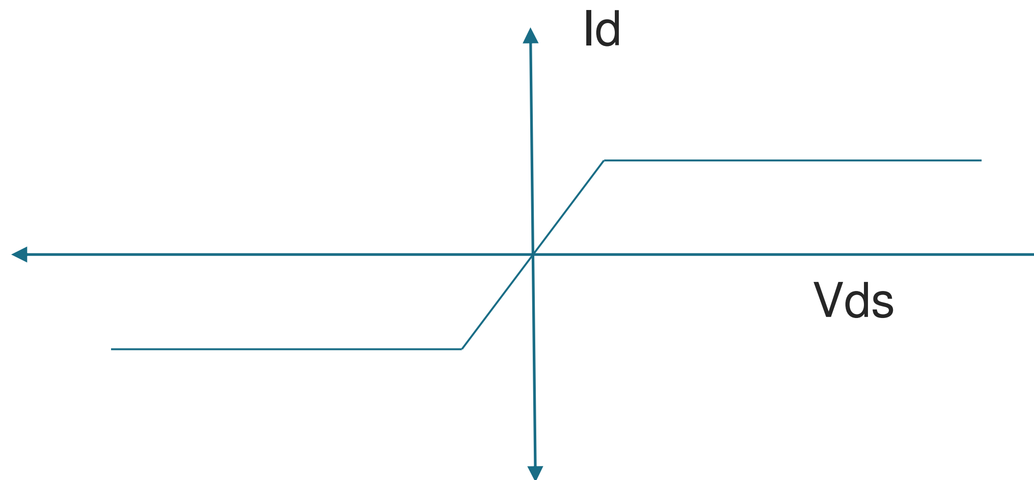


Figure 1: Cell structure of SiC trench JFET.

Intrinsic Current Limiting Function





Setup for Electrothermal Simulations

Surge waveform WF5A
Vpeak (open circuit voltage) = 1500V
Source impedance = 1 Ω

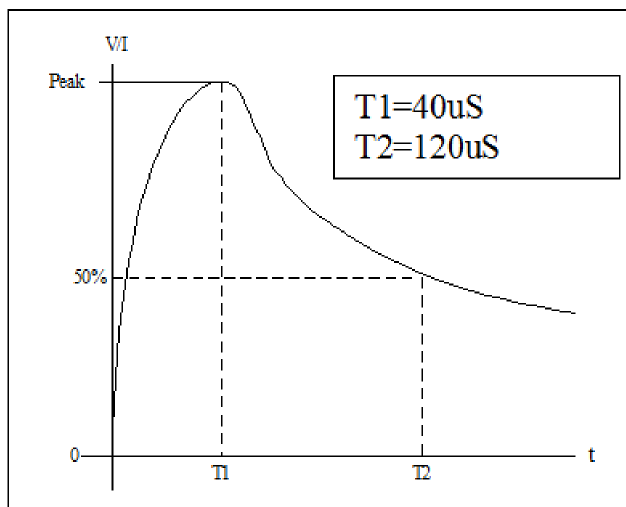
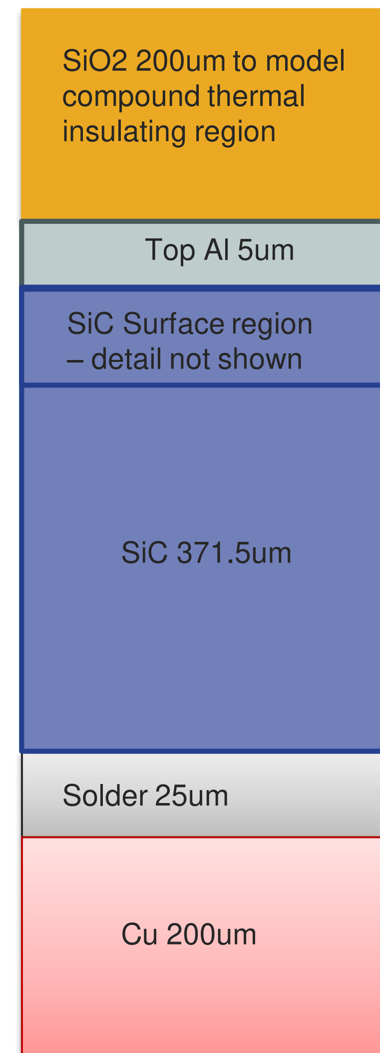
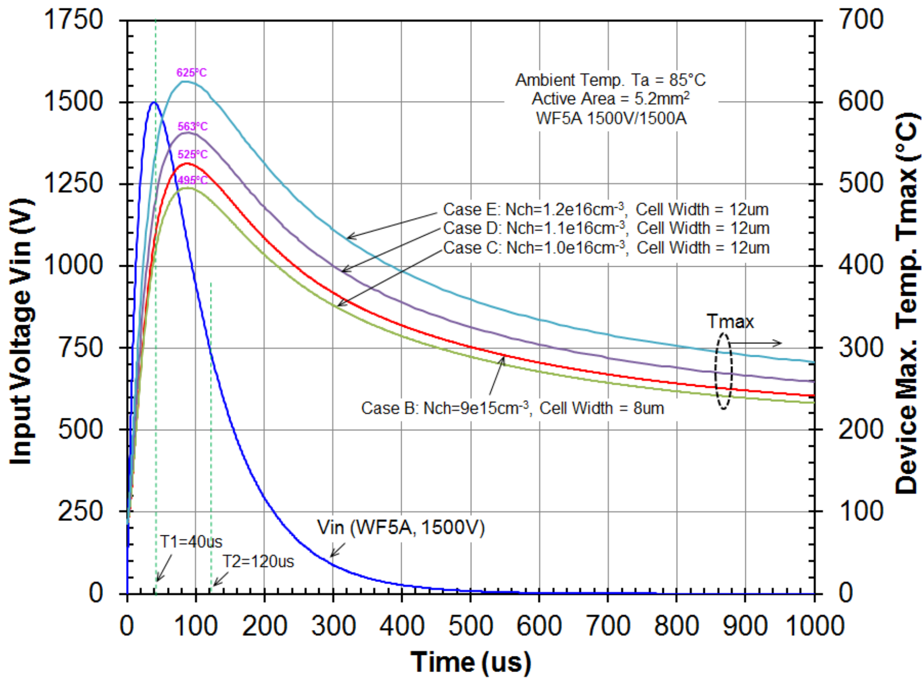


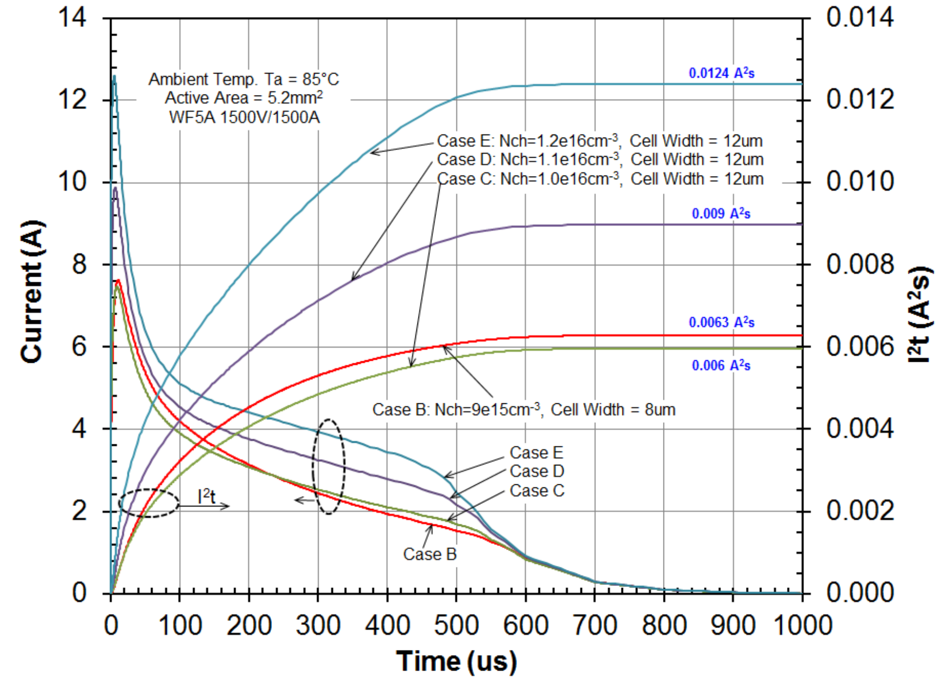
Figure 2 Example Surge Waveform (WF5A)

Layer (From top to bottom)	Thickness um	Thermal Conductivity W/(K cm)	Heat Capacity J/(K cm^3)
SiO2 (Pkg mold)	200	0.014	1.67
Aluminum	5	2.38	2.33
SiC	371.5	4.55	1.63
Solder	25	0.36	1.57
Copper (baseplate)	200	3.85	3.42



Transient Thermal Simulations WF5A 1500V/1500A





Recommended Design

Design	Ron (Ω)	Isat @85°C (A) @10V	Isat @85°C (A) @1.5kV	Tmax (°C)	Imax (A)	I^2t (A^2s)	
Case B	0.58	2.5	12.3	525	7.6	0.0063	8um pitch
Case C		3.2	11.5	495	7.5	0.0060	12um pitch
Case D	0.45	5.2	15.6	563	9.8	0.0090	
Case E	0.39	7.4	19.9	625	12.6	0.0124	

Temperature Distribution along Device Vertical Center Line for Design Case D

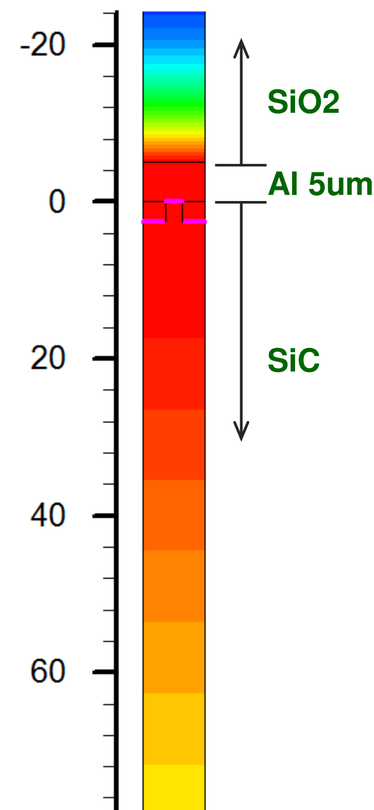
SiO2 200um | Al 5um | SiC 371.5um | Solder 60/40 25um | Copper 200um

X=2um (Cell center line)
Nch=1.1e16cm^{-3}
Cell Width = 12um
Active Area = 5.2mm^2
Ambient Temp. Ta = 85°C
WF5A 1500V/1500A

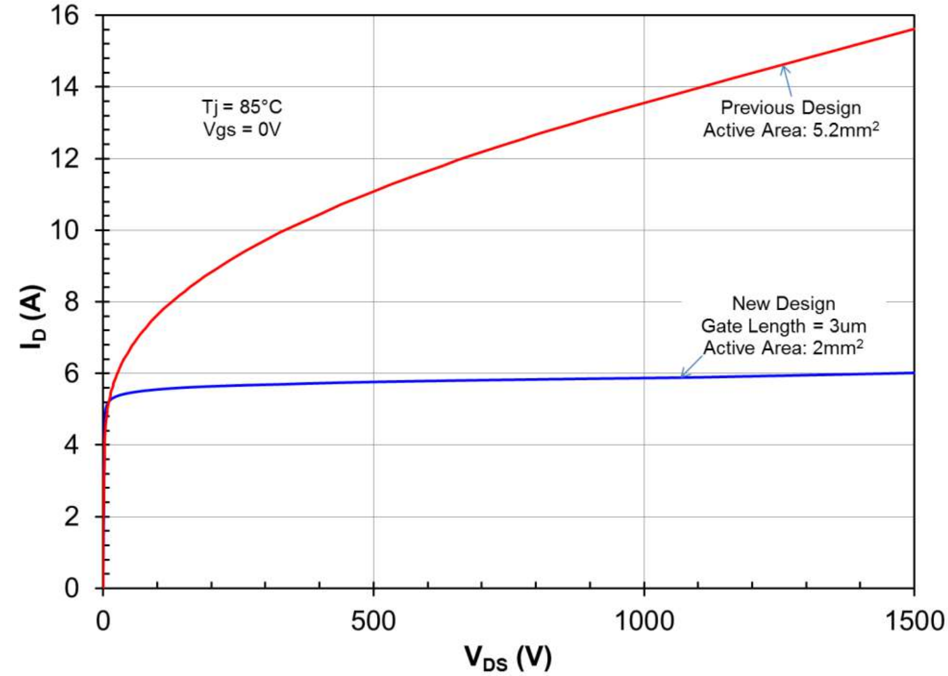
10us 20us 30us 40us 100us 150us 200us 300us 500us 1000us

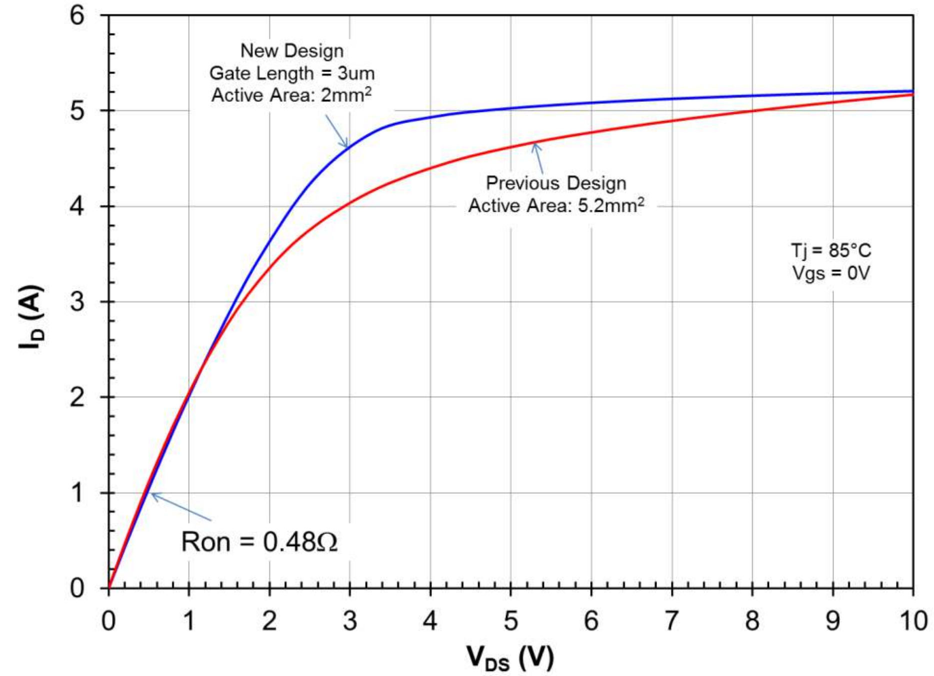
Temperature (°C): 0, 100, 200, 300, 400, 500, 600

Distance Y (um): -200, -100, 0, 100, 200, 300, 400, 500, 600



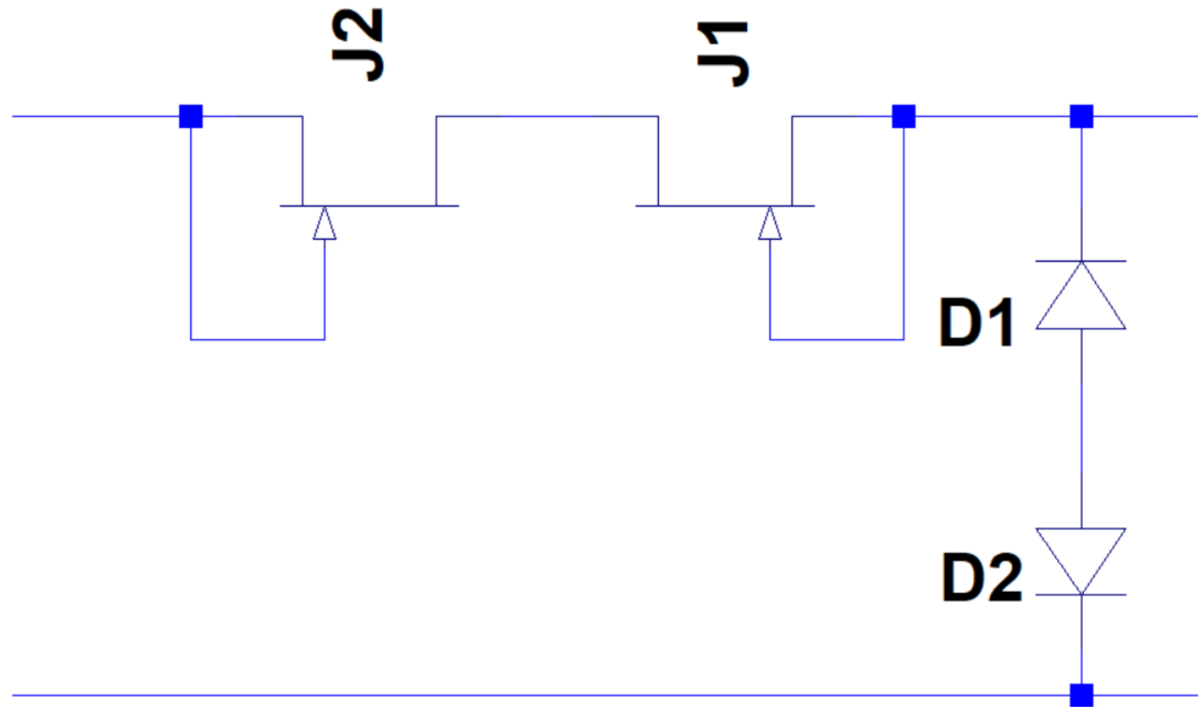
Improved Current limiter DC Characteristics at 85°C





Avoid DIBL type effects for better saturation

Inrush and Overvoltage Protection



Common-drain JFETs – bidirectional inrush current limiting

D1,D2 – TVS diodes. Use Si at low voltages, SiC at high voltage

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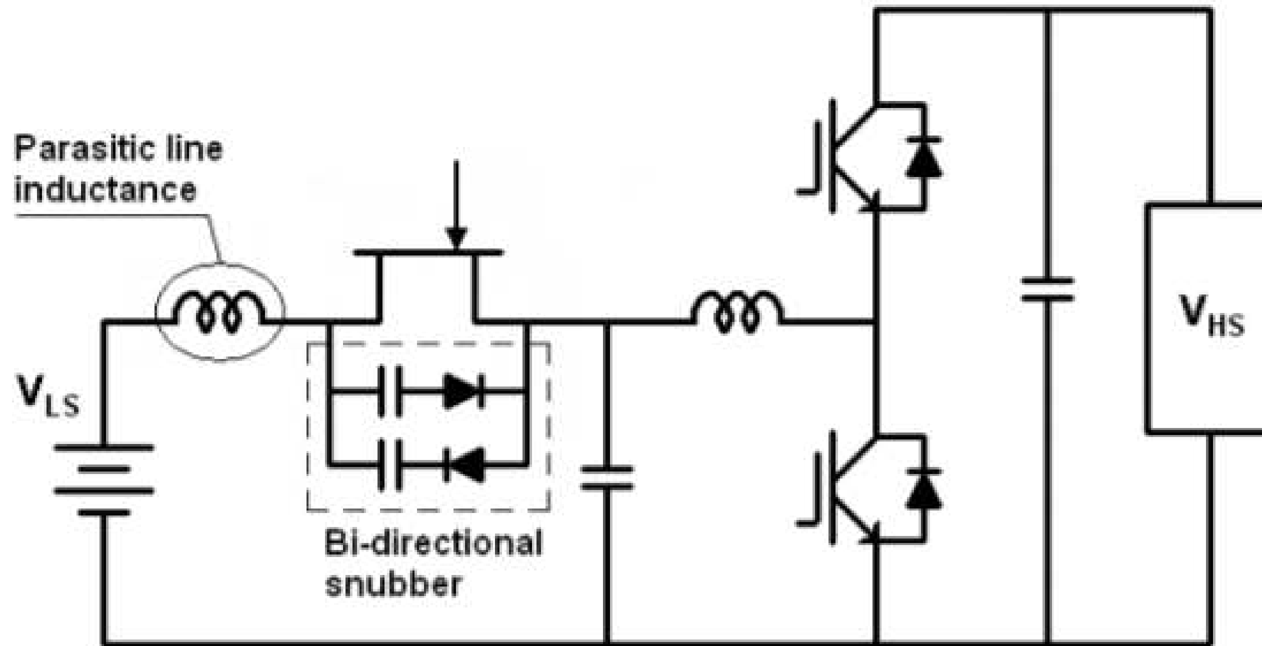
High Speed DC Breaker Example



A MOV may be used across the SD if the line inductance energy becomes too high.

High Speed DC Breaker Example

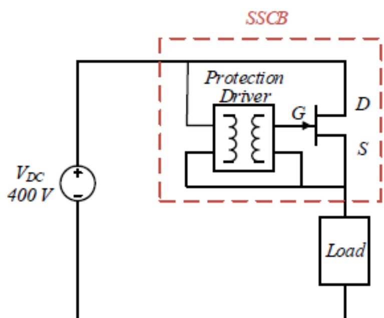


Fig. 1. A unidirectional self-powered SSCB using a normally-on SiC JFET as the main static switch and a fast-starting isolated DC/DC converter as the protection driver.

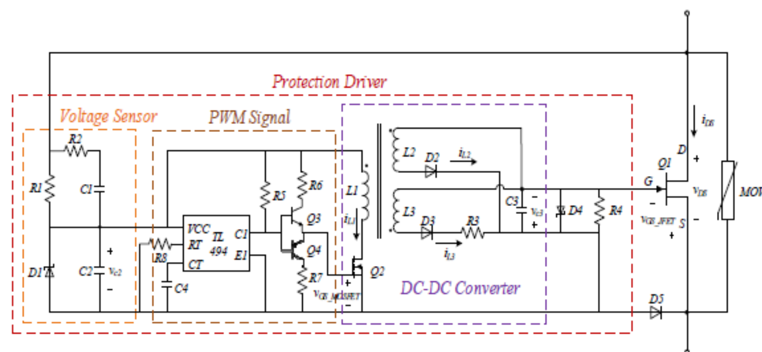


Fig. 2. A detailed circuit schematic of the SSCB with a combined forward-flyback DC/DC converter design.

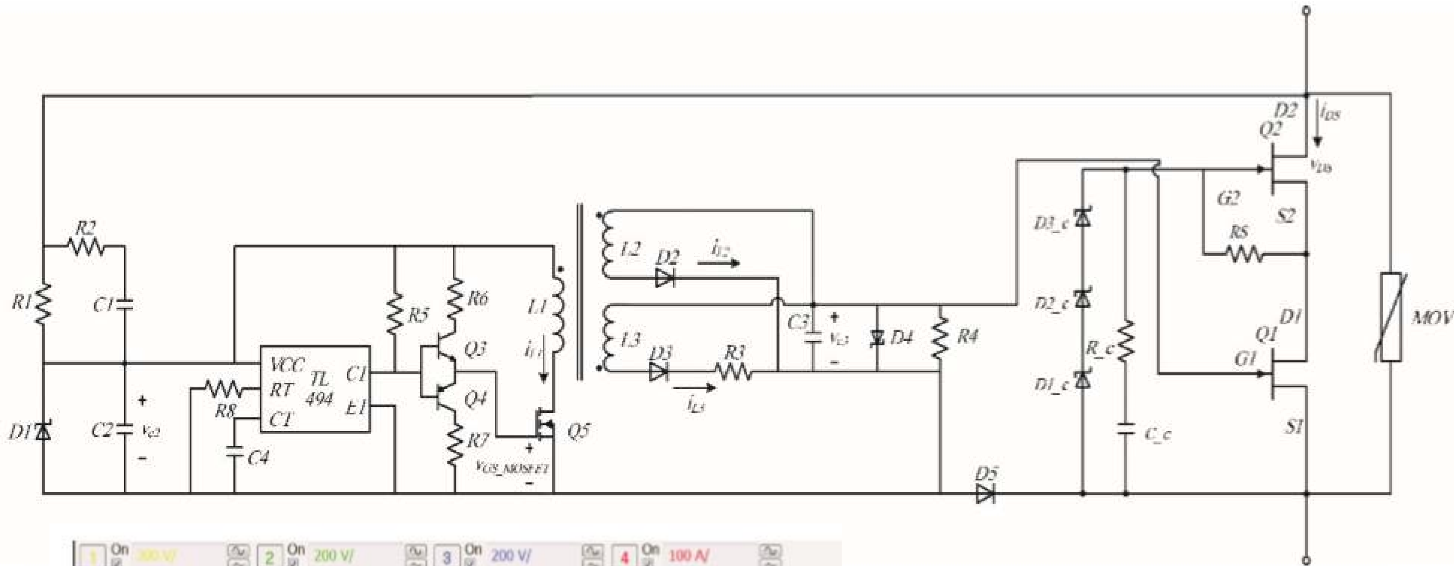
(a)

(b)

Fig. 9. Short circuit switching waveforms of SSCB with a combined forward-flyback protection driver with (a) 1 Ω, and (b) 2 Ω short circuit loop resistance. Time scale: 1 µs/division. BLUE is the JFET drain current i_{DS} waveform (100A/division). YELLOW is the JFET drain-source voltage v_{DS} waveform (200V/division). RED is the SiC JFET gate voltage v_{GS_JFET} waveform (10V/division). The response time is about 0.8 µs and 1 µs for (a) and (b) respectively.

Courtesy of the Illinois Institute of Technology

Multi-Stage JFET Based Breaker



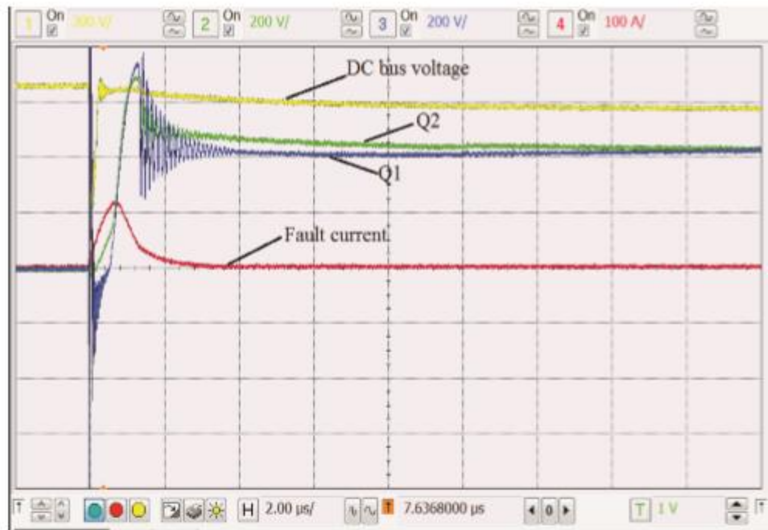
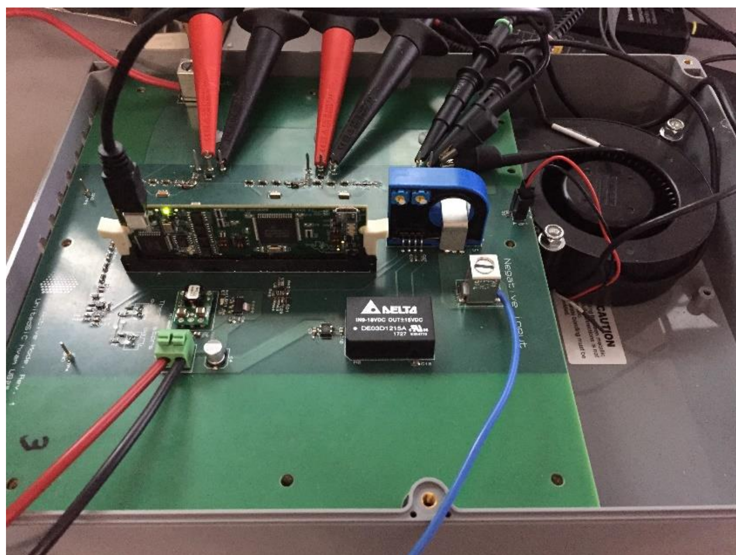


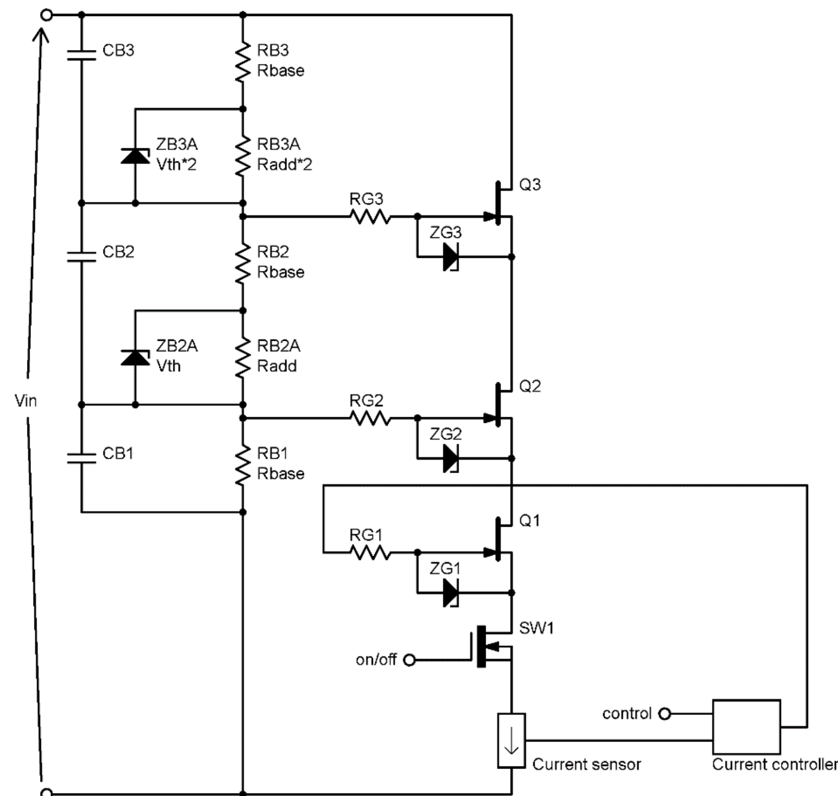
Fig. 7. Measured V_{DS} switching waveforms of Q1 (blue) and Q2 (green) during a short circuit fault. Time scale: 2 μs/division.

Courtesy of the Illinois Institute of Technology

Controlled Current DC SSCB

- Voltages automatically balanced
- Current controlled at any operating voltage
  - Soft start
  - Capacitor precharge
  - Fault ride-through current limiter
- High voltage capability with fast turn-off feature

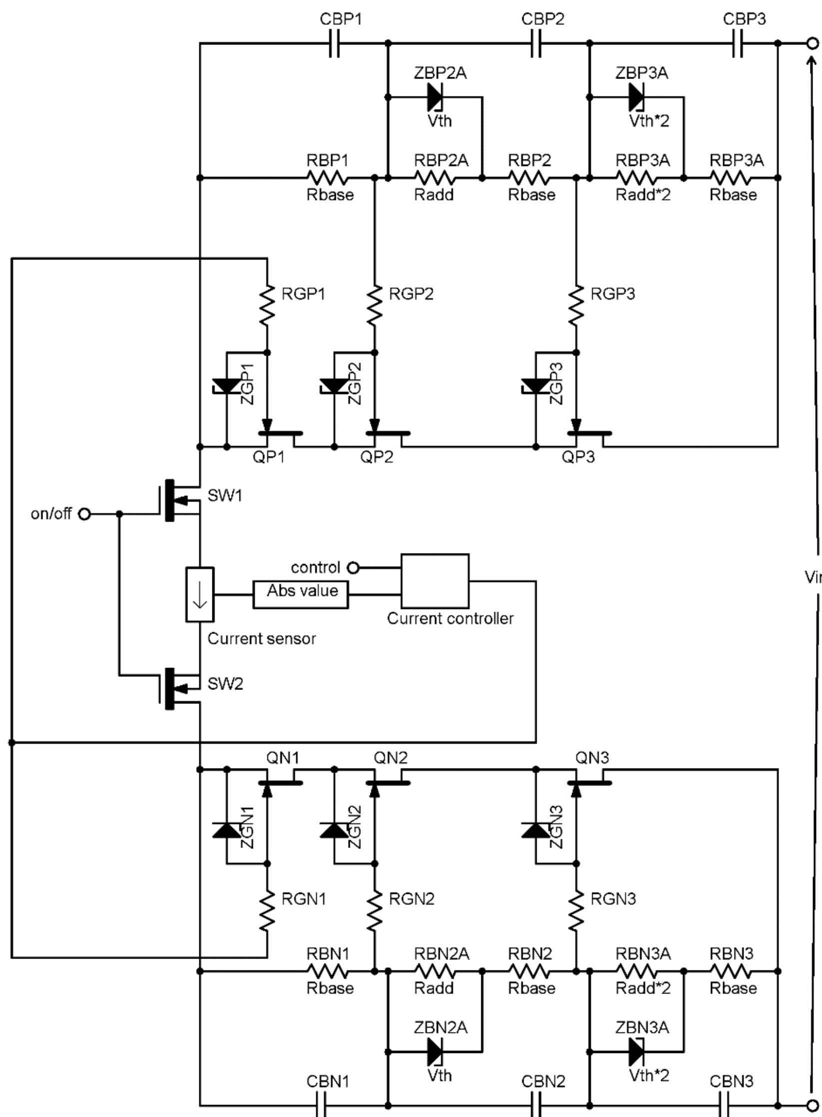




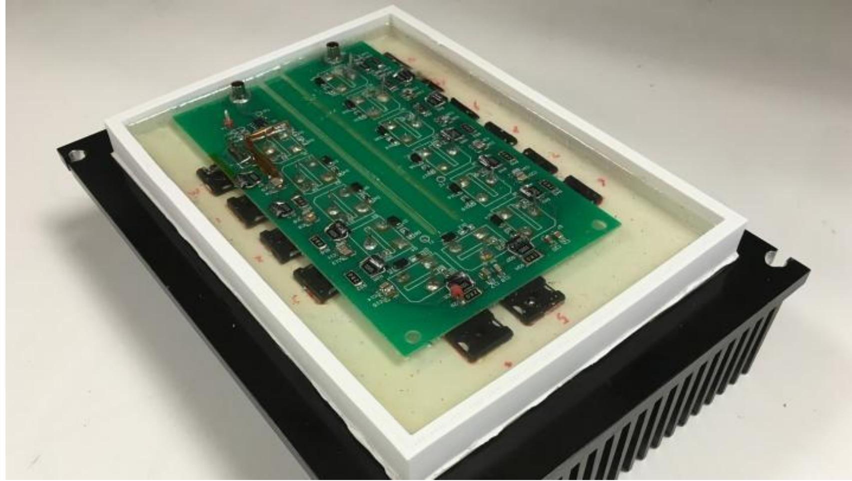
- Even if not operating at high voltage…
  - Multiple JFETs dissipating power
  - One current controller
  - Lower cost than paralleling

Controlled Current AC SSCB

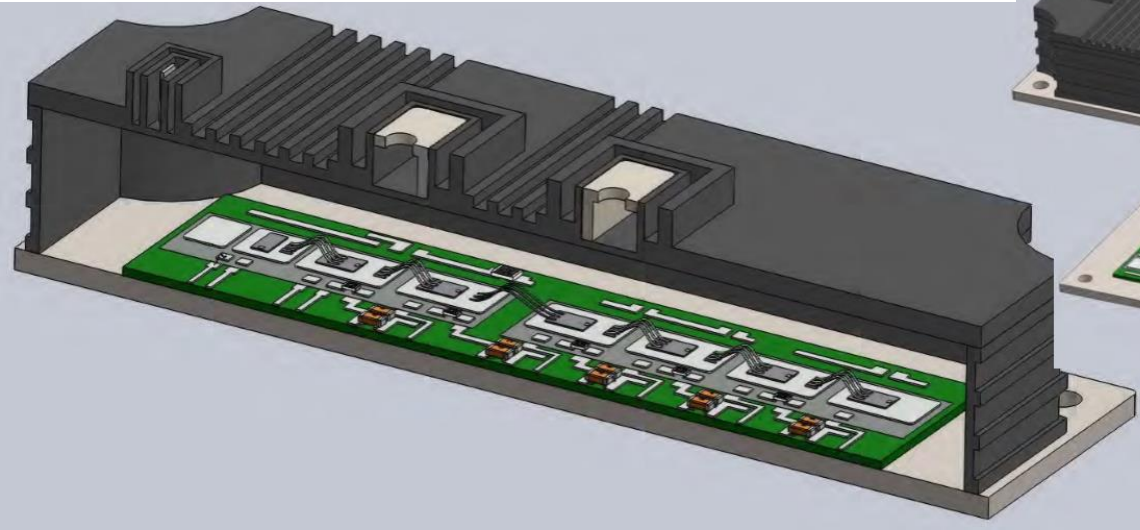
- AC current controlled with alternating voltage applied
  - Clean AC motor start
  - Fault ride-through current limiter
- Bidirectional blocking, fast turn-off feature
- JFETs in reverse conduction are biased fully on because JFET is on when $v_{GS} - v_{DS} > V_{GS(th)}$. When v_{DS} is negative, JFET turns on more with increasing magnitude of its v_{DS} (caused for example by increased current through it), thus creating a positive reinforcement of turning on.



FREEDM HV Supercascodes



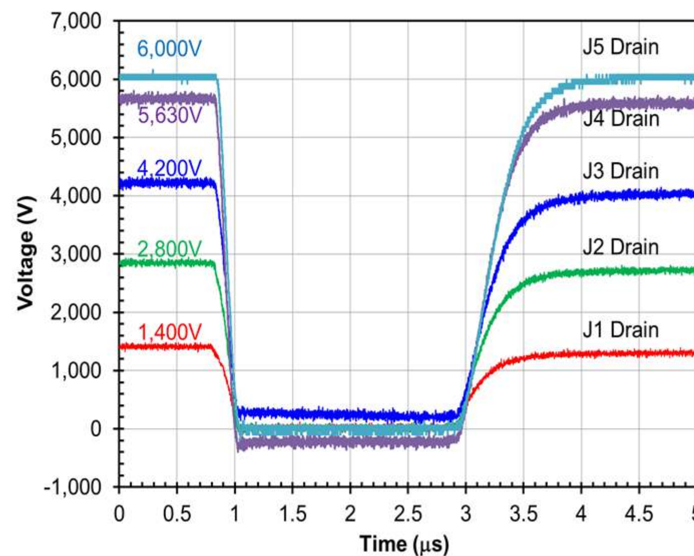
15KV, 40A built with discrete 45m, 1200v JFETs NCSU



100A, 6.5KV SCPM proposed by NCSU

High Voltage Applications

- *200A, 6500V half-bridge*
- *Solid state transformers, MV-XFC fast chargers, wind, traction, HVDC*
- *Uses a 5.7m, 1700V SiC JFET*
- *Can be utilized for HV DC breakers*



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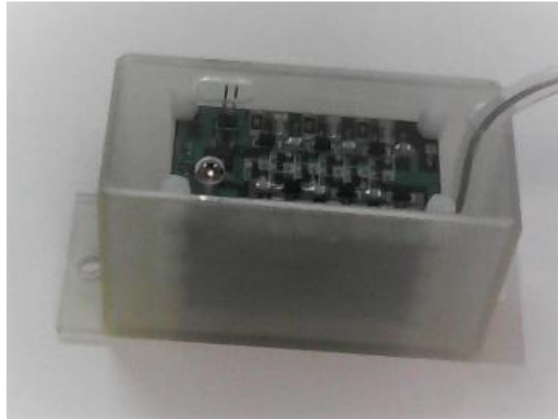
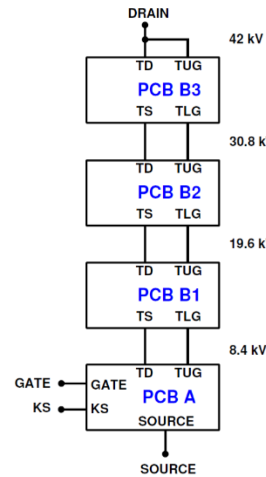
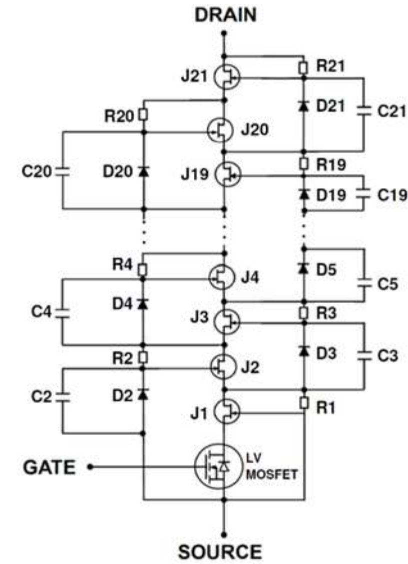
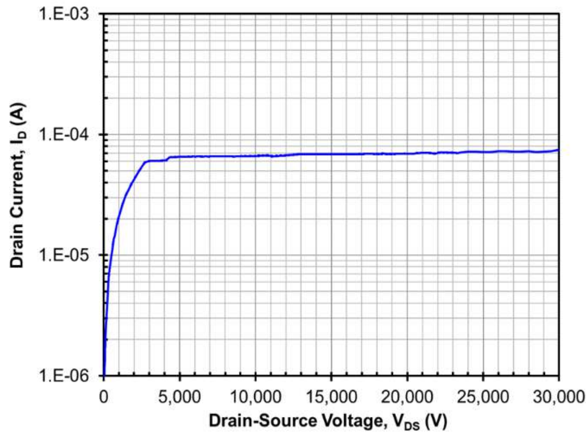
Ultra High Voltage Switches

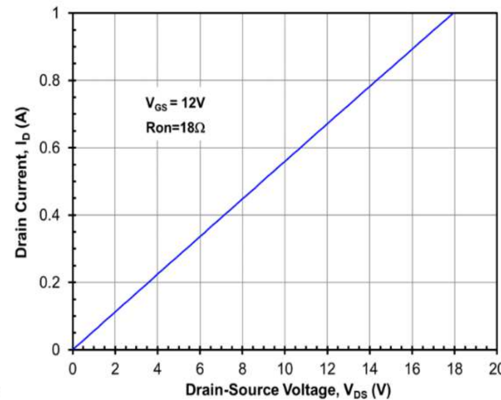


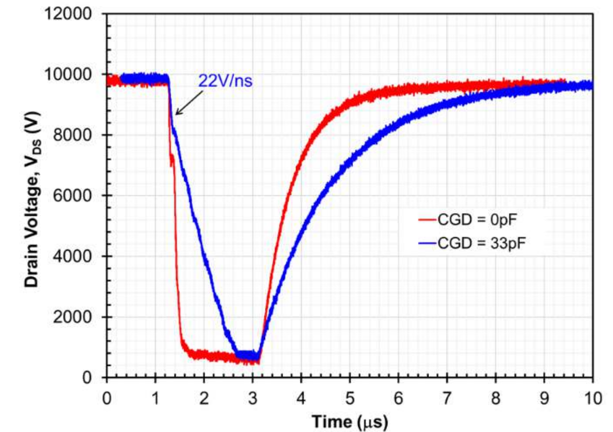
1A, 40KV Demo











Questions

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Table I: Physical characteristics of Si and main wide bandgap semiconductors [1-3].

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, Eg (eV)	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant, ε_r[1]	11.9	13.1	9.66	10.1	9	5.5
Electric Breakdown Field, E_c (kV/cm)	300	400	2500	2200	2000	10000
Electron Mobility, μ_n ($cm^2/V{\cdot}s$)	1500	8500	500 80	1000	1250	2200
Hole Mobility, μ_p ($cm^2/V{\cdot}s$)	600	400	101	115	850	850
Thermal Conductivity, λ (W/cm·K)	1.5	0.46	4.9	4.9	1.3	22
Saturated Electron Drift Velocity, v_{sat} ($\times 10^7$ cm/s)	1	1	2	2	2.2	2.7

[1] $\varepsilon = \varepsilon_r \cdot \varepsilon_0$ where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m