**New Resource for ERCD Ckt Topology Research**

Epoxy Resin Composite Dielectrics (ERCD)

ERCD “substrate-less” approaches identified for high voltage (5kV/120μm), high temperature (≤300°C) and high thermal impedance (10W/mK)
Today, power electronics has strong growth across a board range of power levels. This particularly applies to increases that improve lives versus enhancing entertainment.

However, increasing density and reducing cost still are the primary goals for all designs, and brings focus on Functional Integration at the Systems Level.

Problem? ... much smaller WBG devices

The challenge in thermal management will broaden to address essentially point-source heat generation due to higher power capabilities with shrinking die size ...compared to Si die.
Huang in 2004 developed three pertinent figures of merit [1].

HMFOM tracks the losses
\[ HMFOM = E_c \sqrt{\mu} \]

HCAFOM tracks the chip area.
\[ HCAFOM = E_c^2 \varepsilon \sqrt{\mu} \]

HTFOM tracks thermal conductance.
\[ HTFOM = \sigma_{th} / E_c \varepsilon \]

\( E_c \) is critical electric breakdown field,
\( \mu \) is electron mobility,
\( \varepsilon \) is dielectric constant,
\( \sigma_{th} \) is thermal conductivity

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Shrinking Die Size (so to speak)

- The FOM for GaN & SiC show substantial performance as die size can shrink, OR the power rating increases.
- Small die are preferred for higher and higher frequencies.

\( E_c^2 \varepsilon \) critical field
\( \mu \): mobility
\( \varepsilon \): dielectric constant
\( \sigma \): thermal conductivity

High Frequency Potential (e.g. Unipolar - MOSFET)

Since current does not scale, the speed ≈ 1/c, is significantly increased in WBG devices. Speed measured as di/dt or dv/dt

The reduction in size supports high frequency operation, but creates a greater challenge in heat dissipation and integration.


Comparison is based on hard switched converters with fixed I, V, and f. ZVS for high voltage provides other advantages for SiC.

Small Die for High Voltage – 9kV design in air

Packaging materials have always needed to passivate the chip for voltages greater than ~150V.

Small Die experiences breakdown at 1,800 V.
(Experimental design at NCSU)

A great emphasis to develop "Medium Voltage" power electronic systems is underway for large and small systems, e.g. portable x-ray equipment to large autonomous trucks.
The ‘Ground-Baseplate’ Problem in Packaging

It’s all about vertically conducting devices

Ground Coupling

Review of mid-point voltage…
However, there is a major current path when SW-Top turns on.
What is the problem?

\[ i = C \frac{dV}{dt} \]

Ex: \( V_t: 425 \, V_{dc} \), \( dt: 20\,ns \)
SiC MOSFET Chip Dimensions (used later also)

Ground Coupling (continued)

What current flows into 'ground' from the transistor drain?

Given:
FET: Minimum drain area of semiconductor and solder is 4.5mm X 4.5mm = 20.25mm²
+ bonding pad 2.5 X 2.5mm = 6.25mm²
+ circuit trace is 5mm X 10mm = 50mm²
Substrate:
Al₂O₃ (with εᵣ = 9.4) at 635μm thick

Find switching current:
Area, A = 20.25+6.25+50 = 76.5 mm²
Distance: d = 0.635 mm
Capacitance, C=εᵣε₀A / d = 10 pF
i = C (dV/dt ) = 10 pF (425/20ns)

i = 0.21 A
**Multi-die Modules**

Add diode and space: X2.2,  
Multiply by die in parallel: X8,  
(Add terminal footprint)  
Then,  
\[ i_T = 0.21 \times 2.2 \times 9 = 4.2\text{A@20ns} \]  
(For one side)

Standard packages add even more

---

**High Voltage Capacitive Current**

*Switching >10kV can occur at 125kV/µs*\(^1\)

For a generalized SiC die of 1cm X 1cm  
Use a 40mil (1.02mm) thick AlN ceramic  
\[ \varepsilon_f = 8.6, \quad \varepsilon_r = 8.85 \times 10^{-12} \text{ F/m} \]

The Capacitance,  
\[ C = \varepsilon_f \varepsilon_r A / d \]

\[ A = 10^{-4} \text{ m}^2, \quad d = 10^{-3} \text{m} \]

\[ :. \quad C = 7.6 \text{ pF, “per sq. cm”} \]

Find switching current at 10kV & 125 kV/µs:  
\[ i = C \left( \frac{dV}{dt} \right) = 7.6 \text{ pF} \text{ (125kV/µs)} \]

\[ i = 0.95 \text{A “per sq. cm”} \]

*For multiple dies and diodes use X19.8*  
*Or i = 18.8A*

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\(^{1}\) *Medium Voltage Power Switch Based on SiC JFETs Xueqin Li, Shirley Zhang, Peter Alexandrov, and Anup Bhalla,* IEEE-APEC 2015, Long Beach CA, Mar 21-25, 2016
# Thermal performance of metal clad ceramics

## $R_{th}$ [$^\circ$C/W] for 5mmX5mm SiC on 12/25/12 DBC

<table>
<thead>
<tr>
<th>Part</th>
<th>Width (mm)</th>
<th>Length (mm)</th>
<th>Thickness (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>5</td>
<td>5</td>
<td>0.36</td>
</tr>
<tr>
<td>Solder</td>
<td>5.1</td>
<td>5.1</td>
<td>0.05</td>
</tr>
<tr>
<td>Metal</td>
<td>5.7</td>
<td>5.7</td>
<td>0.3</td>
</tr>
<tr>
<td>Ceramic</td>
<td>6.97</td>
<td>6.97</td>
<td>0.635</td>
</tr>
<tr>
<td>Metal</td>
<td>7.57</td>
<td>7.57</td>
<td>0.3</td>
</tr>
<tr>
<td>Solder</td>
<td>7.67</td>
<td>7.67</td>
<td>0.05</td>
</tr>
<tr>
<td>AlSiC</td>
<td>13.67</td>
<td>13.67</td>
<td>3</td>
</tr>
</tbody>
</table>

**COMSOL Value**
- Heat Flux (W) 100
- Bottom Plate Temperature 293 K
- Mesh Fine
New thin dielectrics for Low Cost modules

Ceramics?

Flexible-Ceramic Power Electronics Packaging

NEEDS ADDRESSED
High Density, Fast Response, Low Voltage, System-in-Package Power Converters
- Need Inexpensive converters with good thermal management
- Operate Temp ≤85°C (similar to PCB)
- Suitable for high current GaN
  - and wearable power electronics

TECHNOLOGY
- Thin E-Strate flexible 3YSZ ceramic for:
  - High volume roll-to-roll manufacturing
  - High thermal management for highly dense LV power converters
- Thin 20 & 40 micron substrates for low thermal resistance
- Licensed from Corning

The 3YSZ Suitable for wearable electronics (<100°C, <100V) applications
New Thin Organic Dielectrics for Low Cost Modules

Epoxy Resin Composite Dielectrics – ERCDs
These provide and opportunity to look at very low cost modules with embedded components.

“Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao1, Yifan Jiang1, Bo Gao1, Kenji Nishiguchi2, Yoshi Fukawa3, D. C. Hopkins1
1North Carolina State University, 2Risho Kogyo Co., LTD, 3TOYOTech LLC

State-of-art development of WBG power module

SiC Module w/ double-sided cooling by ORNL [1]
- 2.6 nH extracted parasitics inductance
- Bus up to 600V with >40A capability
- Kelvin connections implemented
- Gate bonding wire required

SKIN and Direct Pressed Die technology by Semikron [2]
- >20% thermal resistance reduction
- 10% reduction in parasitic inductance
- >25% improvement in surge current
- Improved thermal-cycling based reliability
- 1700V/1800A
- Challenge on the Press Unit design and implementation

**State-of-art development of WBG power module**

- Lower Parasitics between high- and low-side switches
- Improved Power Efficiency
- Better Thermal performance
- Applicable for lower voltage applications for now

- Insulated-Metal-Baseplate based IPM by Mitsubishi [4, 5]
- CTE of insulating resin layer ~17ppm, close to Copper, with better mechanical stress management
- 35% thermal impedance reduction from development of resin
- Less interconnection layers for lower profile, up to 55% size reduction from traditional DBC based module
- Better thermal cycling reliability with less cracks during cycling
- Heavily depends on the resin interface material

**Criterion for thin dielectric selection for**

**Target Application:** 1200V / 40A SiC MOSFET and Schottky Diode based Power Module

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Conductivity</td>
<td>W/mK</td>
<td>&gt; 3</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>kV</td>
<td>&gt; 3</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>µA</td>
<td>~ 10</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td></td>
<td>&lt; 8</td>
</tr>
<tr>
<td>Operation Temperature</td>
<td>ºC</td>
<td>&gt; 175</td>
</tr>
<tr>
<td>Processing Temperature</td>
<td>ºC</td>
<td>&gt; 250</td>
</tr>
</tbody>
</table>

Criterion for thin dielectric selection for power module substrate applications

- **Thermal conductivity** need not be high, due to thin dielectric
- **Sufficient breakdown voltage** for adequate margin for 1200V SiC MOSFETs
- **Low leakage current comparable with SiC devices** at the same conditions, such as temperature
- **High temperature** operation similar to SiC devices
- **High processing temperature** to leave margin for assembly processes

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From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, YiFan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 - Jun 02, 2018

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PREES Laboratory

Packaging Research in Electronic Energy Systems
Epoxy Resin Composite Dielectric by RISHO

**HIGH THERMAL CONDUCTIVITY MATERIALS**

<table>
<thead>
<tr>
<th>Liquid Molding Compound</th>
<th>AC-7208</th>
<th>AC-7210</th>
</tr>
</thead>
<tbody>
<tr>
<td>(One-pack type) 1-4W/mK</td>
<td>8W/mK</td>
<td>10W/mK</td>
</tr>
<tr>
<td>Liquid Molding Compound</td>
<td>AD-7208</td>
<td>AD-7210</td>
</tr>
<tr>
<td>(Two-pack type) 1-7W/mK</td>
<td>8W/mK</td>
<td>10W/mK</td>
</tr>
</tbody>
</table>

**Bonding sheet, RCC, Copper-base CCL without glass fabric**

Courtesy of RISHO

Investigating Flexible Thin Dielectric as Substrates

**Target Material:** Recently developed Epoxy-Resin based dielectric by Risho Kogyo Co., Ltd. – AC-7208

**Properties of the Thin Dielectric (measured at 120 μm)**

- **Better Stress Management**
  - CTE closer to copper than traditional ceramic (4.5 ppm/K ~ 7 ppm/K)
  - Flexible allowing for stress release during assembly and service of the module

**Comparable thermal performance with alumina**

- Better unit area thermal conductance than alumina
- 1/5 unit area thermal conductance of AIN
- Lower cost for epoxy-resin substrate

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unite</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Conductivity</td>
<td>W/mK</td>
<td>8</td>
</tr>
<tr>
<td>Tg</td>
<td>°C</td>
<td>270</td>
</tr>
<tr>
<td>Modulus</td>
<td>GPa</td>
<td>30</td>
</tr>
<tr>
<td>Bending Strength</td>
<td>MPa</td>
<td>94</td>
</tr>
<tr>
<td>CTE</td>
<td>ppm/K</td>
<td>9/22</td>
</tr>
<tr>
<td>DK</td>
<td>/</td>
<td>6.3</td>
</tr>
<tr>
<td>DF</td>
<td>/</td>
<td>0.009</td>
</tr>
<tr>
<td>Water Absorption</td>
<td>%</td>
<td>0.27</td>
</tr>
<tr>
<td>Dielectric Strength</td>
<td>kV</td>
<td>5.6 @ 120 μm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parts</th>
<th>Thickness /μm</th>
<th>Thermal Conductivity W/m-K</th>
<th>Unit Thermal Conductance W/m²⁻°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Epoxy-resin</td>
<td>80</td>
<td>8</td>
<td>0.1E6</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>254</td>
<td>23</td>
<td>0.09E6</td>
</tr>
<tr>
<td>AIN</td>
<td>254</td>
<td>170</td>
<td>0.67E6</td>
</tr>
</tbody>
</table>

From Xin Zhao Presentation: “New Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishipuchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL, May 30 - Jun 02, 2018
Epoxy Resin Composite Dielectric

- Capable of bonding with Copper on both sides
- Copper thickness up to ≤ 0.6 mm
- 80 µm dielectric thickness is available

Leakage current measured on 80 µm sample with Cu bonded on both sides
- 20 µA leakage even at 250 °C with 1200 V voltage applied
- 1 nA leakage at room temperature with > 4kV voltage applied

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECCE, Orlando, FL May 30 – Jun 02, 2018

Resource Development for ERCD Topology Research

1. ERCD "substrate-less" approaches identified for high voltage (5kV/120µm), high temperature (≤300°C) and high thermal impedance (10W/mK).
2. Materials systems for fluid compatibility, multilayering and metal backing for investigation of dense high voltage power module structures.
3. Processes and equipment for ERCD systems identified and ordered through PREES resources.
**ERCD Composition**

Microstructure of the dielectric at 20,000 magnification

- O is corresponding to alumina particles, distributed almost everywhere, N is the AlN particles, with limited number, C is from the polymer, Cu is from the bonding interface
- AlN and alumina particles are also identified by XRD analysis
- High thermal conductivity is from the widely distributed alumina particles and few AlN particles

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECCTC, Orlando, FL May 30 – Jun 02, 2018

**ERCD Breakdown Voltage**

Properties during reliability experiments (Thermal aging and thermal cycling)

- Thermal aging is conducted at 150 °C
- Thermal cycling is from -55°C to 125 °C
- Peel strength (35µm copper on 120µm dielectric with 1mm Al) is not as high as DBC interface (4N/mm for 0.3mm Cu on alumina)
- Limited degradation during thermal aging up to 200 Hr in breakdown voltage and peel strength
- The properties do not change much during thermal cycling up to 1000 cycles

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECCTC, Orlando, FL May 30 – Jun 02, 2018
## AC-7208 (8W/mK)

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product number</td>
<td>AC-7208</td>
</tr>
<tr>
<td>Dielectric layer thickness</td>
<td>120μm</td>
</tr>
<tr>
<td>Thermal cond. (W/mK)</td>
<td>8</td>
</tr>
<tr>
<td>Tg(°C)</td>
<td>270</td>
</tr>
<tr>
<td>Peel strength (kN/m)</td>
<td>1.2</td>
</tr>
<tr>
<td>Solder limit (sec)</td>
<td>Over 60</td>
</tr>
<tr>
<td>CTE (ppm/°C)</td>
<td>9/22</td>
</tr>
<tr>
<td>Breakdown (kV)</td>
<td>Over 5</td>
</tr>
<tr>
<td>CTI</td>
<td>Over 600</td>
</tr>
<tr>
<td>Flammability</td>
<td>V-0 equiv. UL94</td>
</tr>
</tbody>
</table>

---

### High temperature long term test (@175°C)

![Graph showing high temperature long term test](image)

---

### Thermal cycle test (-40°C to 125°C)

![Graph showing thermal cycle test](image)

---

After long term test at 175°C and thermal cycle test, there is no problem in breakdown voltage and peel strength. This material also shows high reliability.

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## AC-7210 (10W/mK)

<table>
<thead>
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<th>Property</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Product number</td>
<td>AC-7210</td>
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<tr>
<td>Dielectric layer thickness</td>
<td>120μm</td>
</tr>
<tr>
<td>Thermal cond. (W/mK)</td>
<td>10</td>
</tr>
<tr>
<td>Tg(°C)</td>
<td>270</td>
</tr>
<tr>
<td>Peel strength (kN/m)</td>
<td>1.2</td>
</tr>
<tr>
<td>Solder limit (sec)</td>
<td>60&lt;</td>
</tr>
<tr>
<td>CTE (ppm/°C)</td>
<td>14/14/14</td>
</tr>
<tr>
<td>Breakdown voltage (kV)</td>
<td>5&lt;</td>
</tr>
<tr>
<td>CTI</td>
<td>600&lt;</td>
</tr>
<tr>
<td>Flammability</td>
<td>V-0 equivalent UL94</td>
</tr>
</tbody>
</table>

---

### HIGH TEMPERATURE LONG TERM RELIABILITY (175°C)

![Graph showing high temperature long term reliability](image)
# High Heat resistance CCL for Power Modules

Low CTE and high heat resistance material
CS-3305A (CCL)
ES-3310A (Prepreg)

Ultra-thin thickness (15μm of 1ply type or 30μm of 2ply type)

---

## General properties of CS-3305A series

<table>
<thead>
<tr>
<th>Item</th>
<th>Unit</th>
<th>CS-3305A (E-glass)</th>
<th>CS-3305AS (Low CTE glass)</th>
<th>CS-3305AQ (Quartz glass)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTE (Other Low CTE glass fabric enables lower CTE)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Y  ( \alpha_1 )</td>
<td>ppm</td>
<td>6~8</td>
<td>2~4</td>
<td>0.5~1</td>
</tr>
<tr>
<td>X  ( \alpha_1 )</td>
<td>ppm</td>
<td>6~8</td>
<td>2~4</td>
<td>0.5~1</td>
</tr>
<tr>
<td>Z  ( \alpha_1 )</td>
<td>ppm</td>
<td>10~15</td>
<td>10~15</td>
<td>10~15</td>
</tr>
<tr>
<td>Glass transition Temperature (Tg)</td>
<td>°C</td>
<td></td>
<td></td>
<td>Over 300°C</td>
</tr>
<tr>
<td>DMA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Water absorption ratio</td>
<td>%</td>
<td>0.13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flexural strength (Y-axis)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25°C MPa</td>
<td></td>
<td>517</td>
<td>660</td>
<td>446</td>
</tr>
<tr>
<td>250°C MPa</td>
<td></td>
<td>415</td>
<td>470</td>
<td>356</td>
</tr>
<tr>
<td>Flexural modulus (Y-axis)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25°C GPa</td>
<td></td>
<td>32</td>
<td>35</td>
<td>32</td>
</tr>
<tr>
<td>250°C GPa</td>
<td></td>
<td>16</td>
<td>19</td>
<td>19</td>
</tr>
<tr>
<td>Peel strength (Copper)</td>
<td>KN/m</td>
<td>0.6</td>
<td>[VLP 1/3oz]</td>
<td></td>
</tr>
<tr>
<td>Solder heat resistance (300°C)</td>
<td>Sec.</td>
<td>over300</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

![Image of CCL thickness comparison](image-url)

---

**Courtesy of RISHO**

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High Tg and high modulus by DMA method

- There is no tanδ peak of CS-3305A → Tg : over 300°C
- Storage modulus maintains higher than the other material under the high temperature.

Thermal decomposition temperature by TGA method

CS-3305A is a long term heat resistance material.

<table>
<thead>
<tr>
<th></th>
<th>CS-3305A</th>
<th>Standard FR-4.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Td(1%)</td>
<td>352°C</td>
<td>277°C</td>
</tr>
<tr>
<td>Td(5%)</td>
<td>487°C</td>
<td>310°C</td>
</tr>
</tbody>
</table>

Atmosphere : Air
Heating rate : 10°C/min
Reference : Al₂O₃
Retention of peel strength of copper foil

- Delamination between copper foil and dielectric layer of standard FR-4.0 was occurred at 175°C.
- CS-3305A maintained peel strength at 175 and 200°C even after 3000 hours treatment.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>CS-3305A 175°C</th>
<th>CS-3305A 200°C</th>
<th>CS-3305A 200°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 hr. (Retention)</td>
<td>1.30 kN/m (100%)</td>
<td>1.30 kN/m (100%)</td>
<td>1.60 kN/m (100%)</td>
</tr>
<tr>
<td>1500 hr. (Retention)</td>
<td>1.25 kN/m (98%)</td>
<td>1.25 kN/m (98%)</td>
<td>1.25 kN/m (80%)</td>
</tr>
<tr>
<td>3000 hr. (Retention)</td>
<td>1.25 kN/m (97%)</td>
<td>1.25 kN/m (92%)</td>
<td>0.99 kN/m (62%)</td>
</tr>
</tbody>
</table>

650Vdc/20A ½-bridge IPM based on RISHO Substrate

From: PowerAmerica Short Course Nov 2018
Raleigh, NC
650Vdc/20A ½-bridge IPM based on RISHO Substrate

Parameters:
- 650V maximum DC bus voltage
- 20A maximum RMS current per device
- 400V->200V Half-bridge buck
- Internal decoupling cap

IDEAL: Simulation condition: 10A, 100pF C

Overshoot w/o decoupling cap
240V @ 100nH
7V @ 5nH

Overshoot w decoupling cap
7V @ 5nH

Parts:
Q1 Q2: Ideal
C1 C2: 10uF 25V X7R
C3: 47nF 1kV X7R
R1: 220Ohm 1/8W
D1: Ideal HF diode
U1: Ideal isolated HB driver

Thermal Analysis

Thermal analysis w/ first order estimation of losses:
\[
P_{\text{ds}} = 129m\times 20A^2 = 51.6W \text{ at } T_{\text{max}}=150^\circ C
\]
\[
P_{\text{sw}} = 55uJ\times 0.5MHz = 27.5W \text{ at } 400V, 15A
\]
\[
P_{\text{tot}} = P_{\text{ds}} + P_{\text{sw}} = 79.1W
\]

Given:
- Die Pad = 6mm X 3mm,
- ERCD Substrate thickness = 80µm,
- Al case thickness = 0.9mm:

Approximating with 45° rule:
\[
A_{\text{sub}} = (6mm + 0.04mm) \times (3mm + 0.04mm) = 18.4mm^2
\]
\[
A_{\text{case}} = (6mm + 0.04mm + 0.9mm) \times (3mm + 0.04mm + 0.9mm) = 27.3mm
\]
\[
R_{\text{sub}} = 0.08mm/18.4mm^2 \times 1000/(10W/m^\circ C) = 0.43 \circ C/W
\]
\[
R_{\text{case}} = 0.9mm/27.3mm^2 \times 1000/(205W/m^\circ C) = 0.16 \circ C/W
\]

\[
R_{\text{total}} = R_{\text{chip}} + R_{\text{sub}} + R_{\text{case}} = 0.5 \circ C/W + 0.43 \circ C/W + 0.16 \circ C/W = 1.09 \circ C/W
\]

At \( P = 56.5W \), \( T_{\text{case}} = 40^\circ C, T_j = 40^\circ C + 79.1W \times 1.09 \circ C/W = 126.2^\circ C \), < \( T_{\text{max}} = 150^\circ C \)

Thank you to sponsors:
**Inductance & Performance**

Inductance estimation:
1. Power loop: 6.5nH using rectangle estimation
2. Gate loop: 3.8nH using rectangle estimation

For optimal gate driver at Q=1.5 (0.3V overshoot):
\[ R = \frac{(L/C)^{1/2}}{Q} = 2.5 \, \Omega \]
\[ L = 3.8nH, \quad C = C_{iss} = 0.26nF \]

Gate driver has \( R_{out} = 2.7\Omega > 2.5 \), therefore no \( R_{ext} \) is required. Then, simulation shows only 0.26V gate overshoot, well within GaN ratings.

---

**Buck converter with Q1 as switch and Q2 as sync rect.**

Full SPICE simulation at 400V->200V 20A:
\[ L_{power-loop} = 6.5 \, nH \]
\[ L_{gate-loop} = 3.8 \, nH \]
\[ C_{substrate\, \text{cap}} = 28.9 \, pF \] (parallel plate method)
\[ R_{heatsink} = 10\Omega \, \text{sink-to-} Q_{source} \]

Results:
\[ P_{loss} = 42.5W \text{ for Q1, } T_j=86.3C \]
\[ P_{loss} = 15.8W \text{ for Q2, } T_j=57.2C \]

Switching \( V_{DS} \) waveform shows 70% overshoot above the 400V

---

Parts:
- Q1 Q2: GS66508B
- C1 C2: 10uF 25V X7R
- C3: 47nF 1kV X7R
- R1: 220ohm 1/8W
- D1: CURN101-HF diode
- UT-Si8274 isolated HB driver
- Bottom-side cooled 650V
- E-mode GaN Systems
**SiC Integrated Power Module Test Design**

Excerpt from: Xin Zhao[1] Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

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[1] Now at Univ. of Texas at Austin

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**Double Sided Design**

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**Substrates on Double Side**

- Volume: 35 mm $\times$ 15.5 mm $\times$ 3mm
- Power Devices: CPM2-1200-0025B / CPW5-1200-Z050B
- Rating: 800 V / 40 A
- Auxiliary terminals on single side of the module, allowing for both side heat sink attachment, with terminals able to attached on PCB for interconnections
SiC IPM Design

Circuit Schematic Design

Schematic Design for SiC half bridge IPM
- Bootstrap Power Supply
- Digital Isolator
- LDO
- Gate driver Circuits
- -5V turn-off power supply
- Single switch pair IPM is developed as initial investigation

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

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Simulation of the SiC IPM Design

Simulation for Parasitic Extraction

Power stage 3D model

Current distribution in the power loop

Summary of extracted parasitics

<table>
<thead>
<tr>
<th>Location</th>
<th>Inductance / nH</th>
<th>Resistance / mΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC+ → DC-</td>
<td>0.6</td>
<td>0.22</td>
</tr>
<tr>
<td>MOSFET Drain</td>
<td>0.44</td>
<td>0.20</td>
</tr>
<tr>
<td>MOSFET Source</td>
<td>0.20</td>
<td>0.10</td>
</tr>
<tr>
<td>Diode Anode</td>
<td>1.87</td>
<td>0.38</td>
</tr>
<tr>
<td>Diode Cathode</td>
<td>2.23</td>
<td>0.46</td>
</tr>
</tbody>
</table>

- Inductance in the entire loop is 0.6 nH.
- Diode inductance is larger, since it parallels the MOSFET drain to source.
- Applicable for lower losses and higher operation frequency.

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
SiC-IPM Layout

Circuit Layout Design

Layout design for the SiC half bridge IPM
- Interconnections are applied to both top and bottom side of substrates
- Interconnection metal in the main power loop is a compromise between thermal spreading and EMI noise reduction
- Only the layout (c) and (d) are discussion in the presentation for the single switch module
- The layout design is not optimized and the long gate loop trace on the plane, results in excessive noise during switching
- Jumper wire minimizes gate loop length during the fabrication for demonstration of the design

SiC IPM Fabrications & Measurements

Module Assembly & MOSFET Statics Test

The forward and reverse characteristics of SiC MOSFET is similar with data shown on the datasheet[7].

The proposed module fabrication and assembly process, including the topside metallization process of SiC devices, can fully exhibits the initial performance of the SiC devices

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiozaki, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Florida, FL, May 30 – Jun 02, 2018
SiC IPM Fabrications & Measurements

Module Assembly & Driver Circuits Test

- Flip-chip assembly for SiC MOSFET and Diode
- Underfill applied for 1200V isolation
- Large terminals for testing

Gate pad is on same plane as gate driver, output signal verified for -5V turn-off and 20V turn-on of MOSFET

Conclusions

- Selection Criterion of Thin dielectric substrate material is set up based on design requirements of 1200V WBG device based IPMs.
- A 120μm recently developed flexible epoxy-resin based dielectric, by Risiko Kogyo Co., Ltd., is investigated, and proved to be suitable for power module substrate in terms of electrical, thermal, mechanical properties, cost, and reliability.
- A high-density half-bridge SiC power module is designed with ultra-low parasitics, utilizing epoxy-resin based dielectric, for high-frequency and low-loss applications.
- Fabrication process of double-side solderable SiC MOSFETs and diodes is developed, capable of deposition of metallization layer up to 2μm.
- A single-switch SiC power module with more functionality is fabricated, allowing for double-side cooling functions, verified by static measurements.
- The proposed substrate material, and designed WBG IPM with ultra-low parasitics, high functionality and double-side cooling is verified and show potential for high frequency and high power density applications.

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
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