FREEDM SYSTEM CENTER
Annual Research Symposium
April 10-12, 2019
Duke Energy Hall, Hunt Library

Trends in Power Electronics Packaging
Prof Douglas C. Hopkins, Ph.D.
New Resource for ERCD Ckt Topology Research

Epoxy Resin Composite Dielectrics (ERCD)
ERCD "substrate-less" approaches identified for high voltage (5kV/120µm), high temperature (≤300ºC) and high thermal impedance (10W/mK)
Today, power electronics has strong growth across a board range of power levels. This particularly applies to increases that improve lives versus enhancing entertainment.

However, increasing density and reducing cost still are the primary goals for all designs, and brings focus on Functional Integration at the Systems Level.
Problem? ... much smaller WBG devices

The challenge in thermal management will broaden to address essentially point-source heat generation due to higher power capabilities with shrinking die size ... compared to Si die.
Huang in 2004 developed three pertinent figures of merit [1].

\[ E_c \] is critical electric breakdown field, 
\( \mu \) is electron mobility, 
\( \varepsilon \) is dielectric constant, 
\( \sigma_{th} \) is thermal conductivity

Shrinking Die Size (so to speak)

- The FOM for GaN & SiC show substantial performance as die size can shrink, OR the power rating increases.
- Small die are preferred for higher and higher frequencies.

<table>
<thead>
<tr>
<th>Semiconductor Materials</th>
<th>Electron mobility μ (cm²/V·s)</th>
<th>Relative dielectric constant ε</th>
<th>Critical field E_c (kV/cm)</th>
<th>Thermal conductivity σ_th (W/m·K)</th>
<th>HMFOM = ( E_c \sqrt{\mu} )</th>
<th>HCAFM = ( \varepsilon E_c^2 \sqrt{\mu} )</th>
<th>HTFOM = ( \frac{\sigma_th}{\varepsilon E_c} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>8,500</td>
<td>13.1</td>
<td>400</td>
<td>55</td>
<td>3.3</td>
<td>4.9</td>
<td>0.3</td>
</tr>
<tr>
<td>GaN</td>
<td>900</td>
<td>9</td>
<td>3,000</td>
<td>110</td>
<td>8.0</td>
<td>61.7</td>
<td>0.1</td>
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<tr>
<td>Ge</td>
<td>3,900</td>
<td>16</td>
<td>100</td>
<td>58</td>
<td>0.6</td>
<td>0.3</td>
<td>1.0</td>
</tr>
<tr>
<td>Si</td>
<td>1,400</td>
<td>11.7</td>
<td>300</td>
<td>130</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>SiC(6H,α)</td>
<td>250</td>
<td>11.1</td>
<td>1,000</td>
<td>110</td>
<td>1.4</td>
<td>4.5</td>
<td>0.3</td>
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<tr>
<td>SiC(4H,α)</td>
<td>330</td>
<td>9.66</td>
<td>2,400</td>
<td>700</td>
<td>3.5</td>
<td>25.7</td>
<td>0.8</td>
</tr>
<tr>
<td>Diamond</td>
<td>2,200</td>
<td>5.7</td>
<td>5,700</td>
<td>2,000</td>
<td>23.8</td>
<td>220.5</td>
<td>1.7</td>
</tr>
</tbody>
</table>

\( E_c \): critical field
\( \mu \): mobility
\( \varepsilon \): dielectric constant
\( \sigma \): thermal conductivity

High Frequency Potential (e.g. Unipolar - MOSFET)

Since current does not scale, the speed ~ \( \text{i/c} \), is significantly increased in WBG devices. Speed measured as \( \text{di/dt} \) or \( \text{dv/dt} \).

The reduction in size supports high frequency operation, but creates a greater challenge in heat dissipation and Integration.


Comparison is based on hard switched converters with fixed \( f \), \( I \), and \( V \). ZVS for high voltage provides other advantages for SiC.
Small Die for High Voltage – 9kV design in air

Packaging materials have always needed to passivate the chip for voltages greater than ~150V.

Small Die experiences breakdown at 1,800 V.
(Experimental design at NCSU)

A great emphasis to develop “Medium Voltage” power electronic systems is underway for large and small systems, e.g. portable x-ray equipment to large autonomous trucks.
The ‘Ground-Baseplate’ Problem in Packaging

It’s all about vertically conducting devices
Ground Coupling

Review of mid-point voltage...

However, there is a major current path when SW-Top turns on.
What is the problem?

\[ i = C \frac{dV}{dt} \]
SiC MOSFET Chip Dimensions (used later also)

Mechanical Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Dimensions (L x W)</td>
<td>4.08 x 4.08</td>
<td>mm</td>
</tr>
<tr>
<td>Exposed Source Pad Metal Dimensions</td>
<td>0.98 x 2.09 (x 2)</td>
<td>mm</td>
</tr>
<tr>
<td>Gate Pad Dimensions</td>
<td>0.84 x 0.60</td>
<td>mm</td>
</tr>
<tr>
<td>Chip Thickness</td>
<td>365 ± 40</td>
<td>µm</td>
</tr>
<tr>
<td>Frontside (Source) metallization (Al)</td>
<td>4</td>
<td>µm</td>
</tr>
<tr>
<td>Frontside (Gate) metallization (Al)</td>
<td>4</td>
<td>µm</td>
</tr>
<tr>
<td>Backside (Drain) metallization (Ni/Ag)</td>
<td>0.8 / 0.6</td>
<td>µm</td>
</tr>
</tbody>
</table>

CPMF-1200-S080B
Ground Coupling (continued)

What current flows into ‘ground’ from the transistor drain?

Given:
FET: Minimum drain area of semiconductor and solder is $4.5 \text{mm} \times 4.5 \text{mm} = 20.25 \text{mm}^2$
+ bonding pad $2.5 \times 2.5 \text{mm} = 6.25 \text{mm}^2$
+ circuit trace is $5 \text{mm} \times 10 \text{mm} = 50 \text{mm}^2$

Substrate:
$\text{Al}_2\text{O}_3$ (with $\varepsilon_r = 9.4$) at 635µm thick

Find switching current:
Area, $A = 20.25 + 6.25 + 50 = 76.5 \text{ mm}^2$
Distance: $d = 0.635 \text{ mm}$
Capacitance, $C = \varepsilon_r \varepsilon_o A / d = 10 \text{ pF}$
$i = C (dV/dt) = 10 \text{ pF} (425/20\text{ns})$

$i = 0.21 \text{ A}$
Multi-die Modules

Add diode and space: X2.2, Multiply by die in parallel: X8, (Add terminal footprint)
Then,
\[ i_T = 0.21 \times 2.2 \times 9 = 4.2 \text{A@20ns} \]
(For one side)

Standard packages add even more
High Voltage Capacitive Current

Switching >10kV can occur at 125kV/µs

For a generalized SiC die of 1cm X 1cm
Use a 40mil (1.02mm) thick AlN ceramic
ε_r = 8.6,  ε_o =8.85 X 10^{-12} F/m
The Capacitance, C=ε_rε_o A / d
A = 10^{-4} m^2, d = 10^{-3}m
∴ C = 7.6 pF, “per sq. cm”

Find switching current at 10kV & 125 kV/µs:
\[ i = C \frac{dV}{dt} = 7.6 \text{ pF} \times (125 \text{kV/µs}) \]
\[ i = 0.95 \text{ A} \ “per \ sq. cm” \]
For multiple dies and diodes use X19.8
Or \[ i = 18.8 \text{ A} \]

Thermal performance of metal clad ceramics
Rth [°C/W] for 5mmX5mm SiC on 12/25/12 DBC

<table>
<thead>
<tr>
<th>Part</th>
<th>Width (mm)</th>
<th>Length (mm)</th>
<th>Thickness (mm)</th>
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<tbody>
<tr>
<td>Device</td>
<td>5</td>
<td>5</td>
<td>0.36</td>
</tr>
<tr>
<td>Solder</td>
<td>5.1</td>
<td>5.1</td>
<td>0.05</td>
</tr>
<tr>
<td>Metal</td>
<td>5.7</td>
<td>5.7</td>
<td>0.3</td>
</tr>
<tr>
<td>Ceramic</td>
<td>6.97</td>
<td>6.97</td>
<td>0.635</td>
</tr>
<tr>
<td>Metal</td>
<td>7.57</td>
<td>7.57</td>
<td>0.3</td>
</tr>
<tr>
<td>Solder</td>
<td>7.67</td>
<td>7.67</td>
<td>0.05</td>
</tr>
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<td>AlSiC</td>
<td>13.67</td>
<td>13.67</td>
<td>3</td>
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<table>
<thead>
<tr>
<th>COMSOL</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Heat Flux (W)</td>
<td>100</td>
</tr>
<tr>
<td>Bottom Plate Temperature</td>
<td>293°K</td>
</tr>
<tr>
<td>Mesh</td>
<td>Fine</td>
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3D Prismatic Packaging – True 3D

Dissertation work of Dr. Haotao Ke, September 2017
“3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules”
State of Art Works

Planar 2D power packaging technology

- Flex circuit structure
  - POL package, SKiN package, etc.
- Embedded structure
  - AT&S GaNPX, PCB embedded, etc.
- Sandwiched structure
  - Planar Bond All package, etc.

ABB Stacked DBC [1]

Power Overlay package [4]

SKiN module [5]

PCB embedded module[6]

GaN PX package[7]

“3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules,” Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017
State of Art Works

3D power packaging technology

- Device level
  - Quilt dies, stacked / vertical dies
- Module level
  - 3D CSP, Power chip on chip, 3D power circuit

Quilt packaging[9]

Power chip on chip[11]

3D Power module[10]

3D CSP module[12]

Stacked device[13]

Vertical connected device[14]

“3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules,” Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017
**3-D Prismatic Package**

**Objective**

- Investigation of power module topologies in >2D

3-D Prismatic package should have:

- Low parasitic inductance
- Good thermal performance
- High power density
- Capability to handle thermal stress brought by high temperature operation, if properly designed

"3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules," Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017
References


The 3D Power Path Concept

Low inductance is desired for WBG module
- Minimize voltage overshoot
- Reduce switching loss

\[
L = \begin{bmatrix}
L_1 & L_2 & L_3 \\
L_2 & L_3 & L_4 \\
L_3 & L_4 & L_4 \\
L_4 & L_4 & L_4
\end{bmatrix}
\]

\[
\begin{bmatrix}
v_1 \\
v_2 \\
v_3 \\
v_4
\end{bmatrix} =
\begin{bmatrix}
L_1 & L_2 & L_3 & L_4 \\
L_2 & L_3 & L_4 & L_4 \\
L_3 & L_4 & L_4 & L_4 \\
L_4 & L_4 & L_4 & L_4
\end{bmatrix}
\begin{bmatrix}
di/ dt \\
di/ dt \\
di/ dt \\
di/ dt
\end{bmatrix}
\]

\[
\Delta V = L_x \frac{di}{dt}
\]

\[
\Delta V = v_1 + v_2 + v_3 + v_4 = (L_1 + L_2 + L_3 + L_4) \frac{di}{dt}
\]

"3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules," Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017
The 3D Power Path Concept

Options to lower inductance in 2D

- Minimize each element (L1 ~ L4)
- Bring in mutual inductance (M14 & M23)

\[
L = \begin{bmatrix}
L_1 & L_2 & -M_{14} \\
-M_{23} & L_3 & L_4 \\
-M_{41} & -M_{32} & L_4
\end{bmatrix}
\]

\[
\Delta V = L_s \frac{di}{dt}
\]

\[
\begin{bmatrix}
v_1 \\
v_2 \\
v_3 \\
v_4
\end{bmatrix} = 
\begin{bmatrix}
L_1 & L_2 & -M_{14} \\
-M_{23} & L_3 & L_4 \\
-M_{41} & -M_{32} & L_4
\end{bmatrix}
\begin{bmatrix}
\frac{di}{dt} \\
\frac{di}{dt} \\
\frac{di}{dt} \\
\frac{di}{dt}
\end{bmatrix} = 
\begin{bmatrix}
(L_1 - M_{14}) \frac{di}{dt} \\
(L_2 - M_{23}) \frac{di}{dt} \\
(L_3 - M_{32}) \frac{di}{dt} \\
(L_4 - M_{41}) \frac{di}{dt}
\end{bmatrix}
\]

\[
\Delta V = v_1 + v_2 + v_3 + v_4
\]

\[
= (L_1 - M_{14}) \frac{di}{dt} + (L_2 - M_{23}) \frac{di}{dt} + (L_3 - M_{32}) \frac{di}{dt} + (L_4 - M_{41}) \frac{di}{dt}
\]

\[
= (L_1 + L_2 + L_3 + L_4) \frac{di}{dt} - 2(M_{14} + M_{23}) \frac{di}{dt}
\]

"3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules," Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017
The 3D Power Path Concept

3D Power path to lower inductance
- Fold output terminal to P/N terminal side
- Bring in more mutual inductance cancelation

\[ L = \begin{bmatrix} L_1 & -M_{12} & -M_{13} & -M_{14} \\ -M_{21} & L_2 & -M_{23} & -M_{24} \\ M_{31} & -M_{32} & L_3 & -M_{34} \\ -M_{41} & M_{42} & -M_{43} & L_4 \end{bmatrix} \]

\[ \Delta V = L_s \frac{di}{dt} \]

\[ \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} I_1 & -M_{12} & M_{13} & -M_{14} \\ -M_{21} & L_2 & -M_{23} & M_{24} \\ M_{31} & -M_{32} & L_3 & -M_{34} \\ -M_{41} & M_{42} & -M_{43} & L_4 \end{bmatrix} \begin{bmatrix} \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \end{bmatrix} = \begin{bmatrix} (I_1 - M_{14}) \frac{di}{dt} - (M_{12} - M_{13}) \frac{di}{dt} + (I_2 - M_{23}) \frac{di}{dt} - (M_{21} - M_{24}) \frac{di}{dt} + (I_3 - M_{32}) \frac{di}{dt} - (M_{31} - M_{34}) \frac{di}{dt} + (I_4 - M_{41}) \frac{di}{dt} - (M_{43} - M_{42}) \frac{di}{dt} \\ (I_1 - M_{14}) \frac{di}{dt} - (M_{12} - M_{13}) \frac{di}{dt} + (I_2 - M_{23}) \frac{di}{dt} - (M_{21} - M_{24}) \frac{di}{dt} + (I_3 - M_{32}) \frac{di}{dt} - (M_{31} - M_{34}) \frac{di}{dt} + (I_4 - M_{41}) \frac{di}{dt} - (M_{43} - M_{42}) \frac{di}{dt} \\ (I_1 - M_{14}) \frac{di}{dt} - (M_{12} - M_{13}) \frac{di}{dt} + (I_2 - M_{23}) \frac{di}{dt} - (M_{21} - M_{24}) \frac{di}{dt} + (I_3 - M_{32}) \frac{di}{dt} - (M_{31} - M_{34}) \frac{di}{dt} + (I_4 - M_{41}) \frac{di}{dt} - (M_{43} - M_{42}) \frac{di}{dt} \\ (I_1 - M_{14}) \frac{di}{dt} - (M_{12} - M_{13}) \frac{di}{dt} + (I_2 - M_{23}) \frac{di}{dt} - (M_{21} - M_{24}) \frac{di}{dt} + (I_3 - M_{32}) \frac{di}{dt} - (M_{31} - M_{34}) \frac{di}{dt} + (I_4 - M_{41}) \frac{di}{dt} - (M_{43} - M_{42}) \frac{di}{dt} \end{bmatrix} = \begin{bmatrix} (I_1 + I_2 + I_3 + I_4) \frac{di}{dt} - 2(M_{12} + M_{23}) \frac{di}{dt} - 2(M_{14} + M_{23}) \frac{di}{dt} - 2(M_{14} + M_{33}) \frac{di}{dt} - 2(M_{14} + M_{43}) \frac{di}{dt} \end{bmatrix} \]

\[ M_{12} > M_{13} \]

"3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules," Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017
The 3D Power Path Concept

Simulation verification (Ansoft Q3D)
- Cu trace cross section: 12mil (0.3mm) by 15 mm
- Current return point: 60 mm
- Spacing: 10mm lateral & 2mm vertical
- Extract inductance between Positive (P) and Negative (N) terminals at 1MHz

41.2 nH
28.3 nH

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HB Module Fabrication

Half bridge schematic as 1st prismatic Module

- 4 Devices, 7 terminals
- Electrical – 3D Power path
- Thermal – 5 sided cooling

Schematic

2D path in power module

3D path in module

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True-3D Module (Phase leg)

Current path in 3D, and Mutual inductance seen from $L_1$

$L = \begin{bmatrix}
L_1 & -M_{12} & M_{13} & -M_{14} \\
-M_{21} & L_2 & -M_{23} & M_{24} \\
M_{31} & -M_{32} & L_3 & -M_{34} \\
-M_{41} & M_{42} & -M_{43} & L_4
\end{bmatrix}$

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Simulated v. Measured Inductance for HB Module

ANSYS Q3D impedance extractor
- AC RL simulation @ 100MHz
- Module inductance between Positive (P) and Output (O) is 9nH

Impedance test with vector network analyzer
- Test with a 3mm wire (1nH) – 7 nH
- Test with module – 12 nH
- Module inductance between Positive (P) and Output (O) is ~6nH

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Half Bridge Module

3D prismatic structure vs Planar Bond All structure
- Similar electrical performance (resistance / inductance / symmetric current path)
- Competitive thermal performance
- Potentially better mechanical performance
- Much smaller footprint

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True-3D Mounting and Electrical Testing

Impedance test with vector network analyzer
- Test w/ 3mm wire (1nH): 7nH
- Test w/ module: 12nH
- 3D module L from Pos and Out is ~6nH

- 1200V/50A SiC MOSFETs & JBS Diode

Double Pulse Testing

50A-to-0A

$t_r = \sim 5\text{ns}$

50A-to-0A

$t_r = \sim 3\text{ns}$

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Thermal Simulation of HB Module

Simulation for half bridge module

- Heatsink simulation (COMSOL)
  - Material: 85Cu15Zn (UNS 23000 red brass)
  - Heat source: 15W per chip
  - Ambient: 25°C air at 7m/s
  - Dimension: 1.5 x 1.5 x 7.5 mm pins with 1.5 spacing.

- Simulation result
  - Max temperature for 3D heatsink: 100 °C
  - Max temperature for planar heatsink: 196 °C with 10 °C difference between two chips

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Thermal Test of HB Module

Test of half bridge module

- Thermal test set up:
  - 20A through L-SBD
  - Measurement points:
    - Tj – Thermistor
    - Theatsink – Thermal couple / IR
    - Tambient – Air flow sensor

- Test result: 
  \[ R_b = \frac{T_j - T_a}{P_{loss}} = \frac{90 - 46}{20 \times 1.3} = 1.69 \frac{^\circ C}{W} \]
Mechanical Simulation of HB Module Ctr Post

Simulation for half bridge module
- Inner post simulation (COMSOL)
  - Material: 85Cu15Zn (UNS 23000 red brass)
  - Heat source: 200°C at chip contact
  - Ambient: 100°C at bottom
  - Constrains: Prescribed displacement
- Simulation result
  - Max von Mises stress: $3 \times 10^8$ N/m²
  - Yield strength of red brass 69-434 Mpa (depending on post process)

<table>
<thead>
<tr>
<th>Properties (UNS23000)</th>
<th>Metric</th>
<th>Imperial</th>
</tr>
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<tbody>
<tr>
<td>Tensile strength</td>
<td>269-724 MPa</td>
<td>39-105 ksi</td>
</tr>
<tr>
<td>Yield strength</td>
<td>69-434 MPa</td>
<td>10-70 ksi</td>
</tr>
<tr>
<td>Elongation</td>
<td>55%</td>
<td>55%</td>
</tr>
<tr>
<td>Poisson's ratio</td>
<td>0.34</td>
<td>0.34</td>
</tr>
<tr>
<td>Elastic modulus</td>
<td>117 GPa</td>
<td>16969 ksi</td>
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</tbody>
</table>

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3Ø Bridge Concept

Example: 3-phase full bridge prismatic module

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New thin dielectrics for Low Cost modules

Ceramics?
Flexible-Ceramic Power Electronics Packaging

**NEEDS ADDRESSED**

*High Density, Fast Response, Low Voltage, System-in-Package Power Converters*

- Need Inexpensive converters with good thermal management
- Operate Temp ≤85°C (similar to PCB)
- Suitable for high current GaN
  - and wearable power electronics

**TECHNOLOGY**

- Thin E-Strate flexible 3YSZ ceramic for:
  - High volume roll-to-roll manufacturing
  - High thermal management for highly dense LV power converters
- Thin 20 & 40 micron substrates for low thermal resistance
- Licensed from Corning

The 3YSZ Suitable for wearable electronics (<100°C, <100V) applications

- **Relative Permittivity**
  - 45 Hz - 20 micron
  - 1000 Hz - 20 micron
  - 10 kHz - 20 micron
  - 100 kHz - 20 micron
  - 1 MHz - 20 micron
  - 1 kHz - 40 micron
  - 10 kHz - 40 micron
  - 100 kHz - 40 micron
  - 1 MHz - 40 micron

- **Leakage Current**
  - 40 micron 3YSZ Leakage Current
  - Voltage
  - Temperature (°C)
  - 25C
  - 75C
  - 125C
  - 175C

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FREEDM SYSTEMS CENTER

PREES Laboratory
NC STATE UNIVERSITY
PACKAGING RESEARCH IN ELECTRONIC ENERGY SYSTEMS
New Thin Organic Dielectrics for Low Cost Modules

Epoxy Resin Composite Dielectrics – ERCDs
These provide an opportunity to look at very low cost modules with embedded components.

“Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao¹, Yifan Jiang¹, Bo Gao¹, Kenji Nishiguchi², Yoshi Fukawa³, D. C. Hopkins¹
¹North Carolina State University, ²Risho Kogyo Co., LTD, ³TOYOTech LLC
State-of-art development of WBG power module

SiC Module w/ double-sided cooling by ORNL[1]:
- 2.6 nH extracted parasitics inductance
- Bus up to 600V with >40A capability
- Kelvin connections implemented
- Gate bonding wire required

SKiN and Direct Pressed Die technology by Semikron[2]:
- >20% thermal resistance reduction
- 10% reduction in parasitic inductance
- >25% improvement in surge current
- Improved thermal-cycling based reliability
- 1700V/1800A
- Challenge on the Press Unit design and implementation

State-of-art development of WBG power module

PowerStack packaging technology by Texas Instruments[3]

- Lower Parasitics between high- and low-side switches
- Improved Power Efficiency
- Better Thermal performance
- Applicable for lower voltage applications for now

- Insulated-Metal-Baseplate based IPM by Mitsubishi [4, 5]
- CTE of insulating resin layer ~17ppm, close to Copper, with better mechanical stress management
- 35% thermal impedance reduction from development of resin
- Less interconnection layers for lower profile, up to 55% size reduction from traditional DBC based module
- Better thermal cycling reliability with less cracks during cycling
- Heavily depends on the resin interface material

Criterion for thin dielectric selection for power module substrate applications

**Target Application:** 1200V / 40A SiC MOSFET and Schottky Diode based Power Module

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Conductivity</td>
<td>W/mK</td>
<td>&gt; 3</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>kV</td>
<td>&gt; 3</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>µA</td>
<td>~ 10</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>1</td>
<td>&lt; 8</td>
</tr>
<tr>
<td>Operation Temperature</td>
<td>ºC</td>
<td>&gt; 175</td>
</tr>
<tr>
<td>Processing Temperature</td>
<td>ºC</td>
<td>&gt; 250</td>
</tr>
</tbody>
</table>

- **Thermal conductivity** need not be high, due to thin dielectric
- **Sufficient breakdown voltage** for adequate margin for 1200V SiC MOSFETs
- **Low leakage current comparable with SiC devices** at the same conditions, such as temperature
- **High temperature** operation similar to SiC devices
- **High processing temperature** to leave margin for assembly processes

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
**Epoxy Resin Composite Dielectric by RISHO**

<table>
<thead>
<tr>
<th>Component</th>
<th>Material Description</th>
<th>Thermal Conductivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper Foil</td>
<td>Dielectric layer (B-stage) (Woven Glass cloth reinforced)</td>
<td></td>
</tr>
<tr>
<td>CCL (CS-XXXX) Cu Clad Laminate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric layer (B-stage)</td>
<td>Aluminum/Copper plate</td>
<td></td>
</tr>
<tr>
<td>(ES-XXXX) Prepreg</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Copper foil</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(AC-XXXX) Metal base CCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Liquid Molding Compound (One-pack type)</td>
<td>(1~4W/mK)</td>
<td></td>
</tr>
<tr>
<td>Liquid Molding Compound (Two-pack type)</td>
<td>(1~7W/mK)</td>
<td></td>
</tr>
<tr>
<td>Al base CCL</td>
<td>AD-7208 8W/mK</td>
<td></td>
</tr>
<tr>
<td>AC-7208 10W/mK</td>
<td>AD-7210 10W/mK</td>
<td></td>
</tr>
<tr>
<td>AC-7210 10W/mK</td>
<td>AD-7210</td>
<td></td>
</tr>
<tr>
<td>AD-7210</td>
<td>AD-7210</td>
<td></td>
</tr>
<tr>
<td>CD-7208 8W/mK</td>
<td>CC-7210 10W/mK</td>
<td></td>
</tr>
<tr>
<td>CD-7210</td>
<td>CD-7210</td>
<td></td>
</tr>
<tr>
<td>CC-7210</td>
<td>CD-7210</td>
<td></td>
</tr>
<tr>
<td>AC-7210</td>
<td>AD-7208 8W/mK</td>
<td></td>
</tr>
<tr>
<td>AD-7208 8W/mK</td>
<td>AD-7210</td>
<td></td>
</tr>
<tr>
<td>CD-7210</td>
<td>CD-7210</td>
<td></td>
</tr>
<tr>
<td>CC-7210</td>
<td>CC-7210</td>
<td></td>
</tr>
</tbody>
</table>

*Bonding sheet, RCC, Copper-base CCL without glass fabric*
Investigating Flexible Thin Dielectric as Substrates

Target Material: Recently developed Epoxy-Resin based dielectric by Risho Kogyo Co., Ltd. – AC-7208

Properties of the Thin Dielectric (measured at 120 µm)

Better Stress Management
- CTE closer to copper than traditional ceramic (4.5 ppm/K ~ 7 ppm/K)
- Flexible allowing for stress release during assembly and service of the module

Investigating Flexible Thin Dielectric as Substrates

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Conductivity</td>
<td>W/mK</td>
<td>8</td>
</tr>
<tr>
<td>Tg</td>
<td>°C</td>
<td>270</td>
</tr>
<tr>
<td>Modulus</td>
<td>GPa</td>
<td>30</td>
</tr>
<tr>
<td>Bending Strength</td>
<td>MPa</td>
<td>94</td>
</tr>
<tr>
<td>CTE</td>
<td>ppm/°C</td>
<td>9/22</td>
</tr>
<tr>
<td>Dk</td>
<td>/</td>
<td>6.3</td>
</tr>
<tr>
<td>Df</td>
<td>/</td>
<td>0.009</td>
</tr>
<tr>
<td>Water Absorption</td>
<td>%</td>
<td>0.27</td>
</tr>
<tr>
<td>Dielectric Strength</td>
<td>kV</td>
<td>5.6 @ 120 µm</td>
</tr>
</tbody>
</table>

Comparable thermal performance with alumina
- Better unit area thermal conductance than alumina
- 1/5 unit area thermal conductance of AlN
- Lower cost for epoxy-resin substrate

<table>
<thead>
<tr>
<th>Parts</th>
<th>Thickness /µm</th>
<th>Thermal Conductivity W/m·K</th>
<th>Unit Thermal Conductance W/m²·°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Epoxy-resin</td>
<td>80</td>
<td>8</td>
<td>0.1E6</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>254</td>
<td>23</td>
<td>0.09E6</td>
</tr>
<tr>
<td>AlN</td>
<td>254</td>
<td>170</td>
<td>0.67E6</td>
</tr>
</tbody>
</table>

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
Epoxy Resin Composite Dielectric

- Capable of bonding with Copper on both sides
- Copper thickness up to $\leq 0.6$ mm
- 80 $\mu$m dielectric thickness is available

Leakage current measured on 80 $\mu$m sample with Cu bonded on both sides
- 20 $\mu$A leakage even at 250 °C with 1200 V voltage applied
- 1 nA leakage at room temperature with $> 4$kV voltage applied

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2$kV / 40$A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
Resource Development for ERCD Topology Research

1. ERCD "substrate-less" approaches identified for high voltage (5kV/120µm), high temperature (≤300ºC) and high thermal impedance (10W/mK).
2. Materials systems for fluid compatibility, multilayering and metal backing for investigation of dense high voltage power module structures.
3. Processes and equipment for ERCD systems identified and ordered through PREES resources.
**ERCD Composition**

**Microstructure of the dielectric at 20,000 magnification**

- O is corresponding to alumina particles, distributed almost everywhere, N is the AlN particles, with limited number, C is from the polymer, Cu is from the bonding interface.
- AlN and alumina particles are also identified by XRD analysis.
- High thermal conductivity is from the widely distributed alumina particles and few AlN particles.

ERCD Breakdown Voltage

Properties during reliability experiments (Thermal aging and thermal cycling)

- Thermal aging is conducted at 150 °C
- Thermal cycling is from -55°C to 125 °C
- Peel strength (35µm copper on 120µm dielectric with 1mm Al) is not as high as DBC interface (4N/mm for 0.3mm Cu on alumina)
- Limited degradation during thermal aging up to 200 Hr in breakdown voltage and peel strength
- The properties do not change much during thermal cycling up to 1000 cycles

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
### AC-7208 (8W/mK)

<table>
<thead>
<tr>
<th>Product number</th>
<th>AC-7208</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric layer thickness</td>
<td>120μm</td>
</tr>
<tr>
<td>Thermal cond. (W/mK)</td>
<td>8</td>
</tr>
<tr>
<td>Laser flash</td>
<td></td>
</tr>
<tr>
<td>Tg(°C)</td>
<td>270</td>
</tr>
<tr>
<td>DMA method</td>
<td></td>
</tr>
<tr>
<td>Peel strength (kN/m)</td>
<td>1.2</td>
</tr>
<tr>
<td>1 oz copper</td>
<td></td>
</tr>
<tr>
<td>Solder limit (sec)</td>
<td>Over 60</td>
</tr>
<tr>
<td>CTE (ppm/°C)</td>
<td>9/22</td>
</tr>
<tr>
<td>Breakdown (kV)</td>
<td>Over 5</td>
</tr>
<tr>
<td>JIS C2110</td>
<td></td>
</tr>
<tr>
<td>CTI</td>
<td>Over 600</td>
</tr>
<tr>
<td>IEC method</td>
<td></td>
</tr>
<tr>
<td>Flammability</td>
<td>V-0equiv.</td>
</tr>
<tr>
<td>UL94</td>
<td></td>
</tr>
</tbody>
</table>

#### High temperature long term test (@175°C)

<table>
<thead>
<tr>
<th>Time (Hr)</th>
<th>Breakdown (kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1000</td>
<td>0</td>
</tr>
<tr>
<td>3000</td>
<td>0</td>
</tr>
<tr>
<td>5000</td>
<td>0</td>
</tr>
</tbody>
</table>

#### Thermal cycle test (-40⇒125°C)

<table>
<thead>
<tr>
<th>Cycle number</th>
<th>Breakdown (kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>500</td>
<td>0</td>
</tr>
<tr>
<td>1000</td>
<td>0</td>
</tr>
<tr>
<td>1500</td>
<td>0</td>
</tr>
<tr>
<td>2000</td>
<td>0</td>
</tr>
<tr>
<td>2500</td>
<td>0</td>
</tr>
<tr>
<td>3000</td>
<td>0</td>
</tr>
<tr>
<td>3500</td>
<td>0</td>
</tr>
</tbody>
</table>

After long term test at 175°C and thermal cycle test, there is no problem in breakdown voltage and peel strength. → This material also shows high reliability.
**AC-7210 (10W/mK)**

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product number</td>
<td>AC-7210</td>
</tr>
<tr>
<td>Dielectric layer thickness</td>
<td>120μm</td>
</tr>
<tr>
<td>Thermal cond. (W/mK)</td>
<td>10</td>
</tr>
<tr>
<td>Tg(℃)</td>
<td>270</td>
</tr>
<tr>
<td>Peel strength (kN/m)</td>
<td>1.2</td>
</tr>
<tr>
<td>Solder limit (sec)</td>
<td>60&lt;</td>
</tr>
<tr>
<td>CTE (ppm/℃)α1</td>
<td>14/14/14</td>
</tr>
<tr>
<td>Breakdown voltage (kV)</td>
<td>5&lt;</td>
</tr>
<tr>
<td>CTI</td>
<td>600&lt;</td>
</tr>
<tr>
<td>Flammability</td>
<td>V-0 equivalent</td>
</tr>
</tbody>
</table>

**HIGH TEMPERATURE LONG TERM RELIABILITY (175 ℃)**

![Graph showing Breakdown voltage vs. Treating time](image)

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DCHopkins@NCSU.edu

www.PREES.org

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High Heat resistance CCL for Power Modules

Low CTE and high heat resistance material
CS-3305A (CCL)
ES-3310A (Prepreg)

Ultra-thin thickness (15μm of 1ply type or 30μm of 2ply type)
## General properties of CS-3305A series

<table>
<thead>
<tr>
<th>Item</th>
<th>Unit</th>
<th>CS-3305A (E-glass)</th>
<th>CS-3305AS (Low CTE glass)</th>
<th>CS-3305AQ (Quartz glass)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CTE</strong> (Other Low CTE glass fabric enables lower CTE)**</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Y  α₁ ppm</td>
<td></td>
<td>6~8</td>
<td>2~4</td>
<td>0.5~1</td>
</tr>
<tr>
<td>X  α₁ ppm</td>
<td></td>
<td>6~8</td>
<td>2~4</td>
<td>0.5~1</td>
</tr>
<tr>
<td>Z  α₁ ppm</td>
<td></td>
<td>10~15</td>
<td>10~15</td>
<td>10~15</td>
</tr>
<tr>
<td><strong>Glass transition Temperature (Tg)</strong> DMA</td>
<td>°C</td>
<td></td>
<td>Over 300°C</td>
<td></td>
</tr>
<tr>
<td><strong>Water absorption ratio</strong> %</td>
<td></td>
<td></td>
<td>0.13</td>
<td></td>
</tr>
<tr>
<td><strong>Flexural strength (Y-axis)</strong> 25°C MPa</td>
<td></td>
<td>517</td>
<td>660</td>
<td>446</td>
</tr>
<tr>
<td>250°C MPa</td>
<td></td>
<td>415</td>
<td>470</td>
<td>356</td>
</tr>
<tr>
<td><strong>Flexural modulus (Y-axis)</strong> 25°C GPa</td>
<td></td>
<td>32</td>
<td>35</td>
<td>32</td>
</tr>
<tr>
<td>250°C GPa</td>
<td></td>
<td>16</td>
<td>19</td>
<td>19</td>
</tr>
<tr>
<td><strong>Peel strength (Copper) KN/m</strong></td>
<td></td>
<td></td>
<td>0.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>[VLP 1/3oz]</td>
<td></td>
</tr>
<tr>
<td><strong>Solder heat resistance(300°C)</strong> Sec.</td>
<td></td>
<td></td>
<td>over300</td>
<td></td>
</tr>
</tbody>
</table>
High Tg and high modulus by DMA method

- There is no \( \tan\delta \) peak of CS-3305A \( \rightarrow \) Tg : over 300°C
- Storage modulus maintains higher than the other material under the high temperature.
Thermal decomposition temperature by TGA method

CS-3305A is a long term heat resistance material.

Atmosphere: Air
Heating rate: 10°C/min
Reference: Al₂O₃

<table>
<thead>
<tr>
<th></th>
<th>CS-3305A</th>
<th>Standard FR-4.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Td(1%)</td>
<td>352°C</td>
<td>277°C</td>
</tr>
<tr>
<td>Td(5%)</td>
<td>487°C</td>
<td>310°C</td>
</tr>
</tbody>
</table>
Retention of peel strength of copper foil

- Delamination between copper foil and dielectric layer of standard FR-4.0 was occurred at 175°C.

- CS-3305A maintained peel strength at 175 and 200°C even after 3000 hours treatment.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>CS-3305A</th>
<th>Std FR-4.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>175°C</td>
<td>1.30kN/m</td>
<td>1.60kN/m</td>
</tr>
<tr>
<td>1500hr. (Retention)</td>
<td>1.27kN/m (98 %)</td>
<td>1.28kN/m (80 %)</td>
</tr>
<tr>
<td>3000hr. (Retention)</td>
<td>1.26kN/m (97 %)</td>
<td>0.99kN/m (62 %)</td>
</tr>
</tbody>
</table>
650Vdc/20A ½-bridge IPM based on RISHO Substrate

From: PowerAmerica Short Course Nov 2018
Raleigh, NC
650Vdc/20A ½-bridge IPM based on RISHO Substrate

Parameters:
- 650V maximum DC bus voltage
- 20A maximum RMS current per device
- 400V→200V Half-bridge buck
- Internal decoupling cap

IDEAL: Simulation condition: 10A, 100pF $C_{\text{oss}}$

Overshoot w/o decoupling cap
- 240V @100nH
- 7V @5nH

Overshoot w decoupling cap
- 7V @5nH

Parts:
- Q1 Q2: Ideal
- C1 C2: 10uF 25V X7R
- C3: 47nF 1kV X7R
- R1: 22Ohm 1/8W
- D1: Ideal HF diode
- U1: Ideal isolated HB driver
**Thermal Analysis**

Thermal analysis w/ first order estimation of losses:

\[ P_{\text{rds}} = 129m \times 20A^2 = 51.6W \text{ @ } Tj_{\text{max}}=150^\circ C \]

\[ P_{\text{sw}} = 55uJ \times 0.5MHz = 27.5W \text{ @ } 400V, 15A \]

\[ P_{\text{tot}} = P_{\text{rds}} + P_{\text{sw}} = 79.1W \]

Given:

- Die Pad = 6mm X 3mm,
- ERCD Substrate thickness = 80µm,
- Al case thickness = 0.9mm:

Approximating with 45º rule:

\[ A_{\text{sub}} = (6mm + 0.04mm) \times (3mm + 0.04mm) = 18.4mm^2 \]

\[ A_{\text{case}} = (6mm + 0.04mm + 0.9mm) \times (3mm + 0.04mm + 0.9mm) = 27.3mm^2 \]

\[ R_{\text{sub}} = \frac{0.08mm}{18.4mm^2} \times \frac{1000}{(10W/m^\circ C)} = 0.43 \, ^\circ C /W \]

\[ R_{\text{case}} = \frac{0.9mm}{27.3mm^2} \times \frac{1000}{(205W/m \, ^\circ C)} = 0.16 \, ^\circ C /W \]

\[ R_{\text{total}} = R_{\text{chip}} + R_{\text{sub}} + R_{\text{case}} = 0.5\, ^\circ C /W + 0.43\, ^\circ C /W + 0.16\, ^\circ C /W = 1.09\, ^\circ C /W \]

At \( P = 56.5W \), \( T_{\text{case}} = 40^\circ C \), \( T_j = 40^\circ C + 79.1W \times 1.09\, ^\circ C /W = 126.2^\circ C, < Tj_{\text{max}} = 150^\circ C \)

Thank you to sponsors:
Inductance estimation:
1. Power loop: 6.5nH using rectangle estimation
2. Gate loop: 3.8nH using rectangle estimation

For optimal gate driver at Q=1.5 (0.3V overshoot):
\[ R = (L/C)^{-1/2} / Q = 2.5 \, \Omega, \quad L = 3.8nH, \quad C = C_{iss} = 0.26nF \]

Gate driver has \( R_{out} = 2.7\Omega > 2.5 \), therefore no \( R_{ext} \) is required. Then, simulation shows only 0.26V gate overshoot, well within GaN ratings.

Thank you to GaN Systems, Risho and Electronic Interconnect for supplying parts and processing.
**Buck converter with Q1 as switch and Q2 as sync rect.**

Full SPICE simulation at 400V->200V 20A:

\[ L_{\text{pwr-loop}} = 6.5 \text{ nH} \]
\[ L_{\text{gate-loop}} = 3.8 \text{ nH} \]
\[ C_{\text{substrate cap}} = 28.9 \text{ pF (parallel plate method)} \]
\[ R_{\text{heatsink}} = 10\Omega \text{ sink-to-Q}_{\text{source}} \]

Results:

\[ P_{\text{loss}} = 42.5W \text{ for Q1, } T_j=86.3\text{C} \]
\[ P_{\text{loss}} = 15.8W \text{ for Q2, } T_j=57.2\text{C} \]

Switching \( V_{DS} \) waveform shows 70 overshoot above the 400V

---

**Parts:**

- Q1 Q2: GS66508B
- C1 C2: 10uF 25V X7R
- C3: 47nF 1kV X7R
- R1: 22Ohm 1/8W
- D1: CURN101-HF diode
- U1: Si8274 isolated HB driver
- Bottom-side cooled 650V
- E-mode GaN Systems
SiC Integrated Power Module Test Design

Excerpt from: Xin Zhao\cite{1} Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

[1] Now at Univ. of Texas at Austin
Double Sided Design

Substrates on Double Side

- Volume: 35 mm × 15.5 mm × 3mm
- Power Devices: CPM2-1200-0025B / CPW5-1200-Z050B
- Rating: 800 V/ 40 A
- Auxiliary terminals on single side of the module, allowing for both side heat sink attachment, with terminals able to attached on PCB for interconnections

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
SiC IPM Design

Circuit Schematic Design

Schematic Design for SiC half bridge IPM
- Bootstrap Power Supply
- Digital Isolator
- LDO
- Gate driver Circuits
- -5V turn-off power supply
- Single switch pair IPM is developed as initial investigation

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
Simulation of the SiC IPM Design

Simulation for Parasitic Extraction

- Inductance in the entire loop is 0.6 nH.
- Diode inductance is larger, since it parallels the MOSFET drain to source.
- Applicable for lower losses and higher operation frequency.

Current distribution in the power loop

Summary of extracted parasitics

<table>
<thead>
<tr>
<th>Location</th>
<th>Inductance / nH</th>
<th>Resistance / mΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC+ → DC-</td>
<td>0.6</td>
<td>0.22</td>
</tr>
<tr>
<td>MOSFET Drain</td>
<td>0.44</td>
<td>0.20</td>
</tr>
<tr>
<td>MOSFET Source</td>
<td>0.20</td>
<td>0.10</td>
</tr>
<tr>
<td>Diode Anode</td>
<td>1.87</td>
<td>0.38</td>
</tr>
<tr>
<td>Diode Cathode</td>
<td>2.23</td>
<td>0.46</td>
</tr>
</tbody>
</table>

From Xin Zhao Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018
SiC-IPM Layout

Circuit Layout Design

Layout design for the SiC half bridge IPM

- Interconnections are applied to both top and bottom side of substrates
- Interconnection metal in the main power loop is a compromise between thermal spreading and EMI noise reduction
- Only the layout (c) and (d) are discussed in the presentation for the single switch module
- The layout design is not optimized and the long gate loop trace on the plane, results in excessive noise during switching
- Jumper wire minimizes gate loop length during the fabrication for demonstration of the design

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The forward and reverse characteristics of SiC MOSFET is similar with data shown on the datasheet[7].

The proposed module fabrication and assembly process, including the topside metallization process of SiC devices, can fully exhibits the initial performance of the SiC devices.

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SiC IPM Fabrications & Measurements

Module Assembly & Driver Circuits Test

- Flip-chip assembly for SiC MOSFET and Diode
- Underfill applied for 1200V isolation
- Large terminals for testing

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Conclusions

• Selection Criterion of Thin dielectric substrate material is set up based on design requirements of 1200V WBG device based IPMs.
• A 120µm recently developed flexible epoxy-resin based dielectric, by Risho Kogyo Co., Ltd., is investigated, and proved to be suitable for power module substrate in terms of electrical, thermal, mechanical properties, cost, and reliability.
• A high-density half-bridge SiC power module is designed with ultra-low parasitics, utilizing epoxy-resin based dielectric, for high-frequency and low-loss applications.
• Fabrication process of double-side solderable SiC MOSFETs and diodes is developed, capable of deposition of metallization layer up to 2µm.
• A single-switch SiC power module with more functionality is fabricated, allowing for double-side cooling functions, verified by static measurements.
• The proposed substrate material, and designed WBG IPM with ultra-low parasitics, high functionality and double-side cooling is verified and show potential for high frequency and high power density applications.

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End

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