FREEDM SYSTEM CENTER
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Duke Energy Hall, Hunt Library

Trends in Power Electronics Packaging

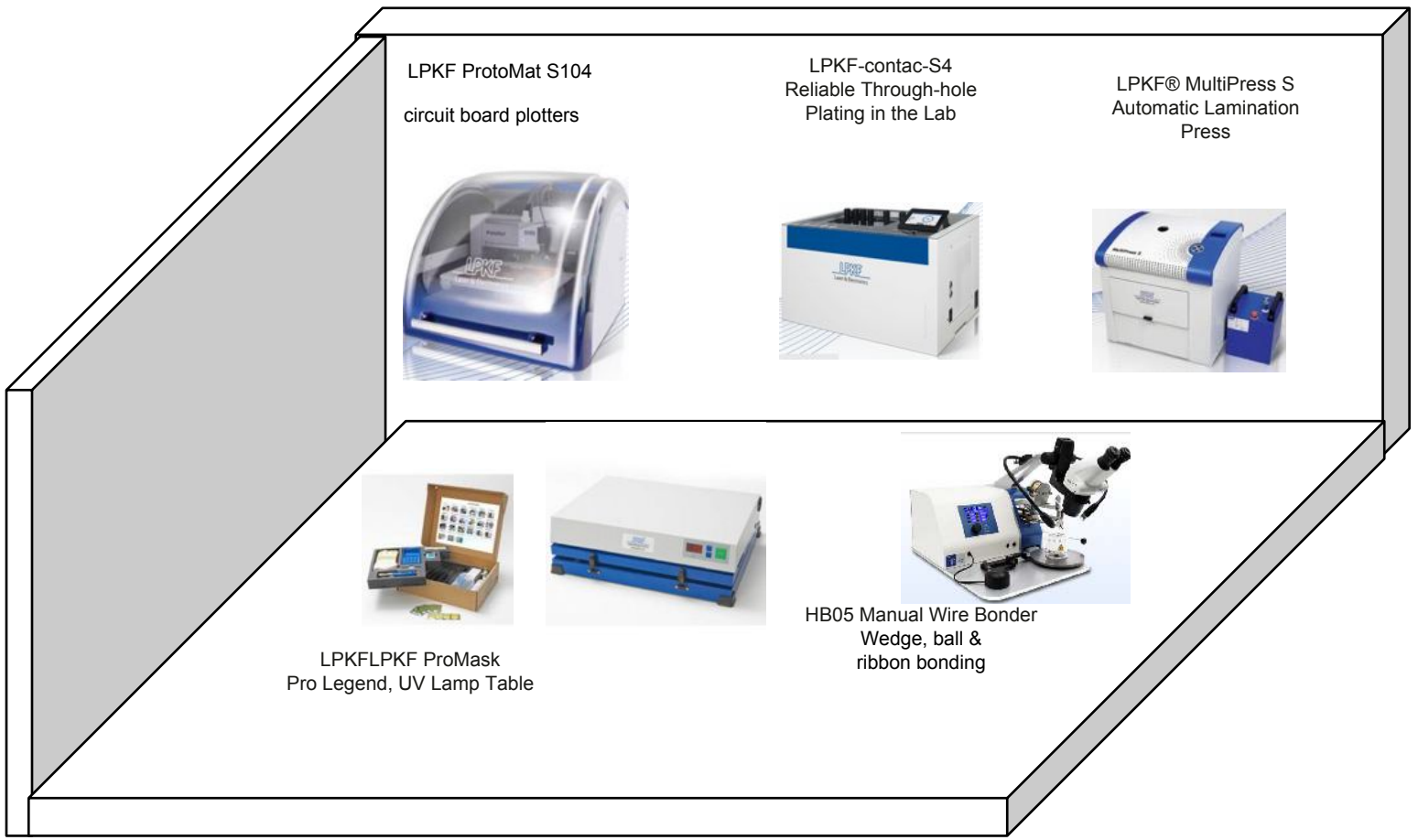
Prof Douglas C. Hopkins, Ph.D.

Director – PREES Laboratory
FREEDM System Center
North Carolina State Univ.
1791 Varsity Dr., Suite 100
Raleigh, NC 27606-7571
919-513-5929
DCHopkins@NCSU.Edu
www.prees.org

New Resource for ERCD Ckt Topology Research

Epoxy Resin Composite Dielectrics (ERCD)

ERCD ”substrate-less” approaches identified for high voltage (5kV/120µm), high temperature (≤300ºC) and high thermal impedance (10W/mK)



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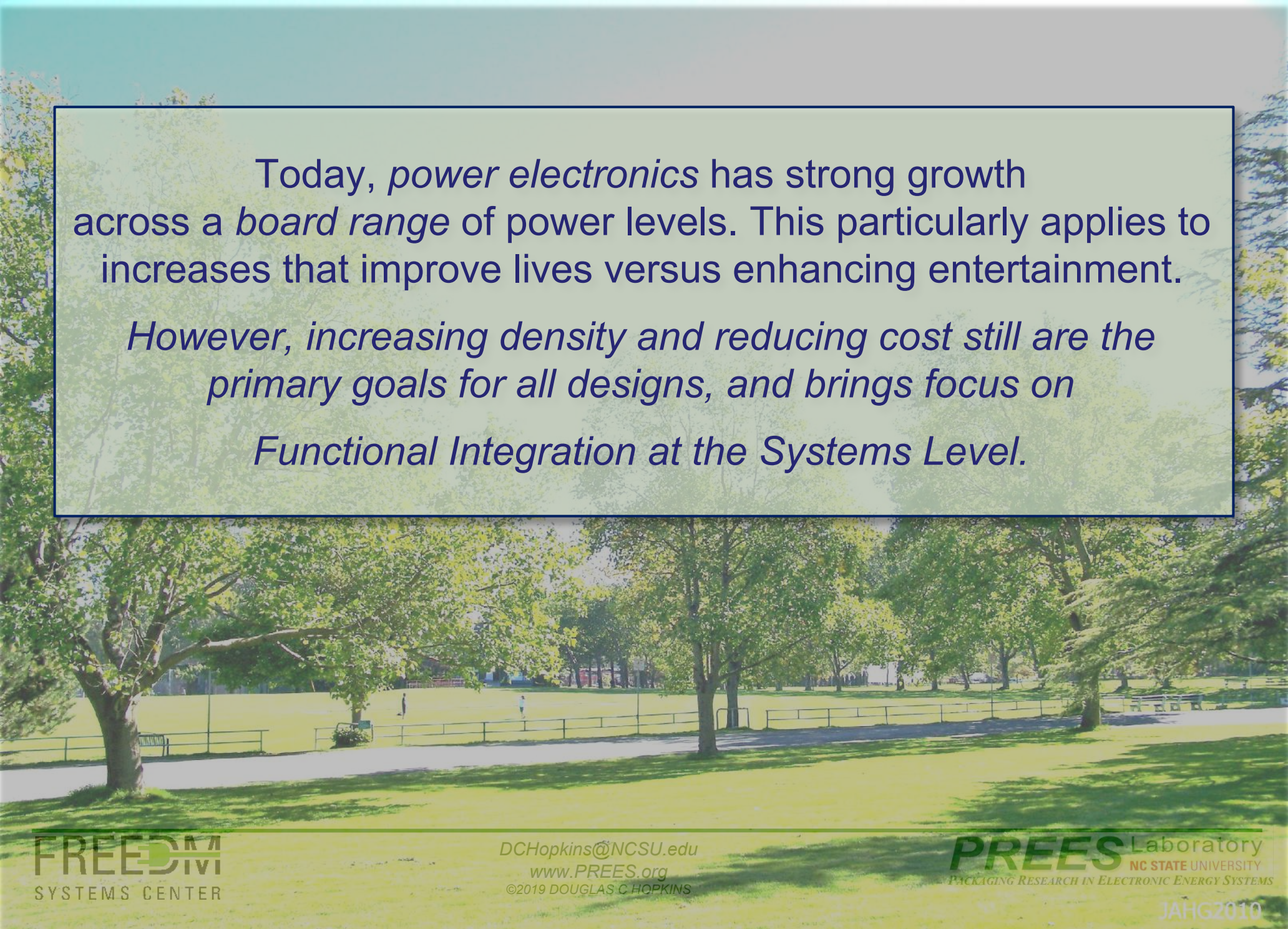

Today, *power electronics* has strong growth across a *board range* of power levels. This particularly applies to increases that improve lives versus enhancing entertainment.

However, increasing density and reducing cost still are the primary goals for all designs, and brings focus on

Functional Integration at the Systems Level.

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Problem?… much smaller WBG devices

The challenge in thermal management will broaden to address essentially point-source heat generation due to higher power capabilities with shrinking die size …compared to Si die.

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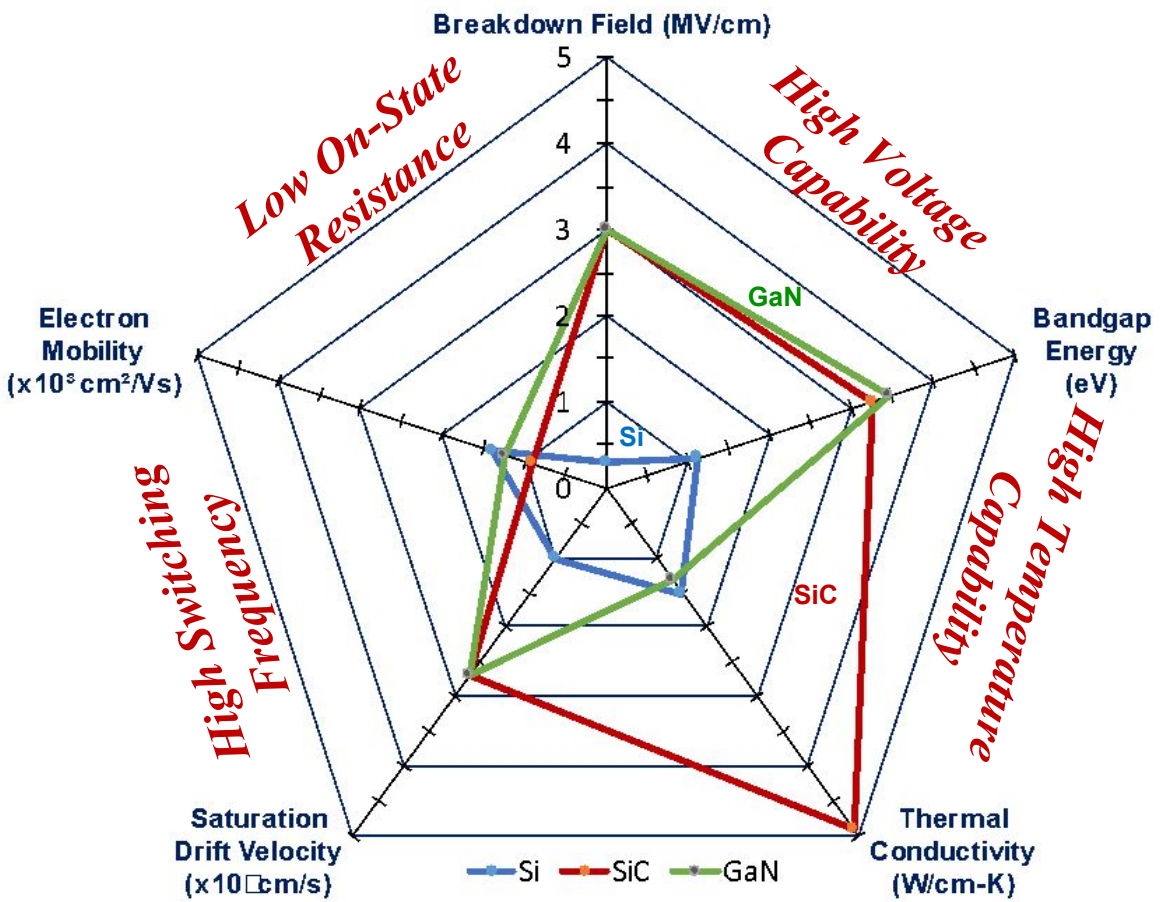
Shrinking power die challenge



Huang in 2004 developed three pertinent figures of merit [1].

E_c is critical electric breakdown field,
μ is electron mobility,
ε is dielectric constant,
σ_{th} is thermal conductivity

[1] "New Unipolar Switching Power Device Figures of Merit," Alex Q. Huang, IEEE Electron Device Letters, Vol. 25, No. 5, May 2004

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Shrinking Die Size (so to speak)

Losses Die size $R_{th,die}$

TABLE I
COMPARISON OF VARIOUS SEMICONDUCTOR MATERIALS BASED ON THE NEW HMFOM, HCAFOM, AND HTFOM (NORMALIZED AGAINST SILICON)

Semiconductor Materials	Electron mobility μ (cm^2/V-s)	Relative dielectric constant ε	Critical field E_c (kV/cm)	Thermal conductivity σ_{th} (W/m-K)	HMFOM= $E_C\sqrt{\mu}$	HCAFOM= $\varepsilon E_C^2\sqrt{\mu}$	HTFOM= $\frac{\sigma_{th}}{\varepsilon E_C}$
GaAs	8,500	13.1	400	55	3.3	4.9	0.3
GaN	900	9	3,000	110	8.0	61.7	0.1
Ge	3,900	16	100	58	0.6	0.3	1.0
Si	1,400	11.7	300	130	1	1.0	1.0
GaP	250	11.1	1,000	110	1.4	4.5	0.3
SiC(6H,α)	330	9.66	2,400	700	3.9	25.7	0.8
SiC(4H,α)	700	9.7	3,180	700	7.5	65.9	0.6
Diamond	2200	5.7	5,700	2000	23.8	220.5	1.7

- The FOM for GaN & SiC show substantial performance as die size can shrink, OR the power rating increases.
- Small die are preferred for higher and higher frequencies.

E_c: critical field
μ: mobility
ε: dielectric constant
σ: thermal conductivity

"New Unipolar Switching Power Device Figures of Merit," Alex Q. Huang, IEEE Electron Device Letters, Vol. 25, No. 5, May 2004.

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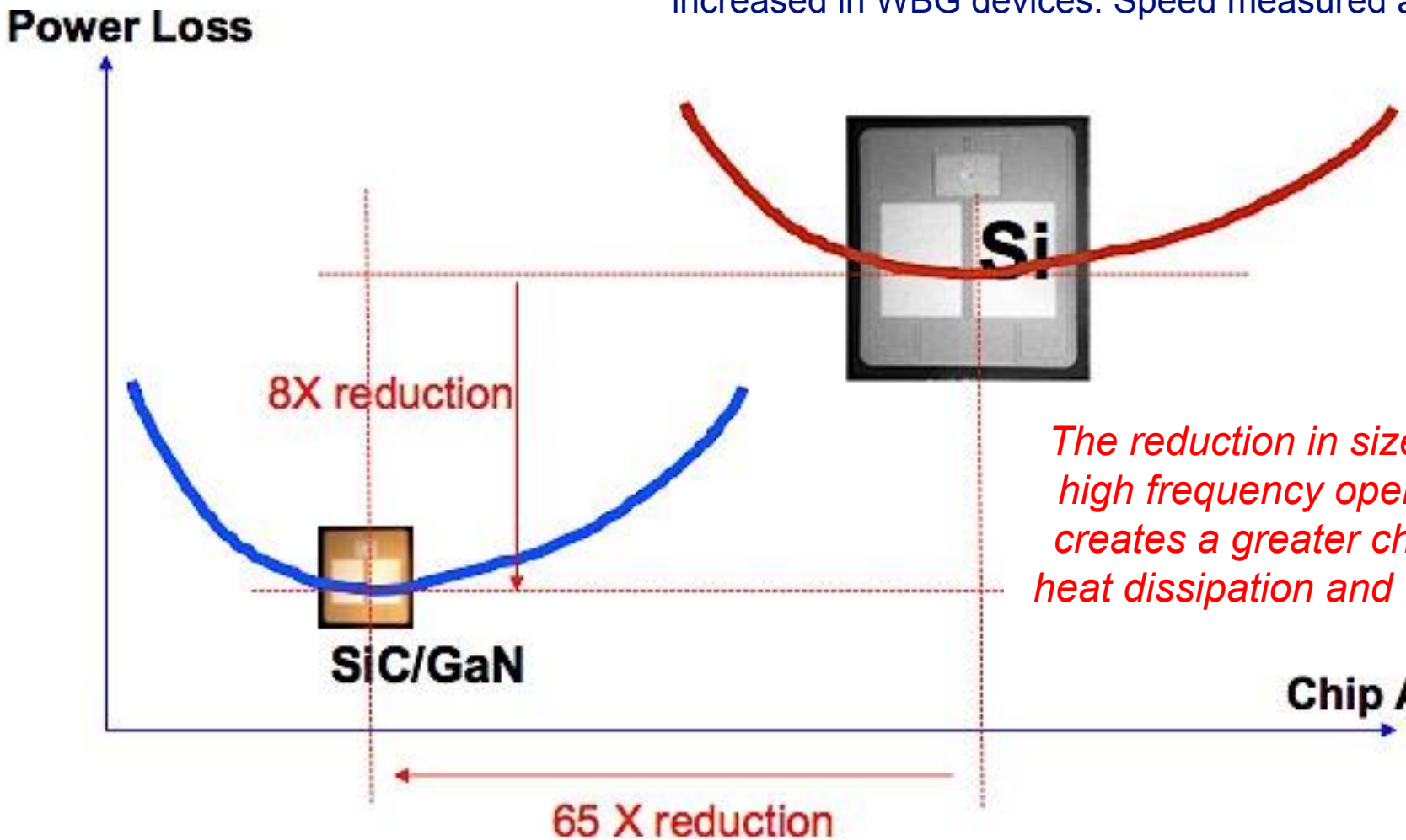
High Frequency Potential (e.g. Unipolar - MOSFET)

Since current does not scale, the speed ~ *i/c*, is significantly increased in WBG devices. Speed measured as *di/dt* or *dv/dt*



The reduction in size supports high frequency operation, but creates a greater challenge in heat dissipation and Integration.

Graph excerpt w/ permission, A. Q. Huang, "Wide Bandgap Power Devices: Die Size Shrinking and Its Impact on Power Delivery Architecture," PSMA Webinar,Feb25,2016

Comparison is based on hard switched converters with fixed f, I, and V. ZVS for high voltage provides other advantages for SiC.

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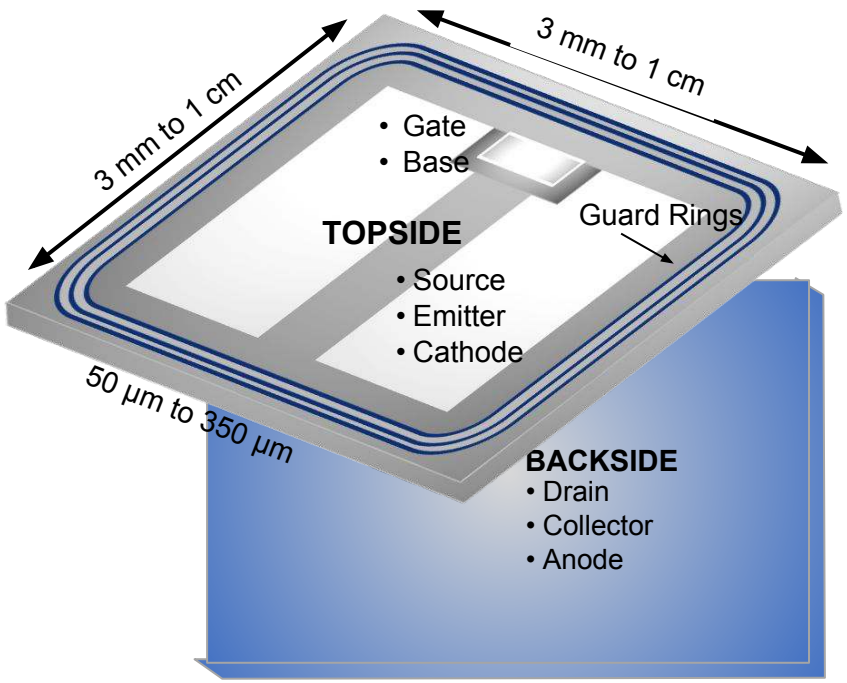
Small Die for High Voltage – 9kV design in air

Packaging materials have always needed to passivate the chip for voltages greater than ~150V.

THE THOUGHT METRIC



Small Die experiences breakdown at 1,800 V. (Experimental design at NCSU)

VIDEO

A great emphasis to develop “Medium Voltage” power electronic systems is underway for large and small systems, e.g. portable x-ray equipment to large autonomous trucks.

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The 'Ground-Baseplate' Problem in Packaging

It's all about vertically conducting devices

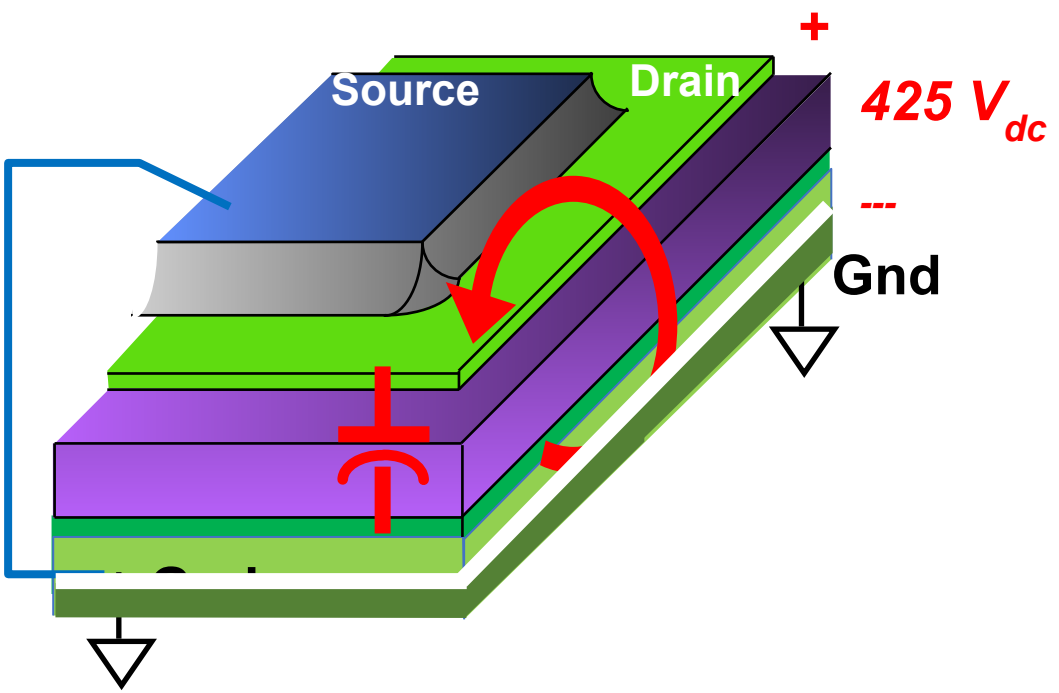
Ground Coupling

Review of mid-point voltage…

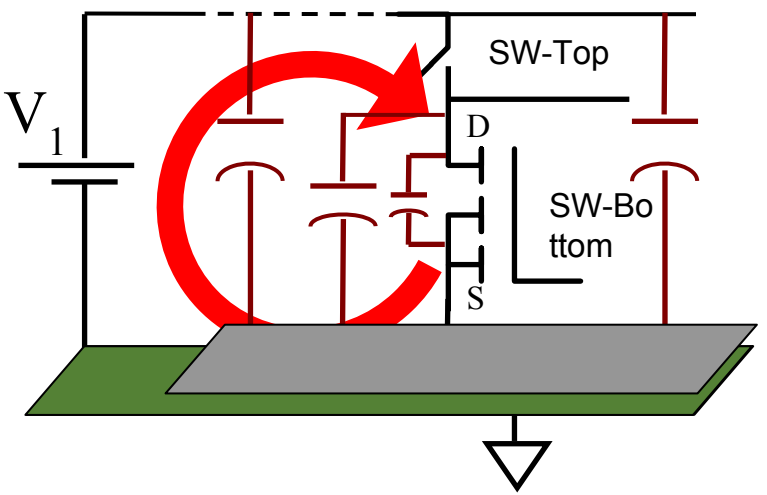
However, there is a major current path when SW-Top turns on.

What is the problem?

$$i = C\,(dV/dt)$$



Ex: V_1: 425 V_{dc} dt: 20ns



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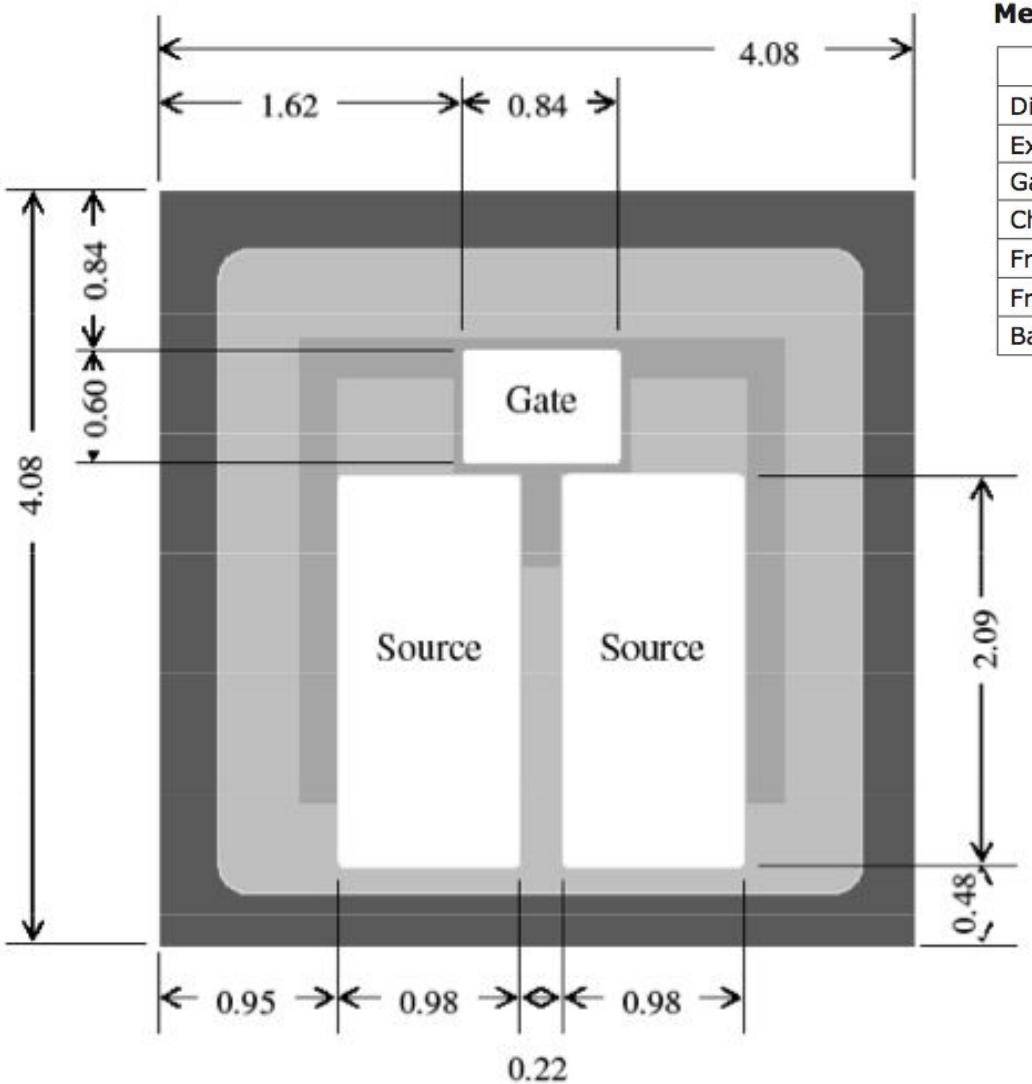
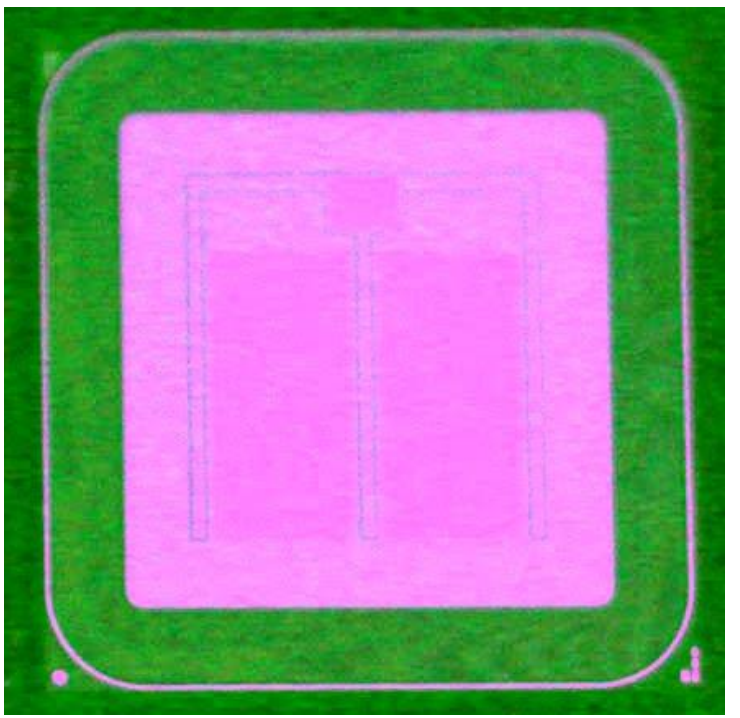
SiC MOSFET Chip Dimensions (used later also)



Mechanical Parameters CPMF-1200-S080B

Parameter	Typ	Unit
Die Dimensions (L x W)	4.08 x 4.08	mm
Exposed Source Pad Metal Dimensions	0.98 x 2.09 (x 2)	mm
Gate Pad Dimensions	0.84 x 0.60	mm
Chip Thickness	365 ± 40	µm
Frontside (Source) metallization (Al)	4	µm
Frontside (Gate) metallization (Al)	4	µm
Backside (Drain) metallization (Ni/Ag)	0.8 / 0.6	µm



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Ground Coupling (continued)

What current flows into 'ground' from the transistor drain?

Given:

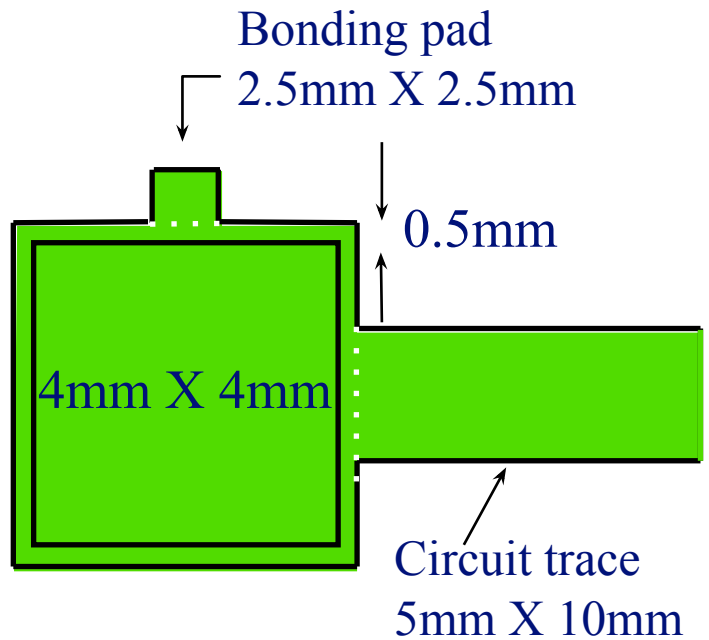
FET: Minimum drain area of semiconductor and solder is 4.5mm X 4.5mm = 20.25mm^2

+ bonding pad 2.5 X 2.5mm = 6.25mm^2

+ circuit trace is 5mm X 10mm = 50mm^2

Substrate:

Al_2O_3 (with ε_r = 9.4) at 635μm thick



Find switching current:

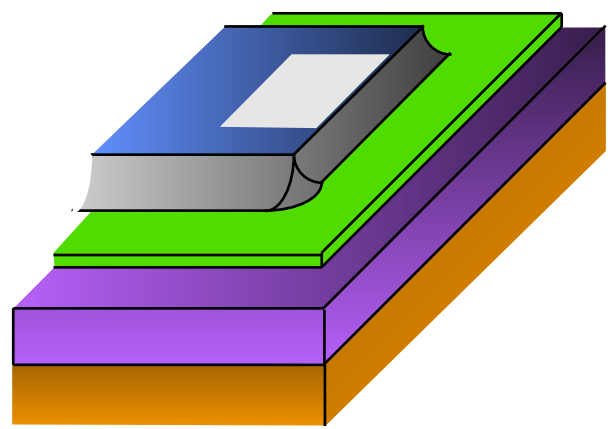
Area, A = 20.25+6.25+50 = 76.5 mm^2

Distance: d = 0.635 mm

Capacitance, $C=\varepsilon_r \varepsilon_o A / d = 10$ pF

$i = C\,(dV/dt) = 10$ pF (425/20ns)

$i = 0.21$ A



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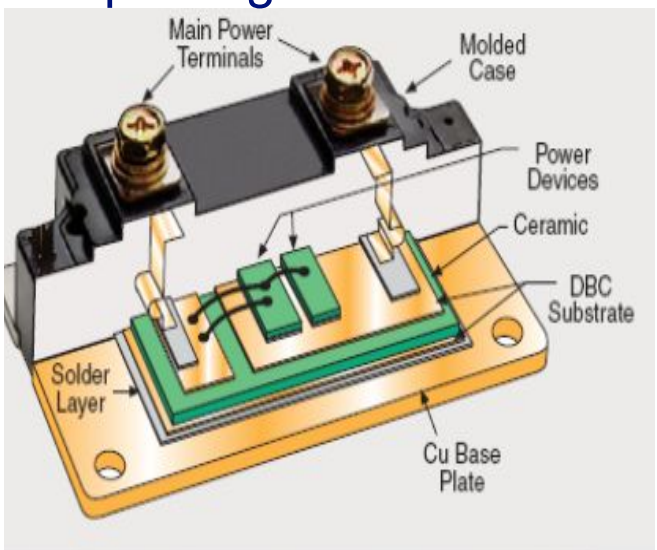
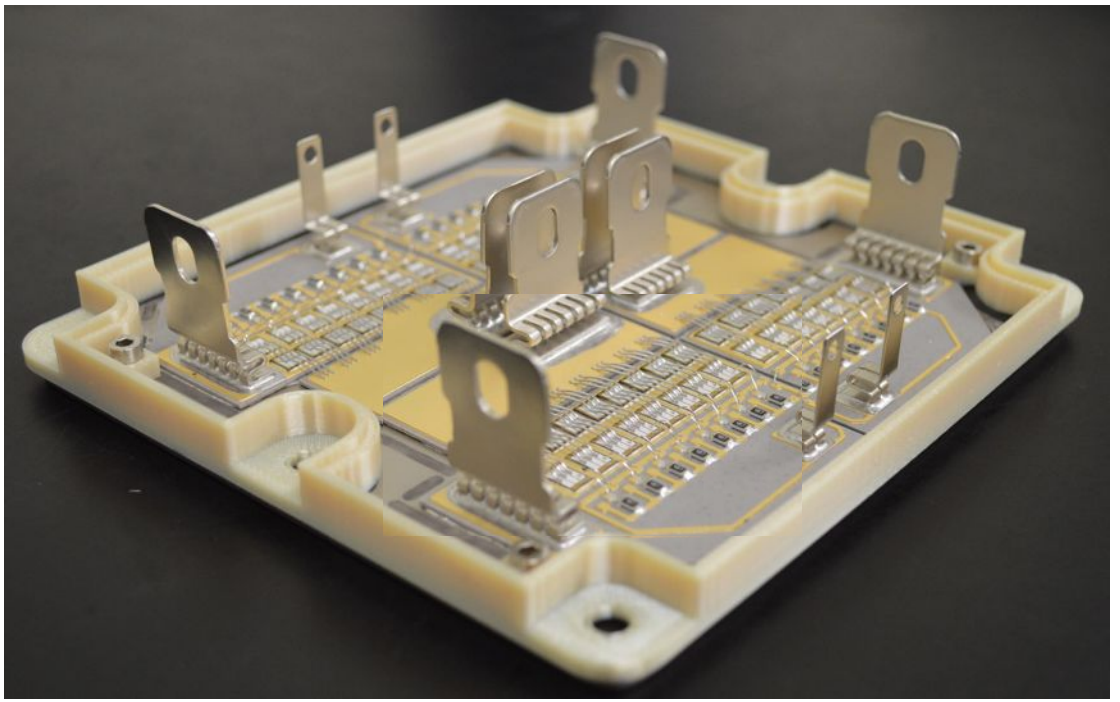
Multi-die Modules

Add diode and space: X2.2,
Multiply by die in parallel: X8,
(Add terminal footprint)
Then,
$i_T = 0.21 \text{ X } 2.2 \text{ X } 9 = 4.2A@20ns$
(For one side)

Standard packages add even more



Low Inductance Power Module with Blade Connector, Ljubisa D. Stevanovic, Richard A. Beaupre, Eladio C. Delgado, and Arun V. Gowda



Courtesy: MS Kennedy 1200V/1200A

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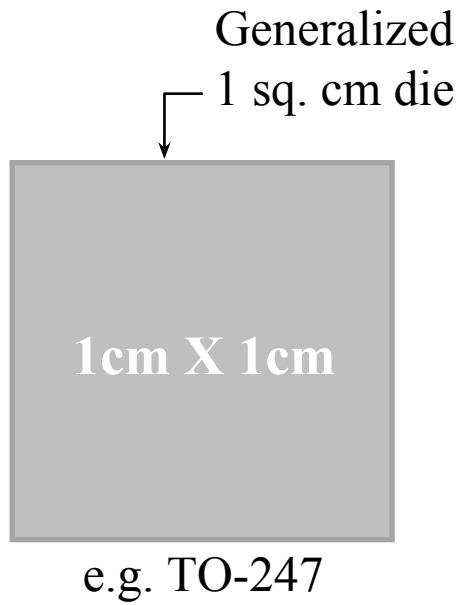
High Voltage Capacitive Current

Switching >10kV can occur at 125kV/μs[1]



For a generalized SiC die of 1cm X 1cm

Use a 40mil (1.02mm) thick AlN ceramic

$\varepsilon_r = 8.6$, $\varepsilon_o = 8.85 \times 10^{-12}$ F/m

The Capacitance, $C = \varepsilon_r \varepsilon_o A / d$

$A = 10^{-4}\ m^2$, $d = 10^{-3} m$

$\therefore C = 7.6$ pF, "per sq. cm"

Find switching current at 10kV & 125 kV/μs:

$i = C\ (dV/dt) = 7.6$ pF $(125$kV/μs$)$

$i = 0.95$ A "per sq. cm"

For multiple dies and diodes use X19.8

Or $i = 18.8$A

[1] "Medium Voltage Power Switch Based on SiC JFETs Xueqing Li, Shirley Zhang, Peter Alexandrov, and Anup Bhalla ," IEEE-APEC 2015, Long Beach CA, Mar 21-25, 2016

DCHopkins@NCSU.edu
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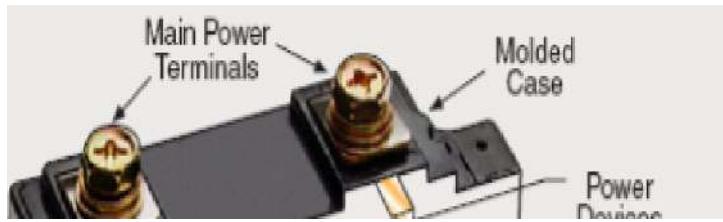
Thermal performance of metal clad ceramics

Rth [˚C/W] for 5mmX5mm SiC on 12/25/12 DBC

Part	Width (mm)	Length (mm)	Thickness (mm)
Device	5	5	0.36
Solder	5.1	5.1	0.05
Metal	5.7	5.7	0.3
Ceramic	6.97	6.97	0.635
Metal	7.57	7.57	0.3
Solder	7.67	7.67	0.05
AlSiC	13.67	13.67	3

COMSOL	Value
Heat Flux (W)	100
Bottom Plate Temperature	293˚K
Mesh	Fine



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3D Prismatic Packaging – True 3D

Dissertation work of Dr. Haotao Ke, September 2017

"3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules"

DCHopkins@NCSU.edu
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State of Art Works

Planar 2D power packaging technology

- Flex circuit structure
  - POL package, SKiN package, etc.
- Embedded structure
  - AT&S GaNPX, PCB embedded, etc.
- Sandwiched structure
  - Planar Bond All package, etc.

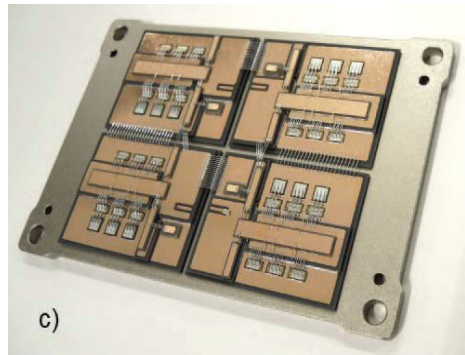
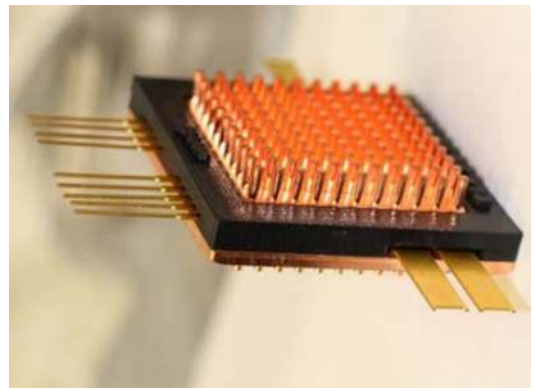
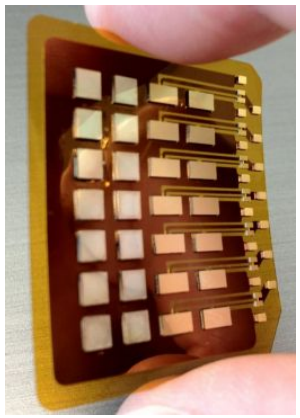


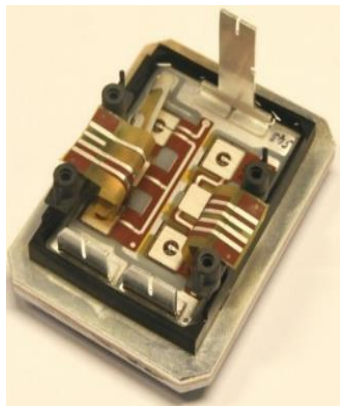
ABB Stacked DBC [1]



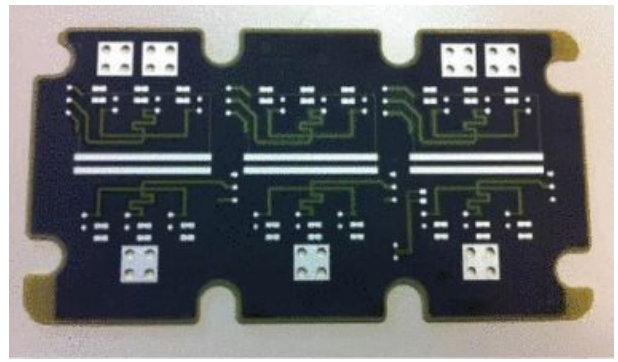
Planar Bond All[8]



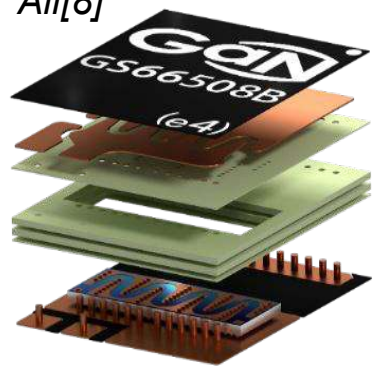
Power Overlay package [4]



SKiN module [5]



PCB embedded module[6]



GaNPX package[7]

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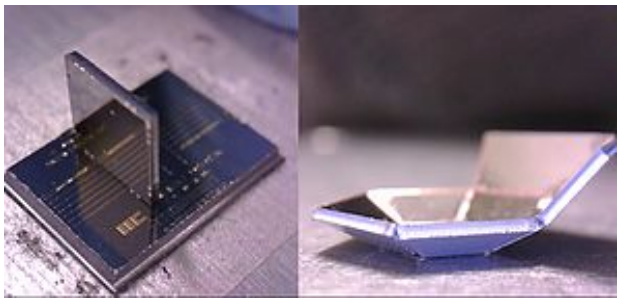
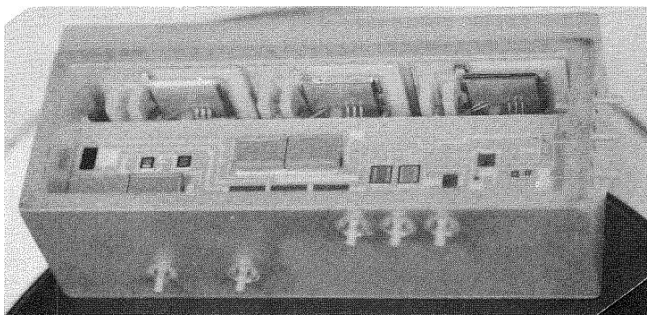
State of Art Works

3D power packaging technology

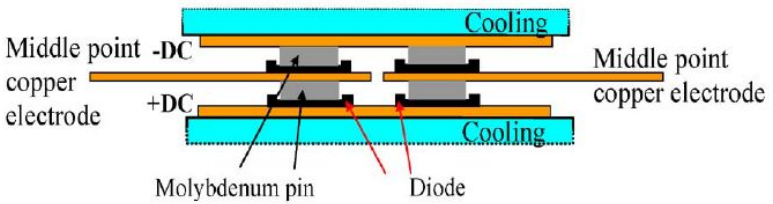
- Device level
  - Quilt dies, stacked / vertical dies
- Module level
  - 3D CSP, Power chip on chip, 3D power circuit .



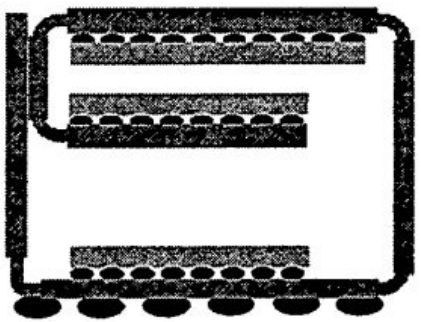
Quilt packaging[9]



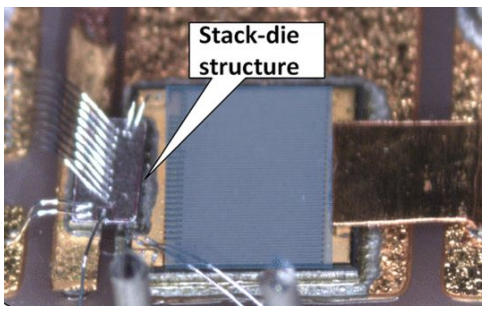
3D Power module[10]



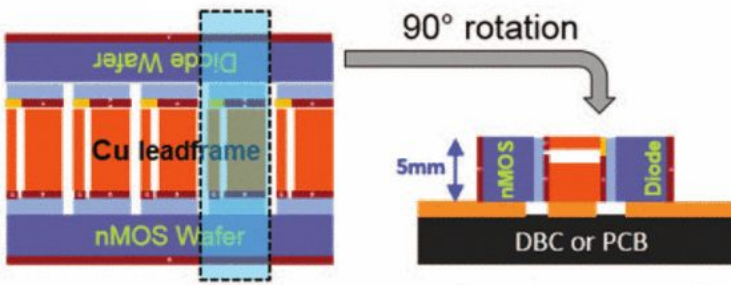
Power chip on chip[11]



3D CSP module[12]



Stacked device[13]



Vertical connected device[14]

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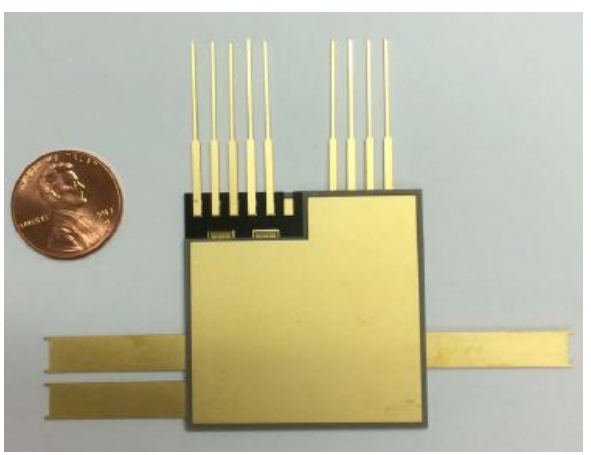
3-D Prismatic Package

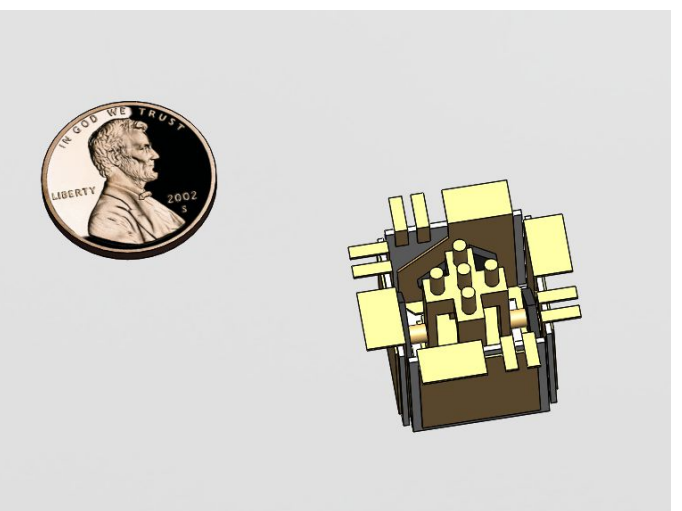
Objective

- Investigation of power module topologies in >2D

3-D Prismatic package should have:

- Low parasitic inductance
- Good thermal performance
- High power density
- Capability to handle thermal stress brought by high temperature operation, if properly designed





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The 3D Power Path Concept

Low inductance is desired for WBG module

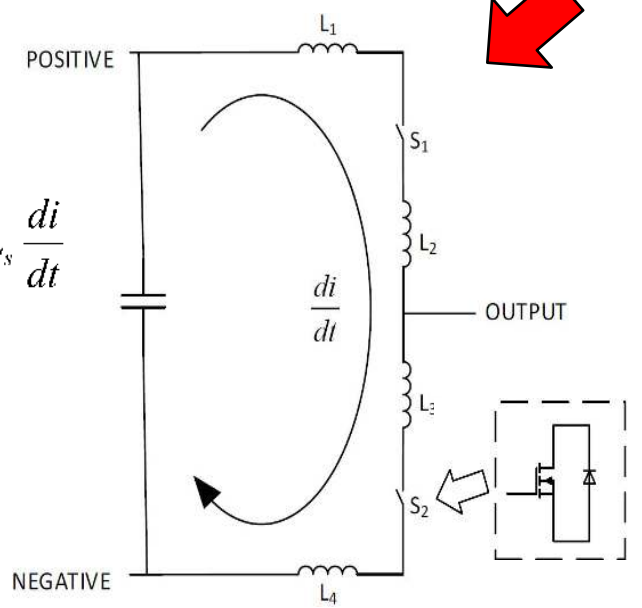
- Minimize voltage overshoot
- Reduce switching loss

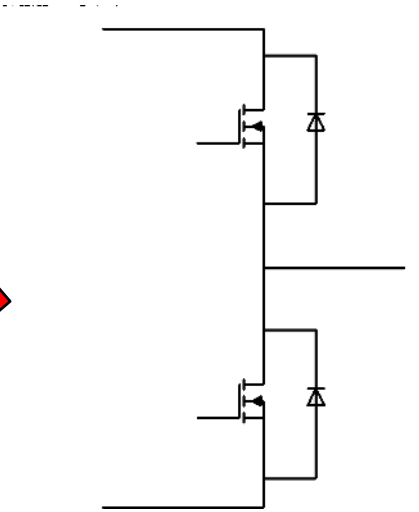
$$L = \begin{bmatrix} L_1 & & & \\ & L_2 & & \\ & & L_3 & \\ & & & L_4 \end{bmatrix}$$

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_1 & & & \\ & L_2 & & \\ & & L_3 & \\ & & & L_4 \end{bmatrix} \begin{bmatrix} \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \end{bmatrix} = \begin{bmatrix} L_1 \frac{di}{dt} \\ L_2 \frac{di}{dt} \\ L_3 \frac{di}{dt} \\ L_4 \frac{di}{dt} \end{bmatrix}$$

$$\Delta V = L_s \frac{di}{dt}$$

$$\Delta V = v_1 + v_2 + v_3 + v_4 = (L_1 + L_2 + L_3 + L_4)\frac{di}{dt}$$





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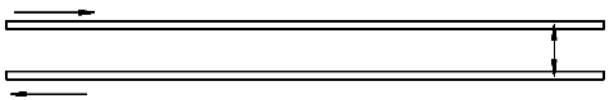
The 3D Power Path Concept

Options to lower inductance in 2D

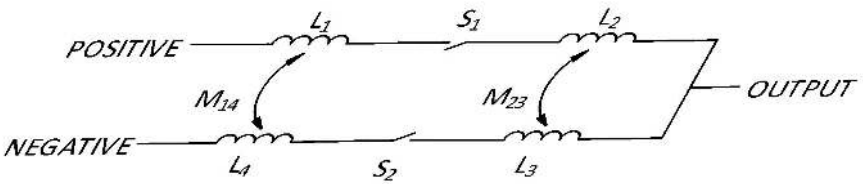
- Minimize each element (L1 ~ L4)
- Bring in mutual inductance (M14 & M23)



$$M = \frac{\mu_0}{2\pi} l[\log\frac{2l}{d} - 1 + \frac{l}{d}]$$

$$L = \begin{bmatrix} L_1 & & & -M_{14} \\ & L_2 & -M_{23} & \\ & -M_{32} & L_3 & \\ -M_{41} & & & L_4 \end{bmatrix}$$

$$\Delta V = L_s \frac{di}{dt}$$

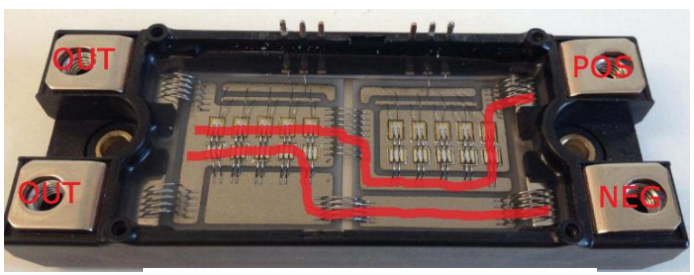


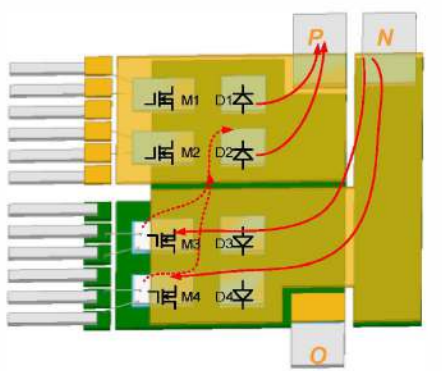
$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_1 & & & -M_{14} \\ & L_2 & -M_{23} & \\ & -M_{32} & L_3 & \\ -M_{41} & & & L_4 \end{bmatrix} \begin{bmatrix} \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \end{bmatrix} = \begin{bmatrix} (L_1 - M_{14})\frac{di}{dt} \\ (L_2 - M_{23})\frac{di}{dt} \\ (L_3 - M_{32})\frac{di}{dt} \\ (L_4 - M_{41})\frac{di}{dt} \end{bmatrix}$$

$$\Delta V = v_1 + v_2 + v_3 + v_4$$

$$= (L_1 - M_{14})\frac{di}{dt} + (L_2 - M_{23})\frac{di}{dt} + (L_3 - M_{32})\frac{di}{dt} + (L_4 - M_{41})\frac{di}{dt}$$

$$= (L_1 + L_2 + L_3 + L_4)\frac{di}{dt} - 2(M_{14} + M_{23})\frac{di}{dt}$$





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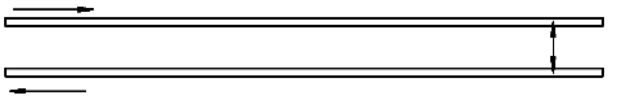
The 3D Power Path Concept

3D Power path to lower inductance

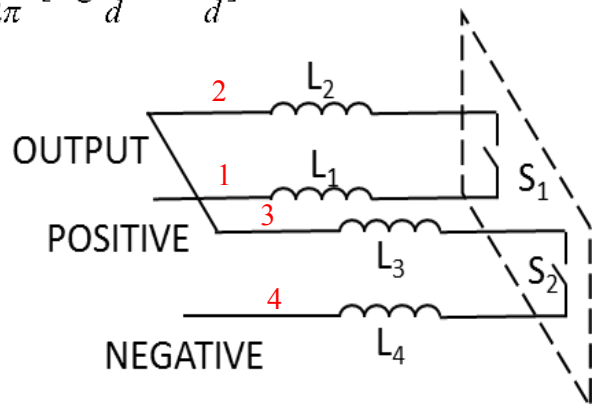
- Fold output terminal to P/N terminal side
- Bring in more mutual inductance cancelation



$$M = \frac{\mu_0}{2\pi} l[\log\frac{2l}{d} - 1 + \frac{l}{d}]$$

$$L = \begin{bmatrix} L_1 & -M_{12} & M_{13} & -M_{14} \\ -M_{21} & L_2 & -M_{23} & M_{24} \\ M_{31} & -M_{32} & L_3 & -M_{34} \\ -M_{41} & M_{42} & -M_{43} & L_4 \end{bmatrix}$$

$$\Delta V = L_s \frac{di}{dt}$$



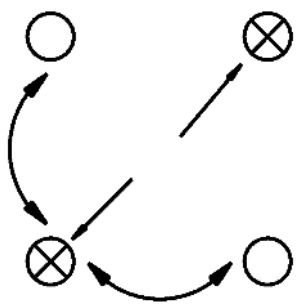
$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_1 & -M_{12} & M_{13} & -M_{14} \\ -M_{21} & L_2 & -M_{23} & M_{24} \\ M_{31} & -M_{32} & L_3 & -M_{34} \\ -M_{41} & M_{42} & -M_{43} & L_4 \end{bmatrix} \begin{bmatrix} \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \end{bmatrix} = \begin{bmatrix} (L_1 - M_{14})\frac{di}{dt} - (M_{12} - M_{13})\frac{di}{dt} \\ (L_2 - M_{23})\frac{di}{dt} - (M_{21} - M_{24})\frac{di}{dt} \\ (L_3 - M_{32})\frac{di}{dt} - (M_{34} - M_{31})\frac{di}{dt} \\ (L_4 - M_{41})\frac{di}{dt} - (M_{43} - M_{42})\frac{di}{dt} \end{bmatrix}$$

$$\Delta V = v_1 + v_2 + v_3 + v_4$$

$$= (I_1 - M_{14})\frac{di}{dt} - (M_{12} - M_{13})\frac{di}{dt} + (I_2 - M_{23})\frac{di}{dt} - (M_{21} - M_{24})\frac{di}{dt} +$$

$$(L_3 - M_{32})\frac{di}{dt} - (M_{34} - M_{31})\frac{di}{dt} + (L_4 - M_{41})\frac{di}{dt} - (M_{43} - M_{42})\frac{di}{dt}$$

$$= \left[(I_1 + I_2 + I_3 + I_4)\frac{di}{dt} - 2(M_{14} + M_{23})\frac{di}{dt}\right] - \left[2(M_{12} - M_{13})\frac{di}{dt} + 2(M_{43} - M_{42})\frac{di}{dt}\right]$$



$$M_{12} > M_{13}$$

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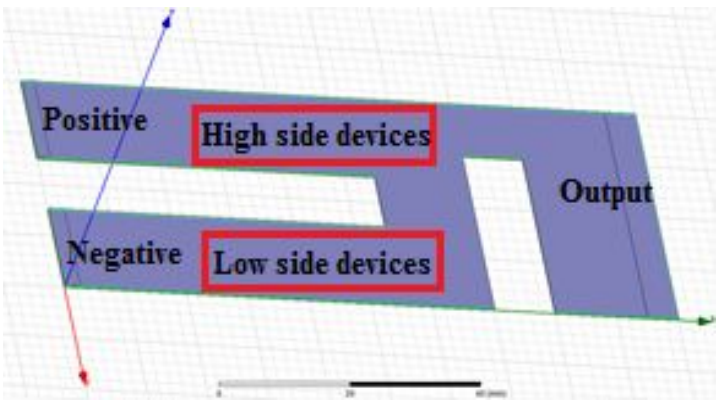
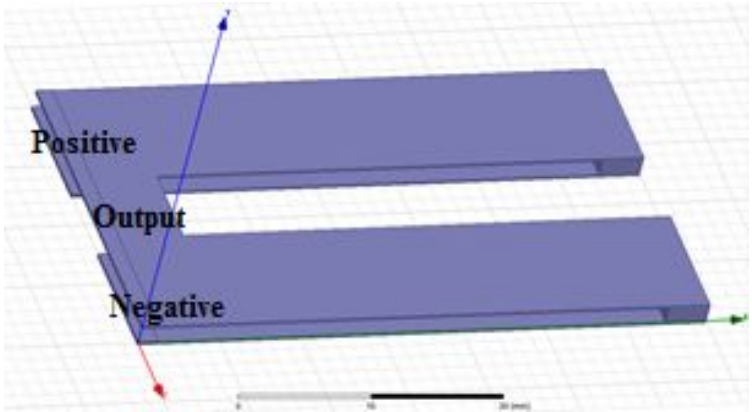
The 3D Power Path Concept

Simulation verification (Ansoft Q3D)

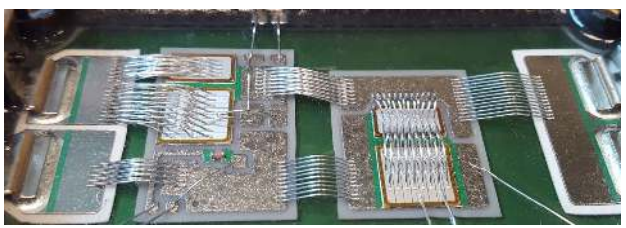
- Cu trace cross section: 12mil (0.3mm) by 15 mm
- Current return point: 60 mm
- Spacing: 10mm lateral & 2mm vertical
- Extract inductance between Positive (P) and Negative (N) terminals at 1MHz



41.2 nH



28.3 nH



POWEREX CM150DX-24A

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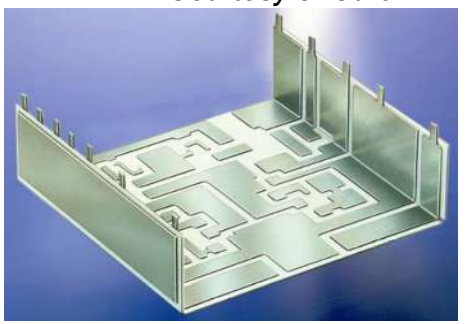
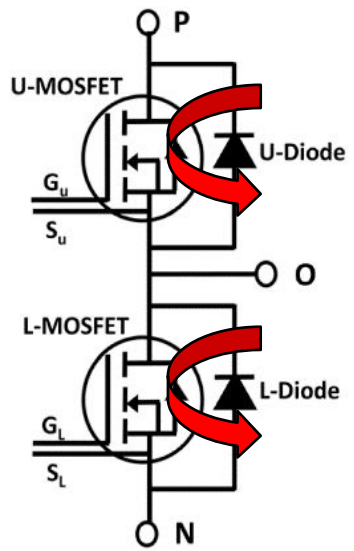
HB Module Fabrication

Half bridge schematic as 1st prismatic Module

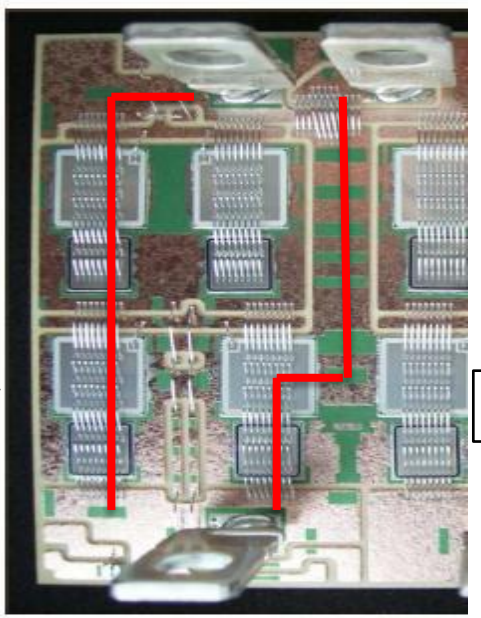
- 4 Devices, 7 terminals
- Electrical – 3D Power path
- Thermal – 5 sided cooling

Courtesy of Curamik

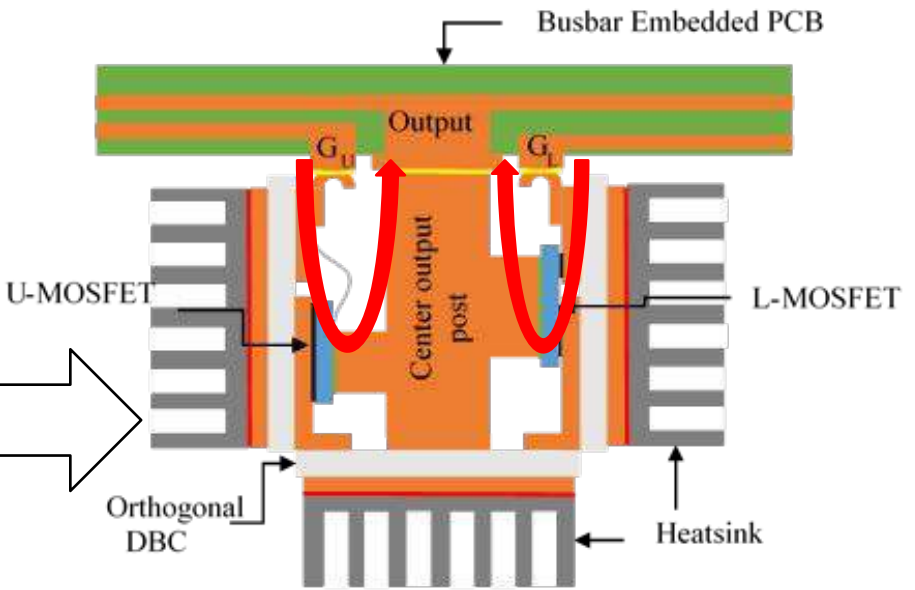




Schematic



2D path in power module



3D path in module

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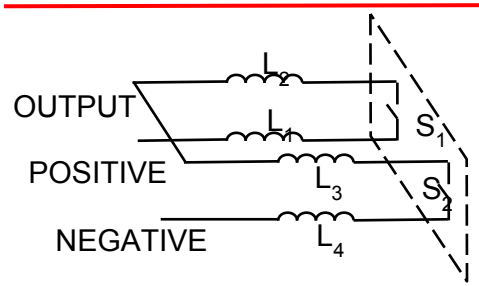
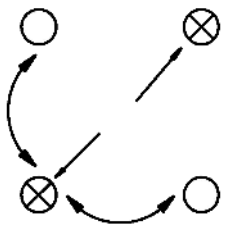
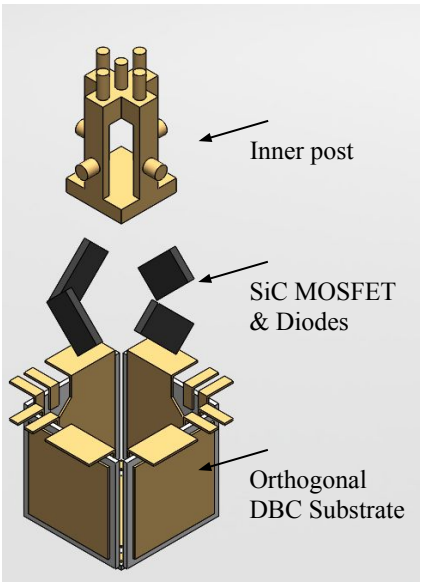
True-3D Module (Phase leg)

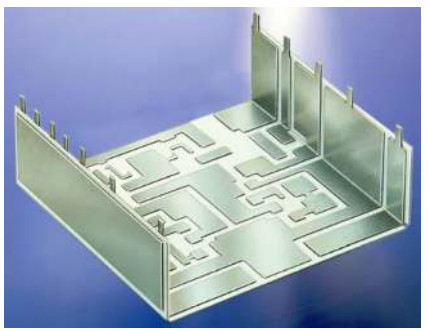


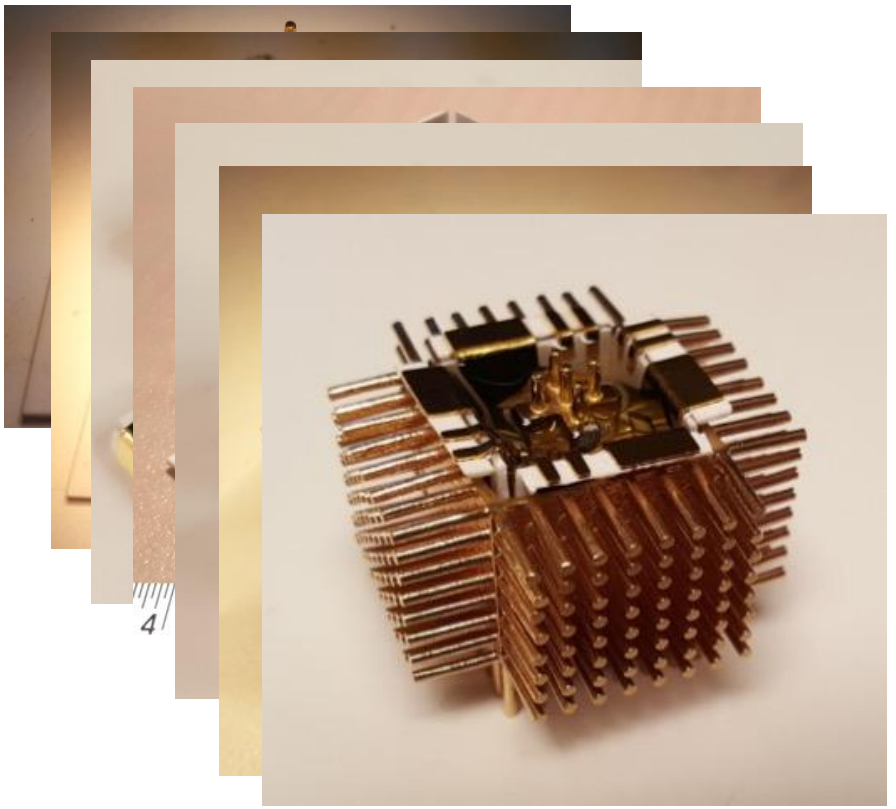
Current path in 3D, and Mutual inductance seen from L_1



$$L = \begin{bmatrix} L_1 & -M_{12} & M_{13} & -M_{14} \\ -M_{21} & L_2 & -M_{23} & M_{24} \\ M_{31} & -M_{32} & L_3 & -M_{34} \\ -M_{41} & M_{42} & -M_{43} & L_4 \end{bmatrix}$$







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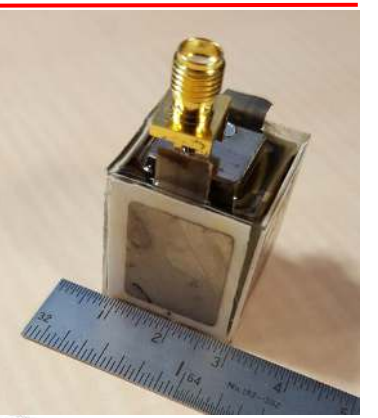
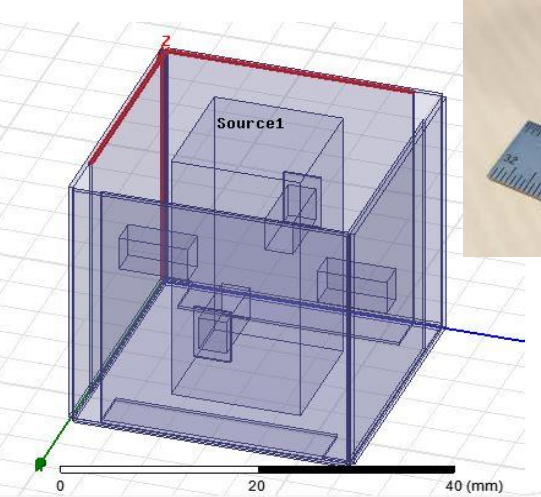
Simulated v. Measured Inductance for HB Module



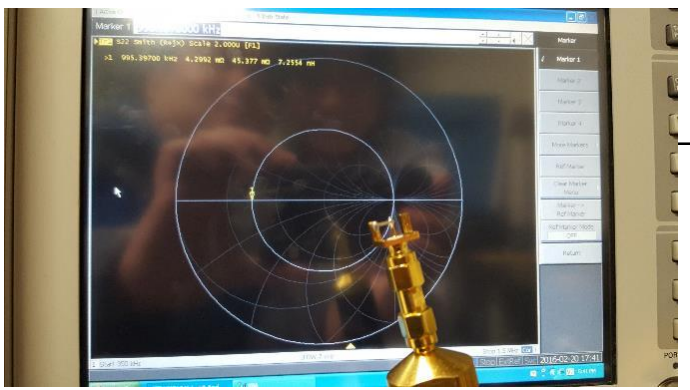
ANSYS Q3D impedance extractor

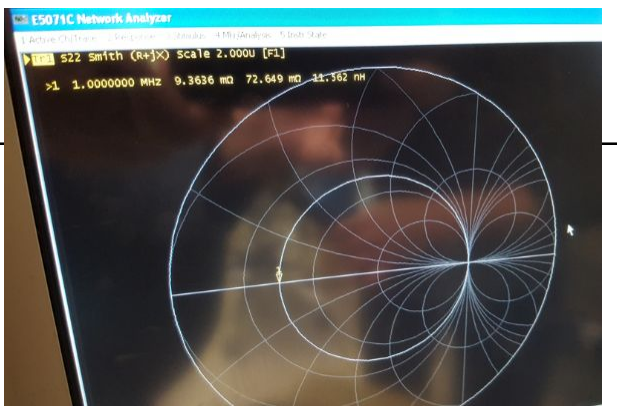
- AC RL simulation @ 100MHz
- Module inductance between Positive (P) and Output (O) is 9nH

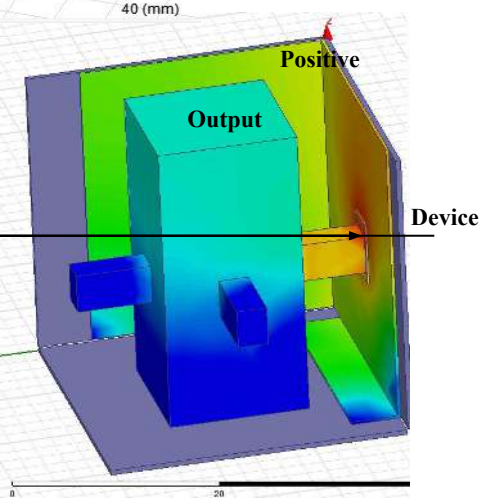


Impedance test with vector network analyzer

- Test with a 3mm wire (1nH) – 7 nH
- Test with module – 12 nH
- Module inductance between Positive (P) and Output (O) is ~6nH







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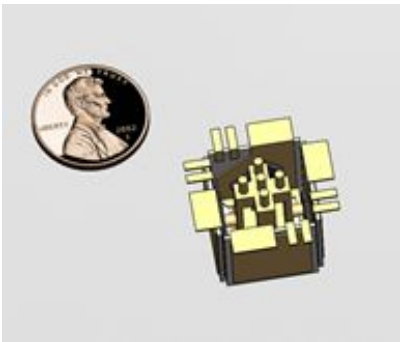
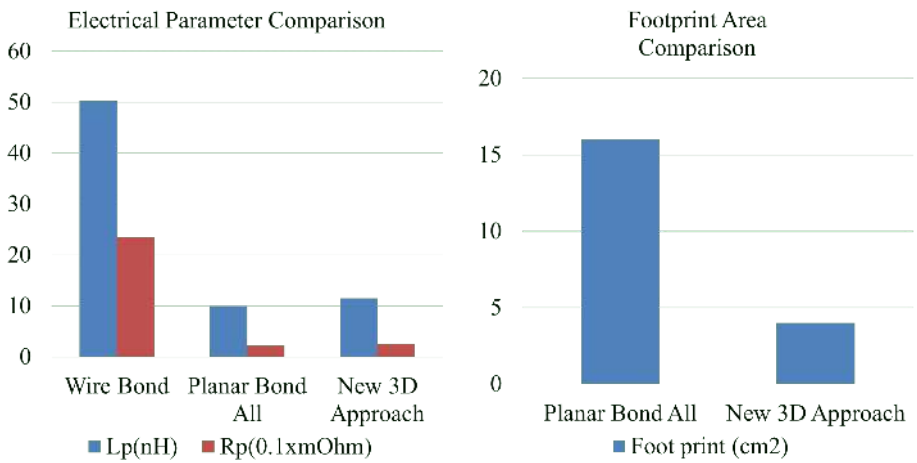
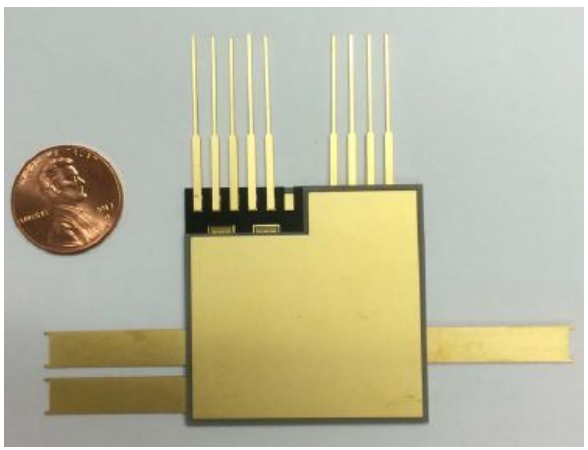
Half Bridge Module

3D prismatic structure vs Planar Bond All structure

- Similar electrical performance (resistance / inductance / symmetric current path)
- Competitive thermal performance
- Potentially better mechanical performance
- Much smaller footprint







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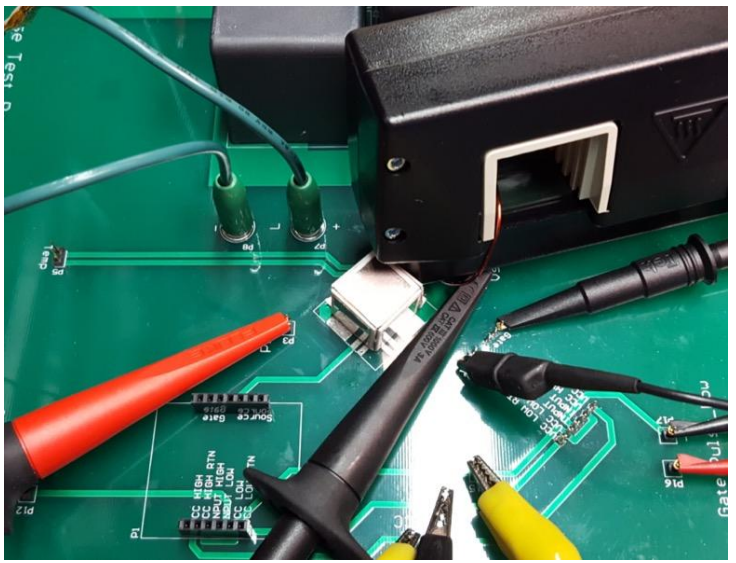
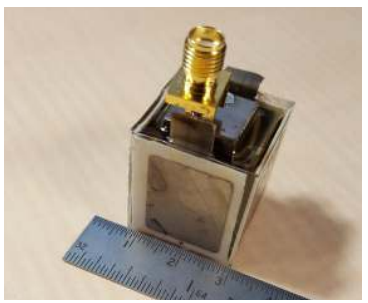
True-3D Mounting and Electrical Testing

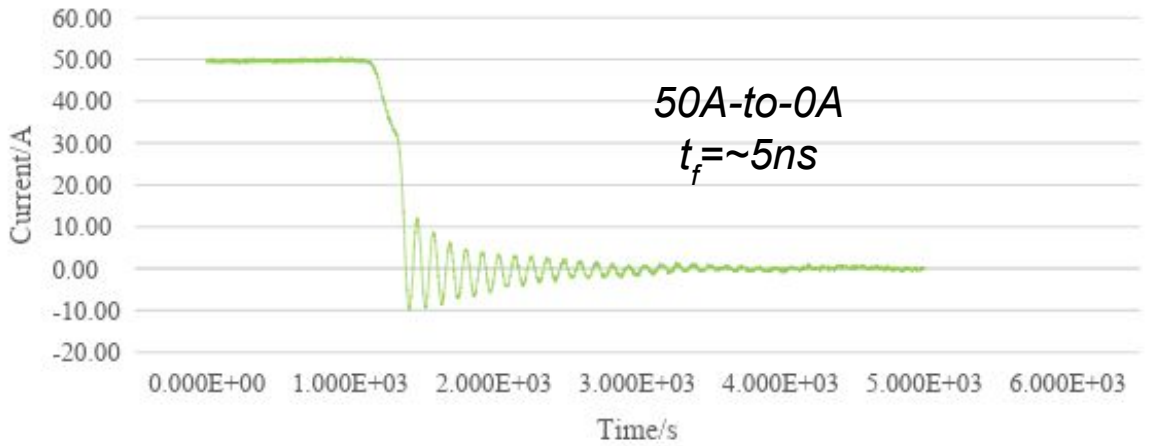


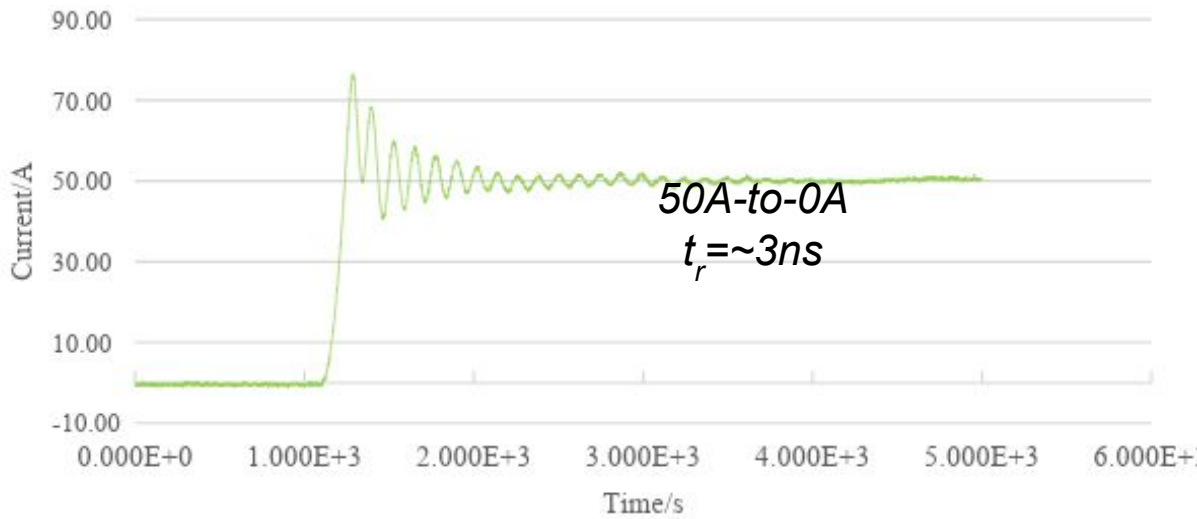


1200V/50A
SiC MOSFETs
& JBS Diode

Impedance test with vector network analyzer
- Test w/ 3mm wire(1nH): 7nH
- Test w/ module:12nH
- 3D module L from Pos and Out is ~6nH

Double Pulse Testing





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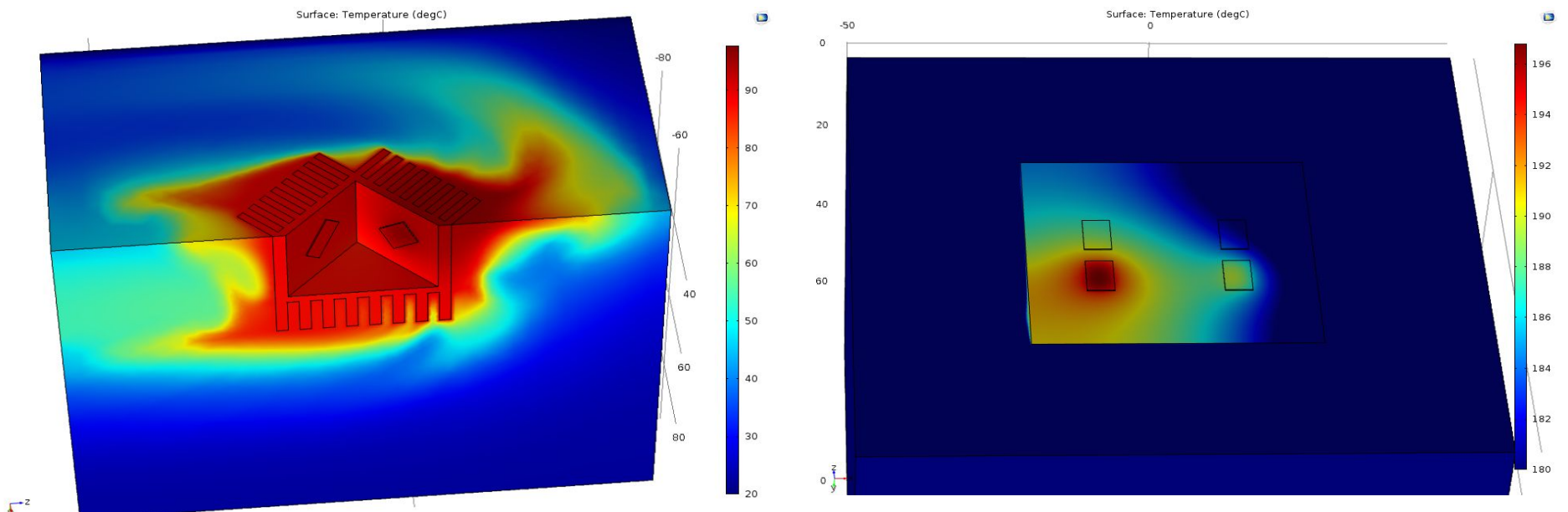
Thermal Simulation of HB Module

Simulation for half bridge module

- Heatsink simulation (COMSOL)
  - Material: 85Cu15Zn (UNS 23000 red brass)
  - Heat source: 15W per chip
  - Ambient: 25˚C air at 7m/s
  - Dimension: 1.5 x 1.5 x 7.5 mm pins with 1.5 spacing.
- Simulation result
  - Max temperature for 3D heatsink: 100 ˚C
  - Max temperature for planar heatsink: 196 ˚C with 10 ˚C difference between two chips



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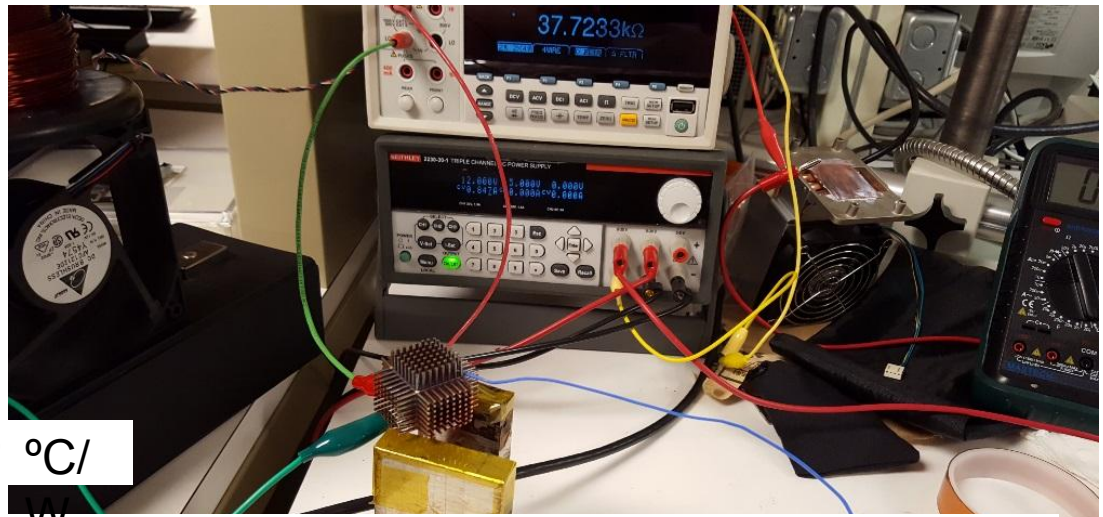
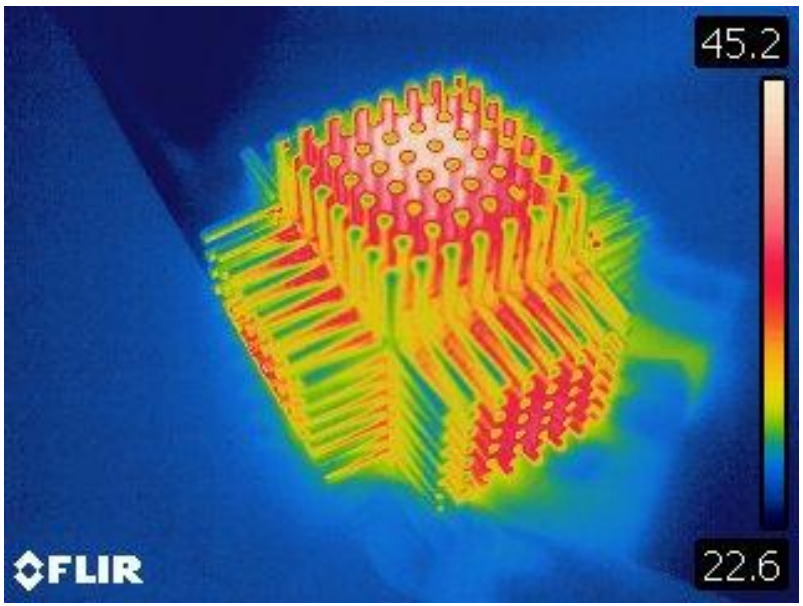
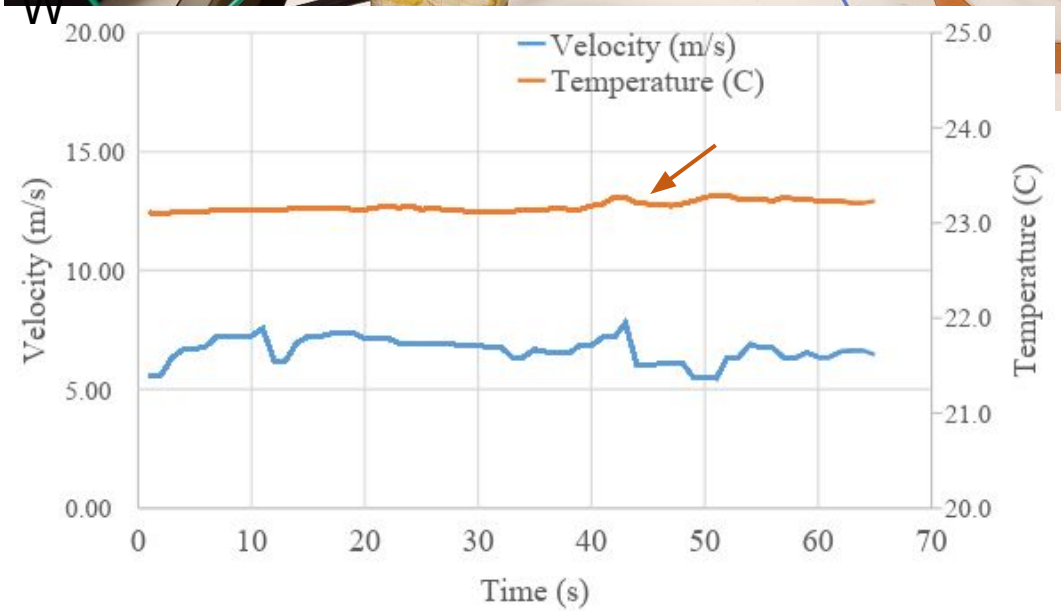
Thermal Test of HB Module

Test of half bridge module

- Thermal test set up:
  - 20A through L-SBD
  - Measurement points:
    - Tj – Thermistor
    - Theatsink – Thermal couple / IR
    - Tambient – Air flow sensor
- Test result: $R_\theta = \frac{T_j - T_a}{P_{loss}} = \frac{90-46}{20\times1.3} = 1.69$ °C/W







"3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules," Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017

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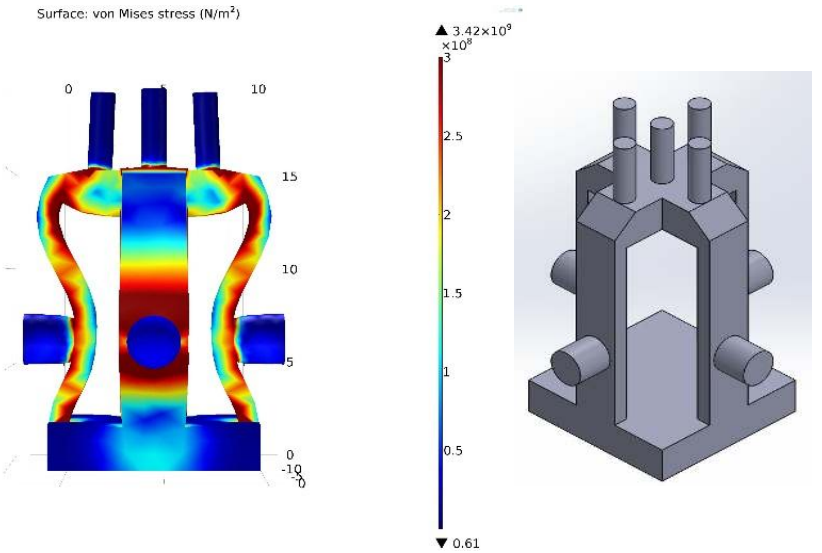
Mechanical Simulation of HB Module Ctr Post

Simulation for half bridge module

- Inner post simulation (COMSOL)
  - Material: 85Cu15Zn (UNS 23000 red brass)
  - Heat source: 200˚C at chip contact
  - Ambient: 100˚C at bottom
  - Constrains: Prescribed displacement
- Simulation result
  - Max von Mises stress: 3 x 108 N/m2
  - Yield strength of red brass 69-434 Mpa (depending on post process)



Properties (UNS23000)	Metric	Imperial
Tensile strength	269-724 MPa	39-105 ksi
Yield strength	69-434 MPa	10-70 ksi
Elongation	55%	55%
Poisson's ratio	0.34	0.34
Elastic modulus	117 GPa	16969 ksi

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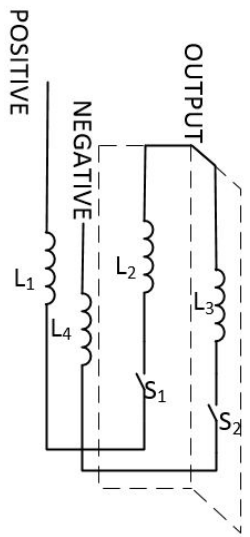
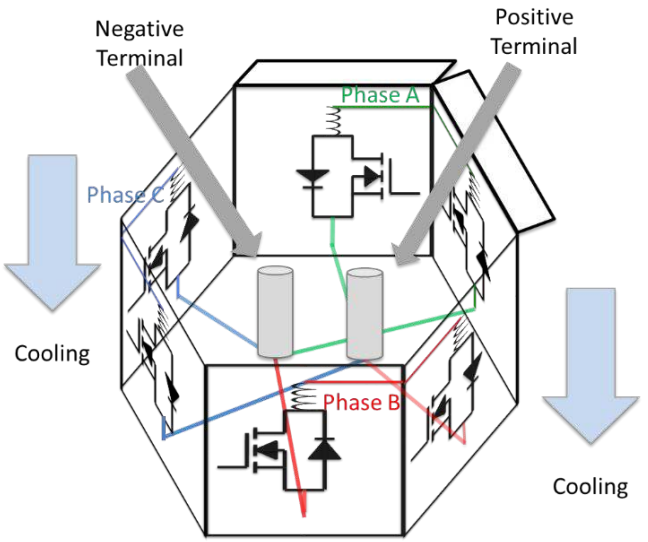
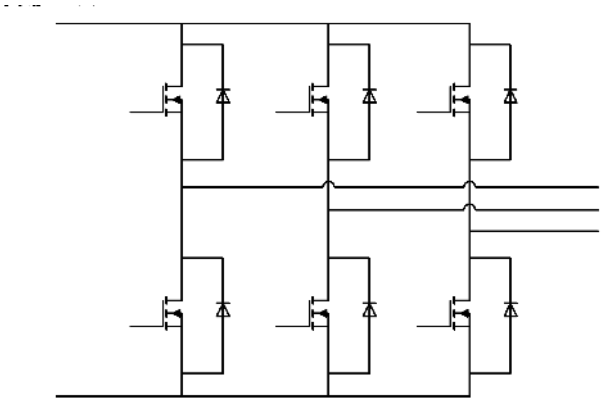
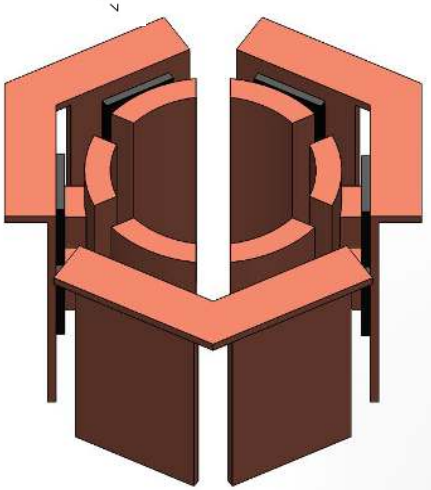
3ø Bridge Concept

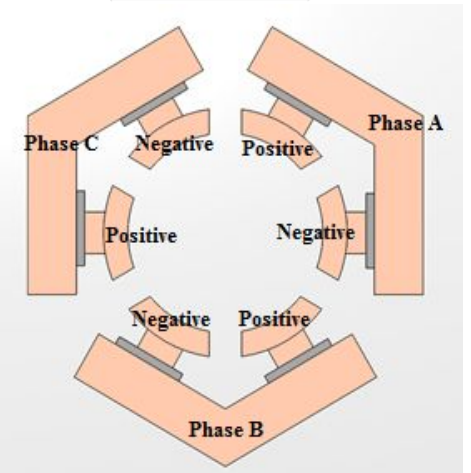
Example: 3-phase full bridge prismatic module

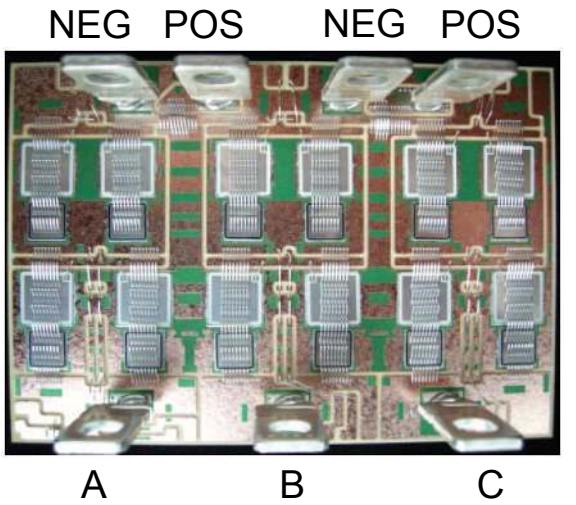












"3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules," Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017

DCHopkins@NCSU.edu
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New thin dielectrics for Low Cost modules

Ceramics?

Flexible-Ceramic Power Electronics Packaging

NEEDS ADDRESSED

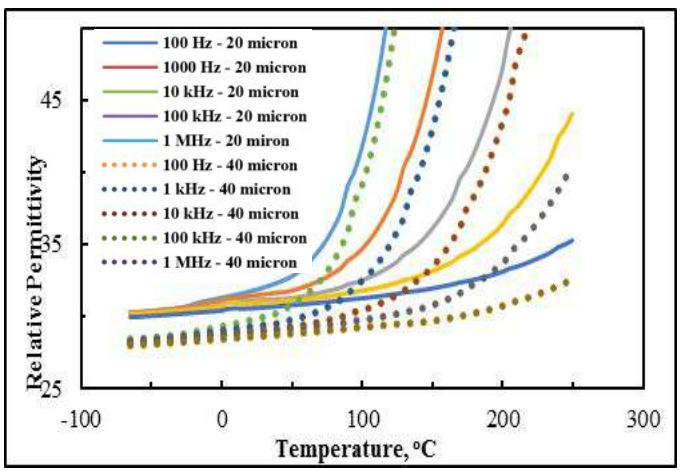
High Density, Fast Response, Low Voltage, System-in-Package Power Converters

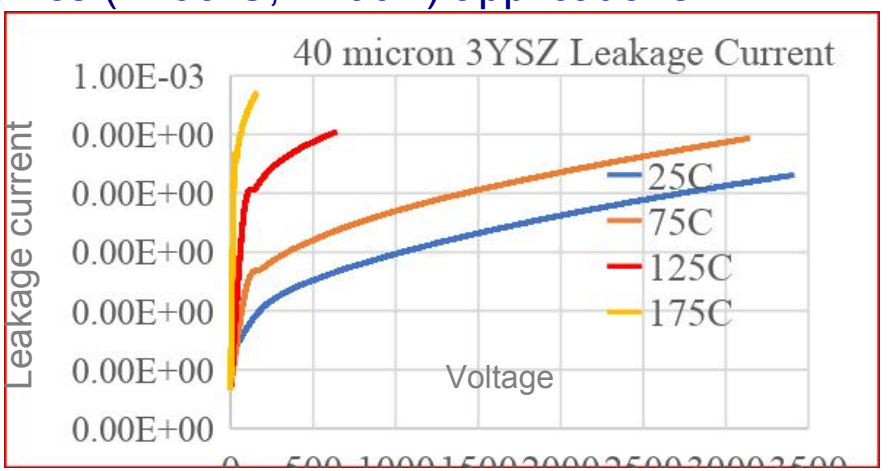
- Need Inexpensive converters with good thermal management
- Operate Temp ≤85˚C (similar to PCB)
- Suitable for high current GaN
  - and wearable power electronics

TECHNOLOGY

- Thin E-Strate flexible 3YSZ ceramic for:
  - High volume roll-to-roll manufacturing
  - High thermal management for highly dense LV power converters
- Thin 20 & 40 micron substrates for low thermal resistance
- Licensed from Corning

The 3YSZ Suitable for wearable electronics (<100˚C, <100V) applications





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New Thin Organic Dielectrics for Low Cost Modules

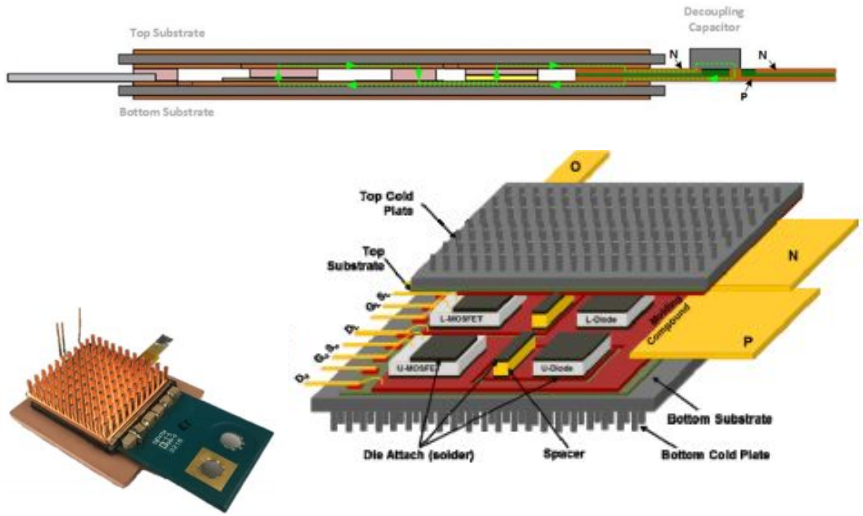
Epoxy Resin Composite Dielectrics – ERCDs

These provide and opportunity to look at very low cost modules with *embedded* components.

"Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao[1], Yifan Jiang[1], Bo Gao[1], Kenji Nishiguchi[2], Yoshi Fukawa[3], D. C. Hopkins[1]

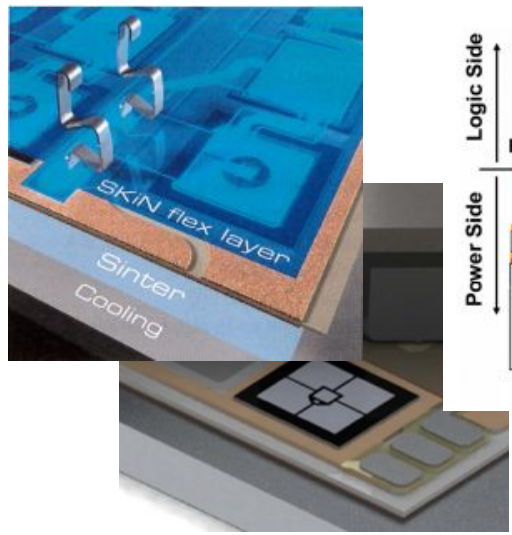
[1]North Carolina State University, [2]Risho Kogyo Co., LTD, [3]TOYOTech LLC

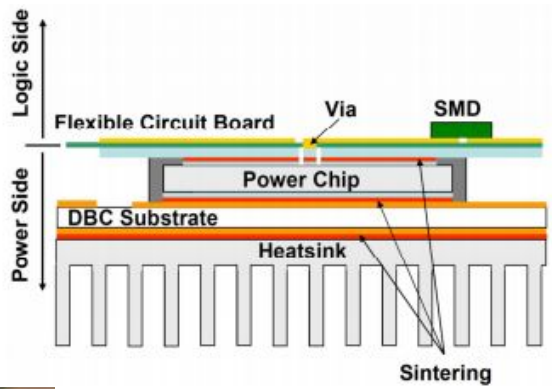
State-of-art development of WBG power module



SiC Module w/ double-sided cooling by ORNL [1]

- 2.6 nH extracted parastics inductance
- Bus up to 600V with >40A capability
- Kelvin connections implemented
- Gate bonding wire required





SKiN and Direct Pressed Die technology by Semikron [2]

- >20% thermal resistance reduction
- 10% reduction in parasitic inductance
- >25% improvement in surge current
- Improved thermal-cycling based reliability
- 1700V/1800A
- Challenge on the Press Unit design and implementation

[1] F. Yang, et al. Design of a Low Parasitic Inductance SiC Power Module with Double-sided Cooling. APEC 2017, Tampa, FL.
[2] S. Hauser. Direct Pressed Die Technology: Increased Power Density and Reliability in Standard Power Module Packages. APEC 2017, Tampa, FL.

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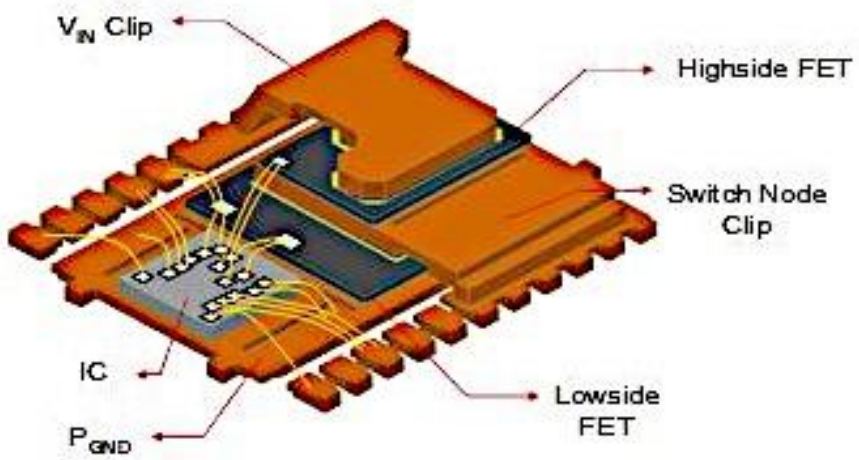
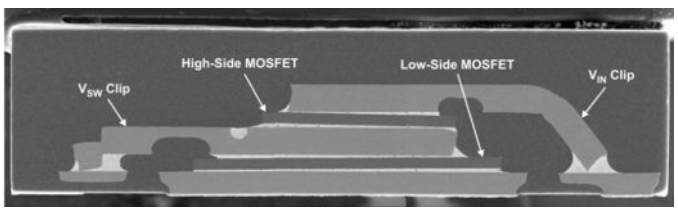
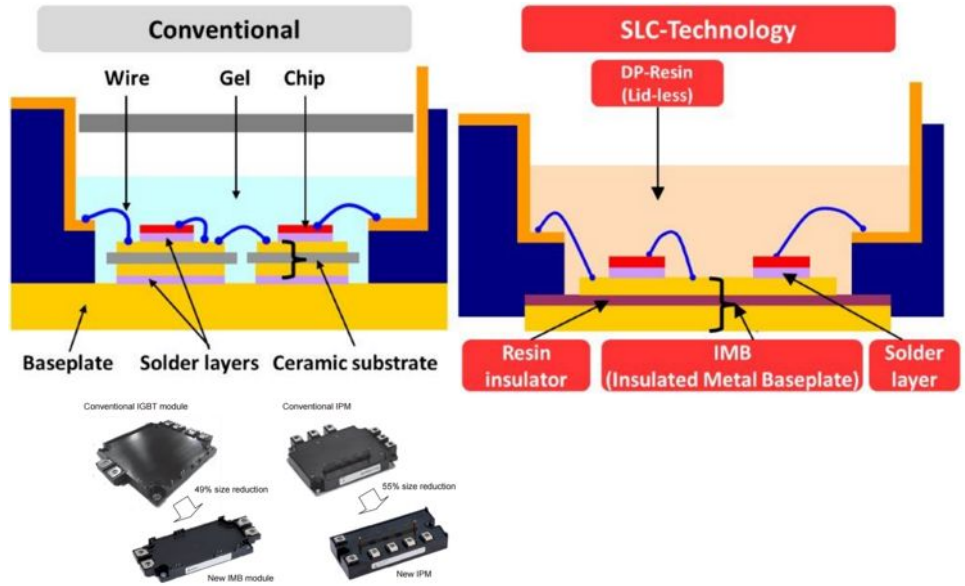
State-of-art development of WBG power module





PowerStack packaging technology by Texas Instruments[3]

- Lower Parasitics between high- and low-side switches
- Improved Power Efficiency
- Better Thermal performance
- Applicable for lower voltage applications for now



- Insulated-Metal-Baseplate based IPM by Mitsubishi [4, 5]
- CTE of insulating resin layer ~17ppm, close to Copper, with better mechanical stress management
- 35% thermal impedance reduction from development of resin
- Less interconnection layers for lower profile, up to 55% size reduction from traditional DBC based module
- Better thermal cycling reliability with less cracks during cycling
- Heavily depends on the resin interface material

[3] M. Roming, et al. 3D packaging advancements drive performance, power and density in power device. White Paper, Junly 2011.
[4] Y. Kaji, et al. Novel IGBT Modules with Epoxy Resin Encapsulation and Insulating Metal Baseplate. ISPSD 2016.
[5] T. Takahashi, et al. A 1700V-IGBT module and IPM with new insulated metal baseplate (IMB) featuring enhanced isolation properties and thermal conductivity. PCIM Europe 2016.

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Criterion for thin dielectric selection for

Target Application: 1200V / 40A SiC MOSFET and Schottky Diode based Power Module

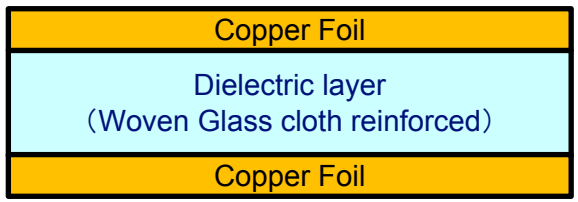
Parameters	Unit	Value
Thermal Conductivity	W/mK	> 3
Breakdown Voltage	kV	> 3
Leakage Current	μA	~ 10
Dielectric Constant	1	< 8
Operation Temperature	°C	> 175
Processing Temperature	°C	> 250

Criterion for thin dielectric selection for power module substrate applications

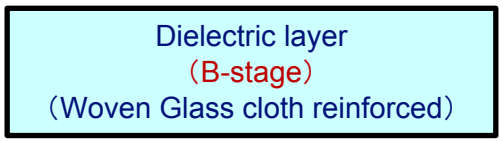
- *Thermal conductivity* need not be high, due to thin dielectric
- *Sufficient breakdown voltage* for adequate margin for 1200V SiC MOSFETs
- *Low leakage current comparable with SiC devices* at the same conditions, such as temperature
- *High temperature* operation similar to SiC devices
- *High processing temperature* to leave margin for assembly processes

From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

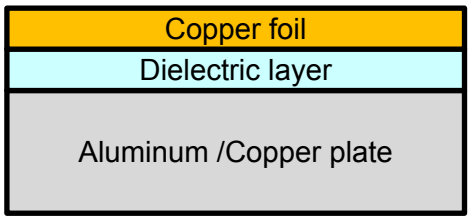
Epoxy Resin Composite Dielectric by RISHO



CCL (CS-XXXX)
Cu Clad Laminate



(ES-XXXX)
Prepreg



(AC-XXXX)
Metal base CCL

HIGH THERMAL CONDUCTIVITY MATERIALS

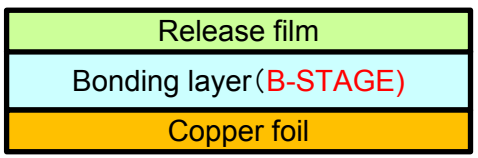
Liquid Molding Compound
(One-pack type)
（1～4W/mK）

Liquid Molding Compound
(Two-pack type)
（1～7W/mK）

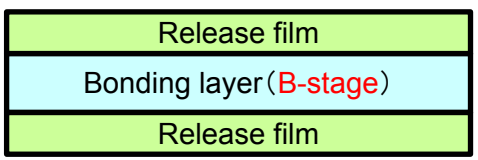
AC-7208 8W/mK	AC-7210 10W/mK

Al base CCL

AD-7208 CD-7208 8W/mK	AD-7210 CD-7210 CC-7210 10W/mK



(CD-XXXX)
Resin Coated Cu



(AD-XXXX)
Bonding sheet

Bonding sheet, RCC, Copper-base CCL without glass fabric

Courtesy of RISHO

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Investigating Flexible Thin Dielectric as Substrates

Target Material: Recently developed Epoxy-Resin based dielectric by Risho Kogyo Co., Ltd. – AC-7208

Properties of the Thin Dielectric (measured at 120 µm)

Better Stress Management

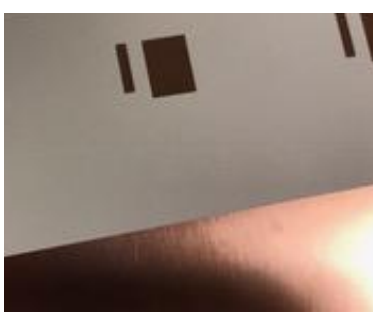
- CTE closer to copper than traditional ceramic (4.5 ppm/K ~ 7 ppm/K)
- Flexible allowing for stress release during assembly and service of the module

Parameter	Unite	Value
Thermal Conductivity	W/mK	8
Tg	°C	270
Modulus	GPa	30
Bending Strength	MPa	94
CTE	ppm/°C	9/22
Dk	/	6.3
Df	/	0.009
Water Absorption	%	0.27
Dielectric Strength	kV	5.6 @ 120 µm

Comparable thermal performance with alumina

- Better unit area thermal conductance than alumina
- 1/5 unit area thermal conductance of AlN
- Lower cost for epoxy-resin substrate

Parts	Thickness /µm	Thermal Conductivity W/m·K	Unit Thermal Conductance $W/m^2 \cdot °C$
Epoxy-resin	80	8	0.1E6
Al_2O_3	254	23	0.09E6
AlN	254	170	0.67E6



From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

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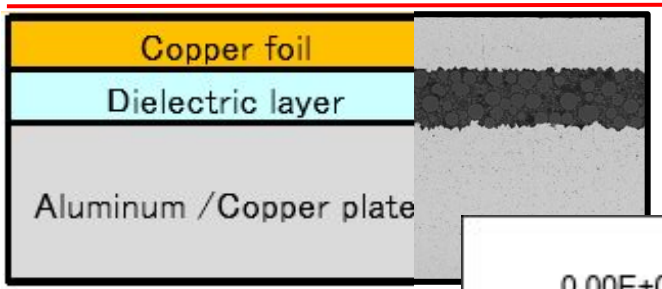
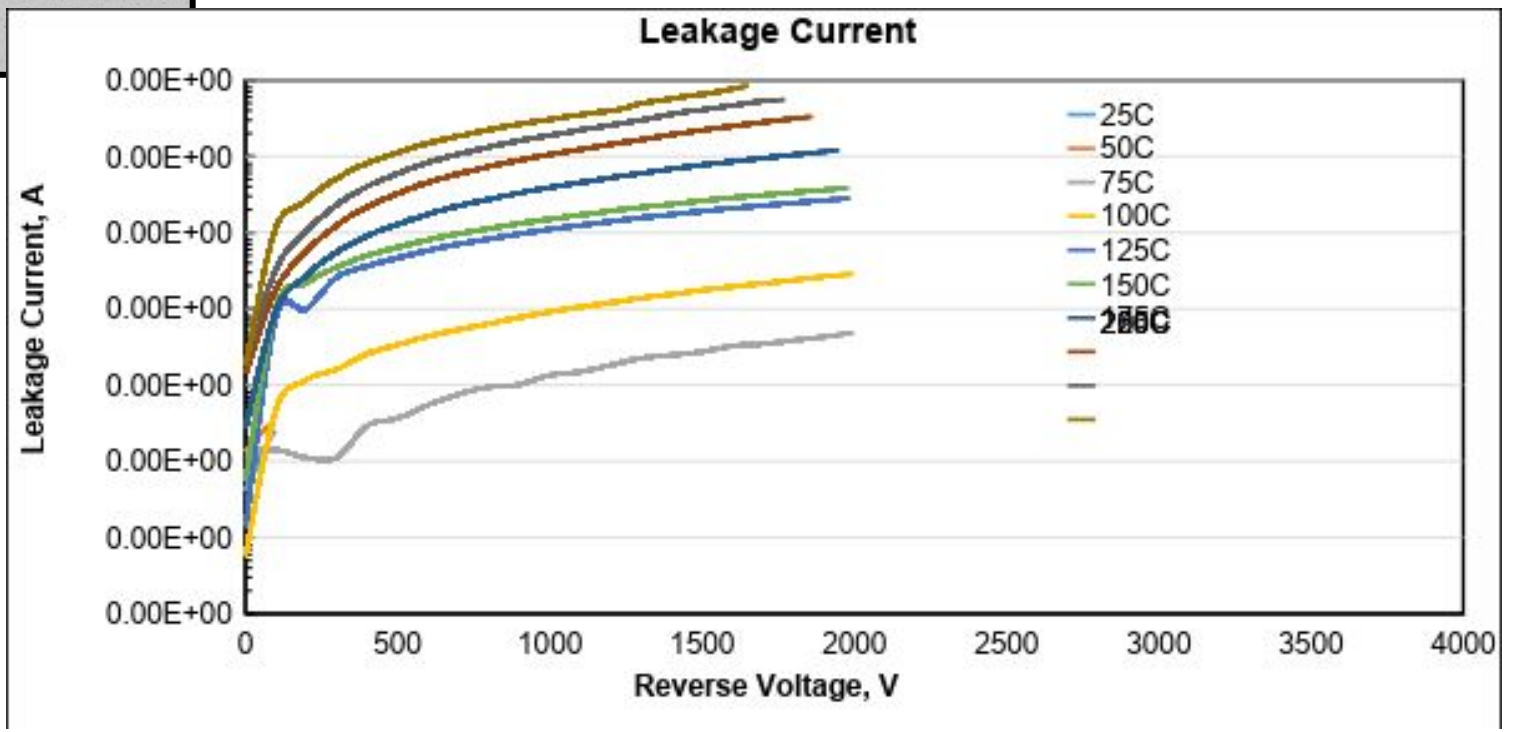
Epoxy Resin Composite Dielectric



- Capable of bonding with Copper on both sides
- Copper thickness up to ≤ 0.6 mm
- 80 µm dielectric thickness is available



Leakage current measured on 80 µm sample with Cu bonded on both sides

- 20 µA leakage even at 250 ºC with 1200 V voltage applied
- 1 nA leakage at room temperature with > 4kV voltage applied

From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

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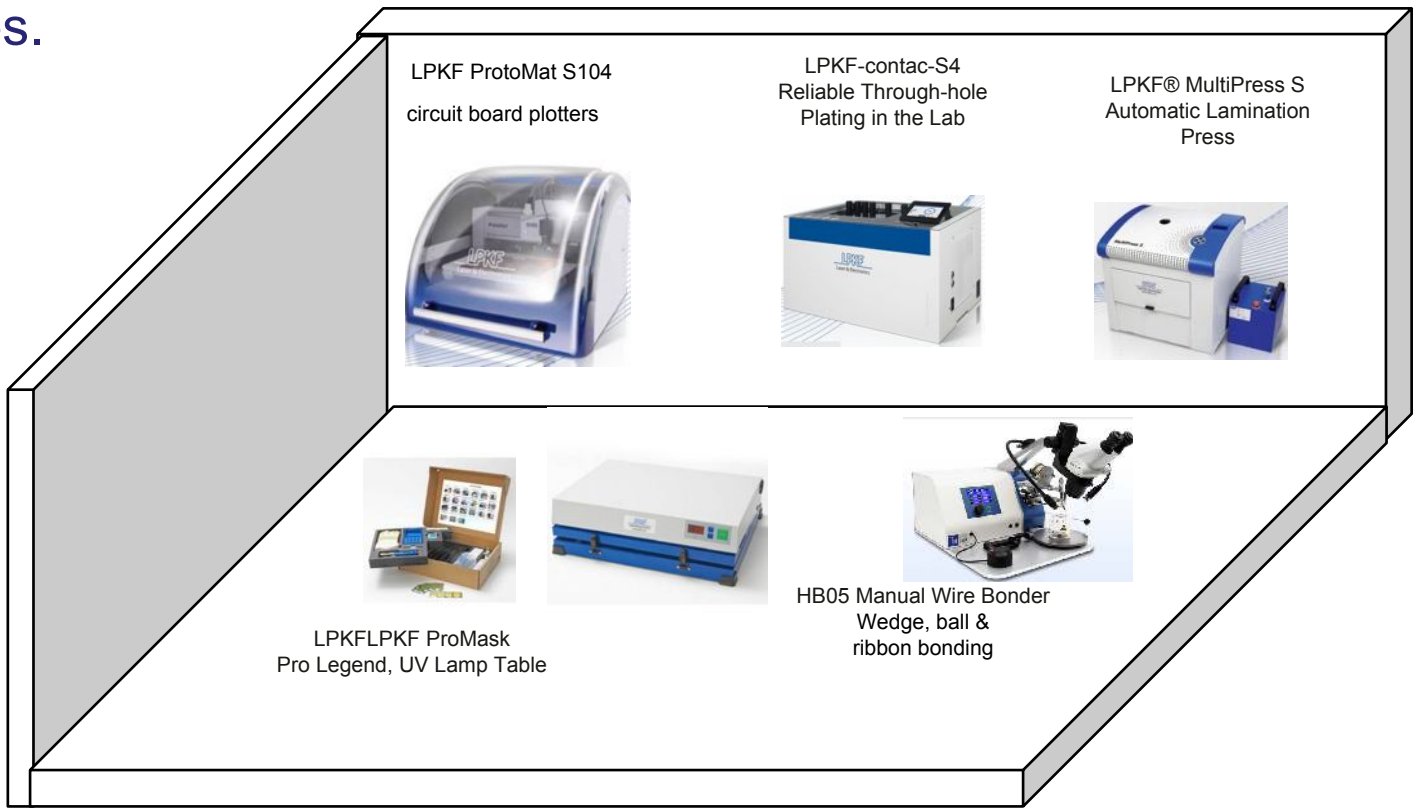
Resource Development for ERCD Topology Research

1. ERCD ”substrate-less” approaches identified for high voltage (5kV/120µm), high temperature (≤300ºC) and high thermal impedance (10W/mK).
2. Materials systems for fluid compatibility, multilayering and metal backing for investigation of dense high voltage power module structures.
3. Processes and equipment for ERCD systems identified and ordered through PREES resources.



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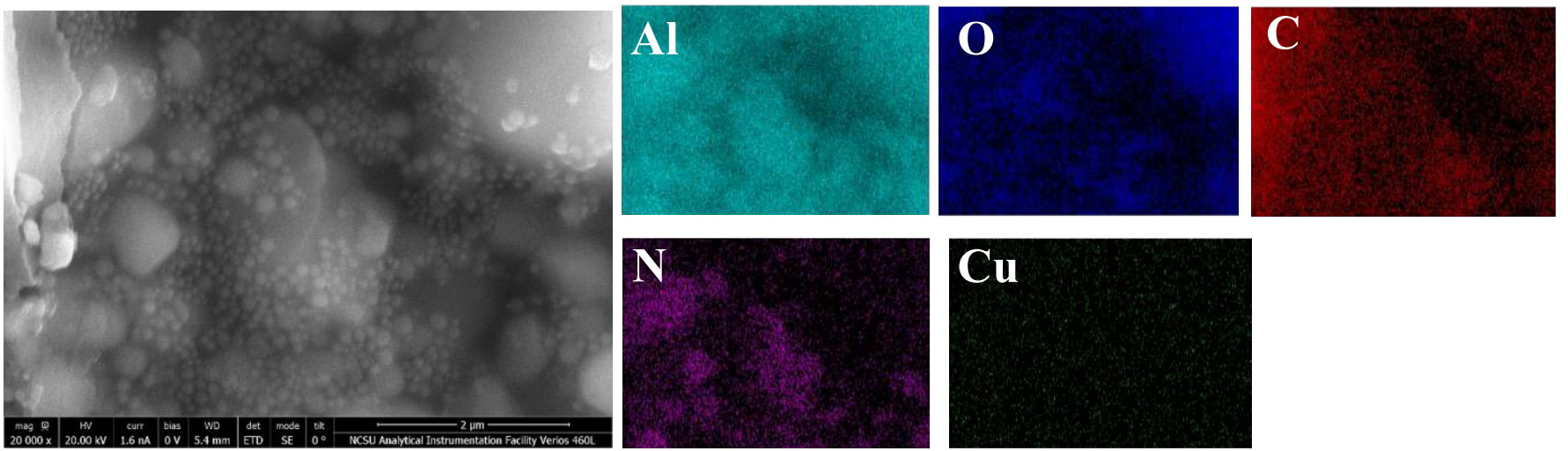
ERCD Composition



Microstructure of the dielectric at 20,000 magnification

- O is corresponding to alumina particles, distributed almost everywhere, N is the AlN particles, with limited number, C is from the polymer, Cu is from the bonding interface
- AlN and alumina particles are also identified by XRD analysis
- High thermal conductivity is from the widely distributed alumina particles and few AlN particles

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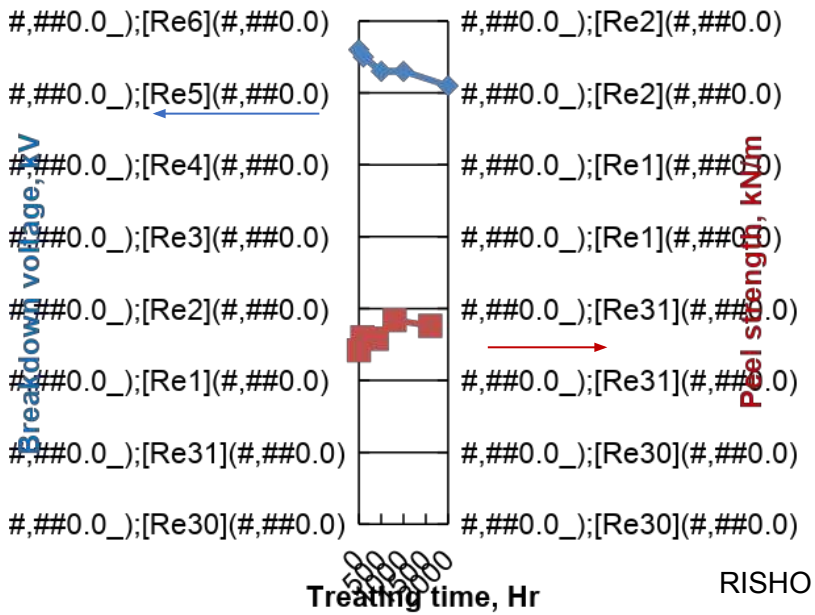
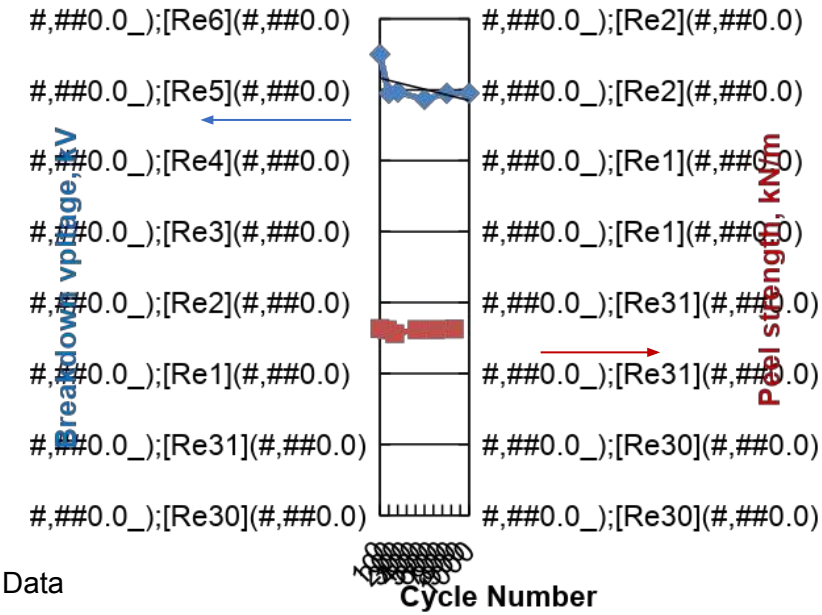
ERCD Breakdown Voltage





RISHO Supplied Data

Properties during reliability experiments (Thermal aging and thermal cycling)

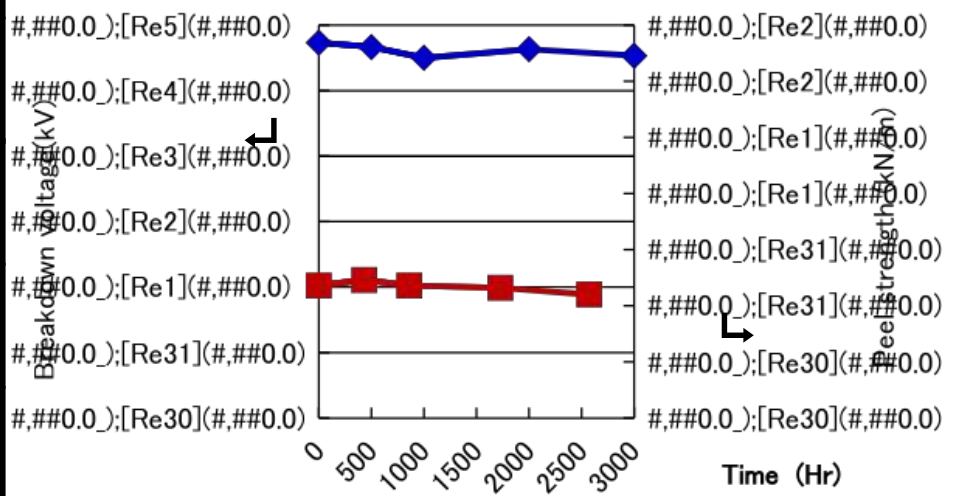
- Thermal aging is conducted at 150 ºC
- Thermal cycling is from -55ºC to 125 ºC
- Peel strength (35µm copper on 120µm dielectric with 1mm Al) is not as high as DBC interface (4N/mm for 0.3mm Cu on alumina)
- Limited degradation during thermal aging up to 200 Hr in breakdown voltage and peel strength
- The properties do not change much during thermal cycling up to 1000 cycles

From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

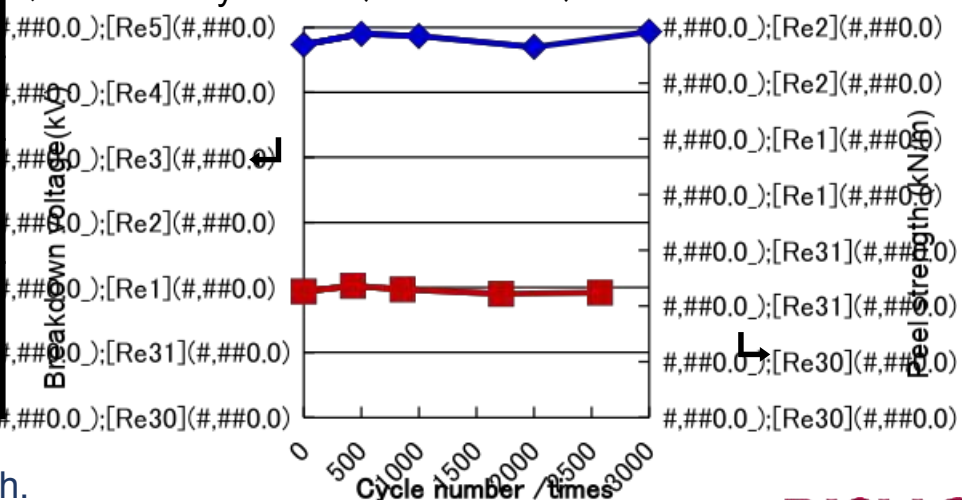
AC-7208 (8W/mK)

Product number	AC-7208	
Dielectric layer thickness	120μm	
Thermal cond. (W/mK)	8	Laser flash
Tg(℃)	270	DMA method
Peel strength (kN/m)	1.2	1 oz copper
Solder limit(sec)	Over 60	260ºC
CTE(ppm/℃)	9/22	α_1/α_2
Breakdown (kV)	Over 5	JIS C2110
CTI	Over 600	IEC method
Flammability	V-0equiv.	UL94

◆High temperature long term test(@175℃)



◆Thermal cycle test(-40⇔125℃)



After long term test at 175℃ and thermal cycle test,
There is no problem in breakdown voltage and peel strength.
→ This material also shows high reliability.

Courtesy of RISHO

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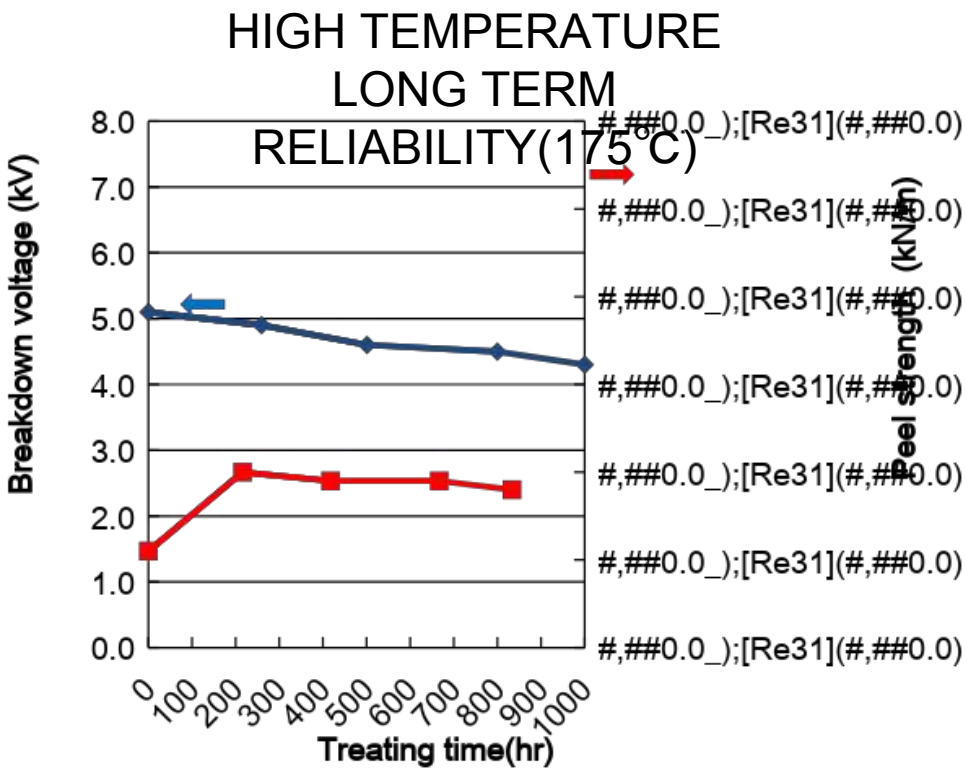
www.PREES.org

AC-7210 (10W/mK)

Product number	AC-7210	
Dielectric layer thickness	120μm	
Thermal cond. (W/mK)	10	Laser flash method
Tg (℃)	270	DMA method
Peel strength (kN/m)	1.2	1 oz copper
Solder limit (sec)	60＜	260℃
CTE (ppm/℃) α1	14/14/14	X/Y/Z
Breakdown voltage (kV)	5＜	JIS C2110
CTI	600＜	IEC method
Flammability	V-0 equivalent	UL94



Courtesy of RISHO

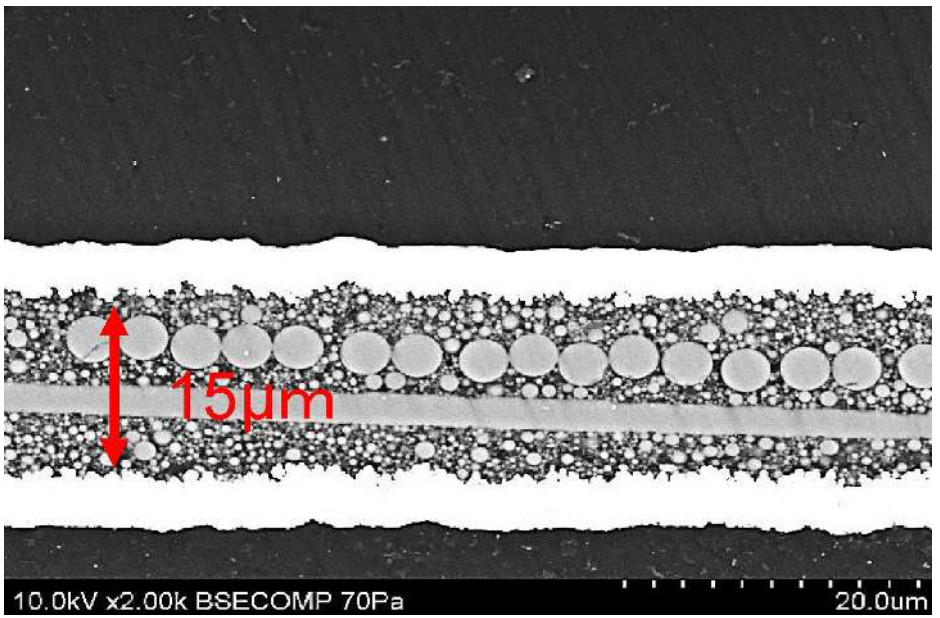
High Heat resistance CCL for Power Modules

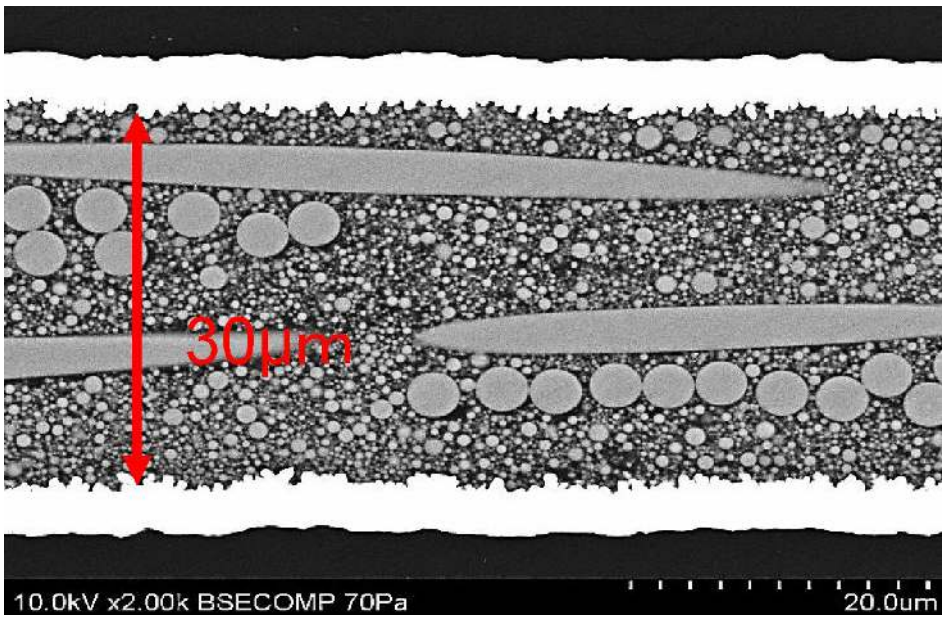
Low CTE and high heat resistance material

CS-3305A (CCL)

ES-3310A (Prepreg)

Ultra-thin thickness(15μm of 1ply type or 30μm of 2ply type)





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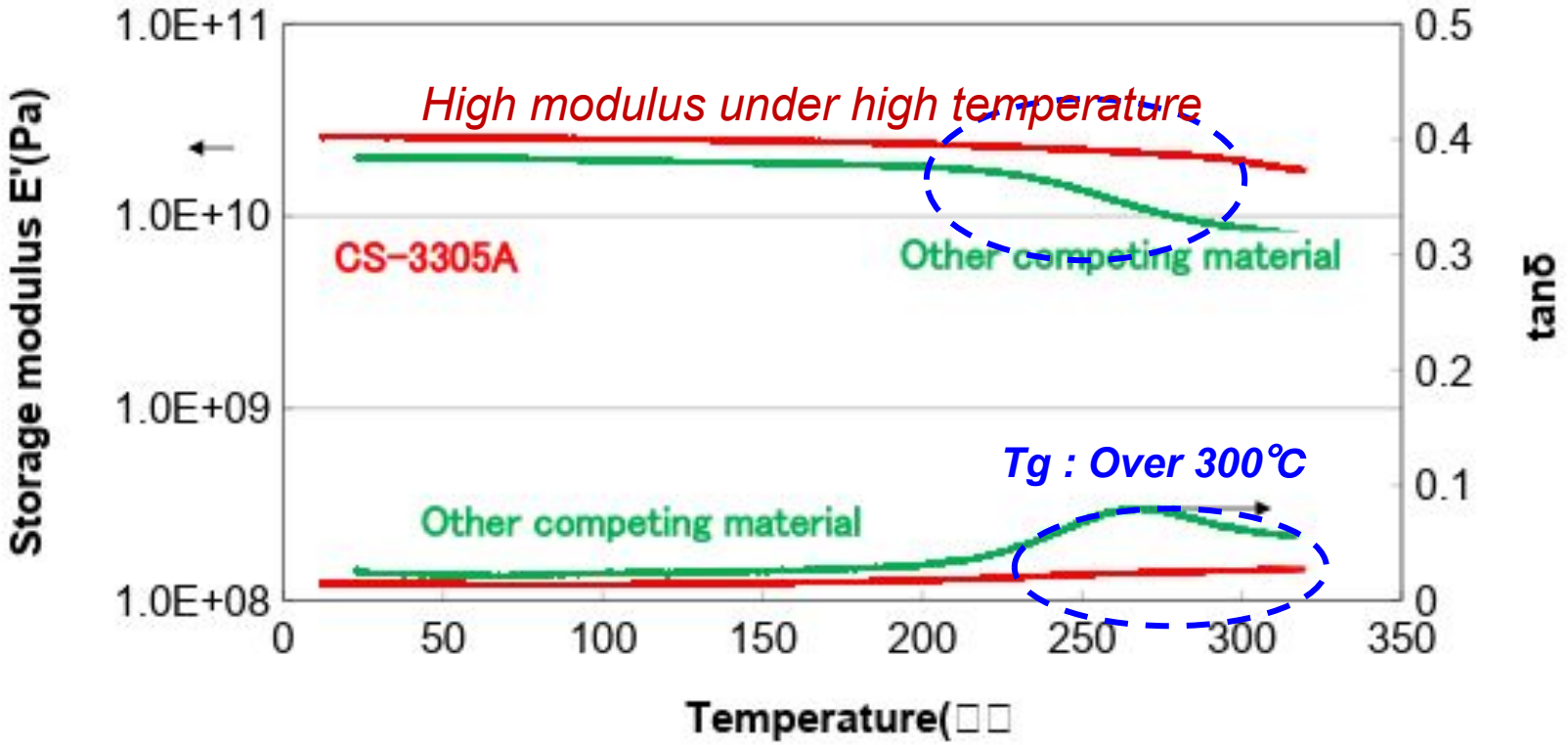
General properties of CS-3305A series

Item			Unit	CS-3305A (E-glass)	CS-3305AS (Low CTE glass)	CS-3305AQ (Quartz glass)
CTE *(Other Low CTE glass fabric enables lower CTE)*	Y	α_1	ppm	6～8	2～4	0.5～1
	X	α_1	ppm	6～8	2～4	0.5～1
	Z	α_1	ppm	10～15	10～15	10～15
Glass transition Temperature (Tg)	DMA		℃	Over 300ºC		
Water absorption ratio			%	0.13		
Flexural strength（Y-axis）	25℃		MPa	517	660	446
	250℃		MPa	415	470	356
Flexural modulus（Y-axis）	25℃		GPa	32	35	32
	250℃		GPa	16	19	19
Peel strength (Copper)			KN/m	0.6 [VLP 1/3oz]		
Solder heat resistance(300℃)			Sec.	over300		

High Tg and high modulus by DMA method

RISHO

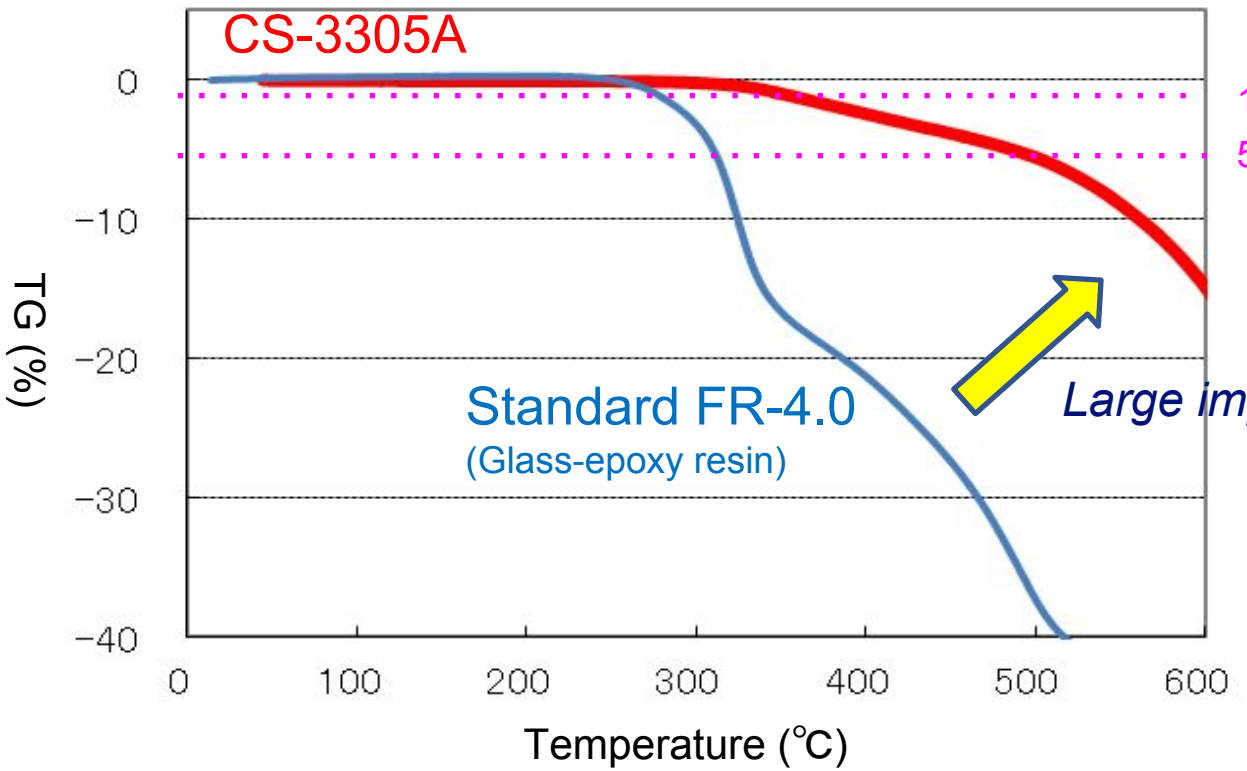


- There is no *tanδ* peak of CS-3305A → Tg : over 300℃
- Storage modulus maintains higher than the other material under the high temperature.

Courtesy of RISHO

Thermal decomposition temperature by TGA method

CS-3305A is a long term heat resistance material.



Atmosphere : Air
Heating rate : 10℃/min
Reference : Al_2O_3

	CS-3305A	Standard FR-4.0
Td(1%)	352℃	277℃
Td(5%)	487℃	310℃

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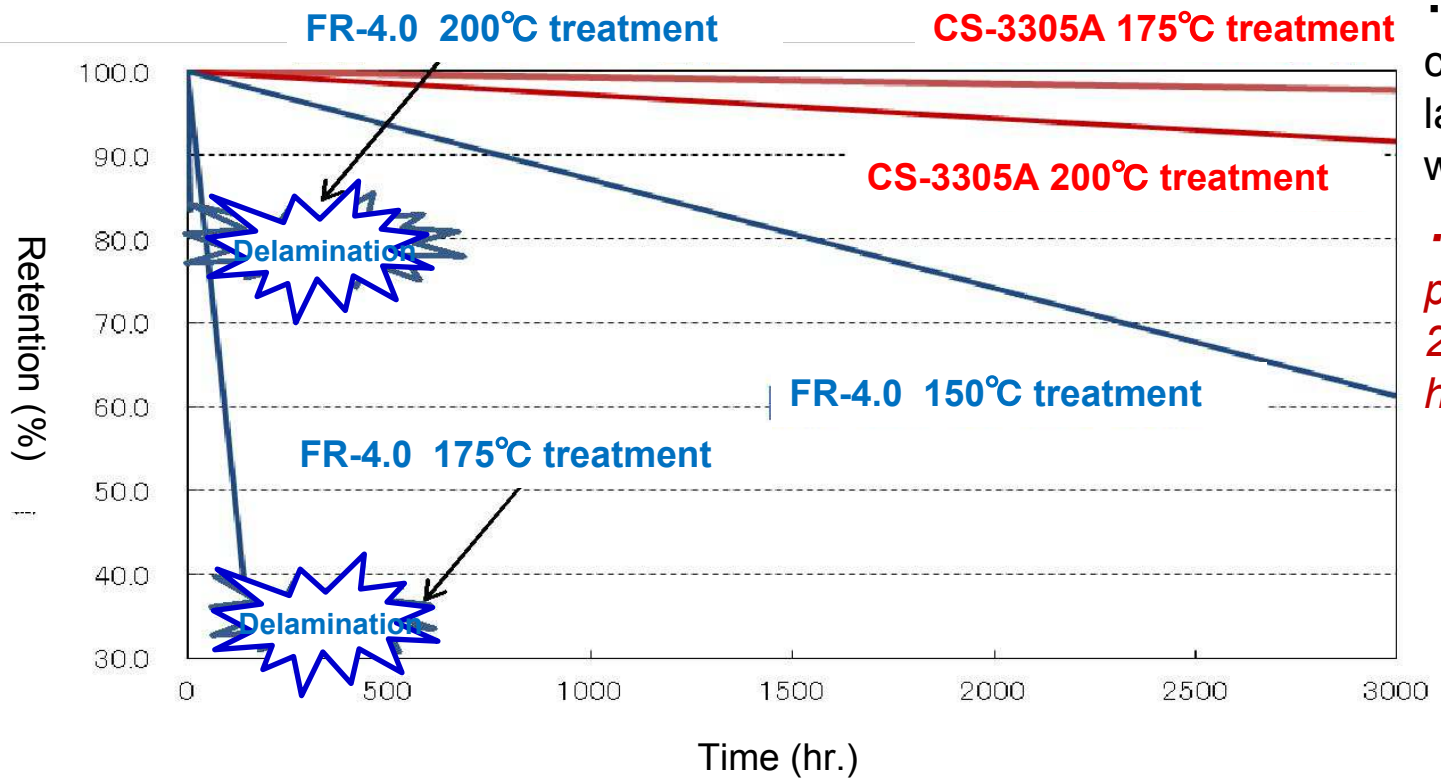
Retention of peel strength of copper foil



- Delamination between copper foil and dielectric layer of standard FR-4.0 was occurred at 175℃.

- *CS-3305A maintained peel strength at 175 and 200℃ even after 3000 hours treatment.*

	CS-3305A		Std FR-4.0
Temperature	175℃	200℃	150℃
0hr. (Retention)	1.30kN/m (100%)	1.30kN/m (100%)	1.60kN/m (100%)
1500hr. (Retention)	1.27kN/m (98 %)	1.25kN/m (96 %)	1.28kN/m (80 %)
3000hr. (Retention)	1.26kN/m (97 %)	1.20kN/m (92 %)	0.99kN/m (62 %)

Courtesy of RISHO

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650Vdc/20A ½-bridge IPM based on RISHO Substrate

From: PowerAmerica Short Course Nov 2018
Raleigh, NC

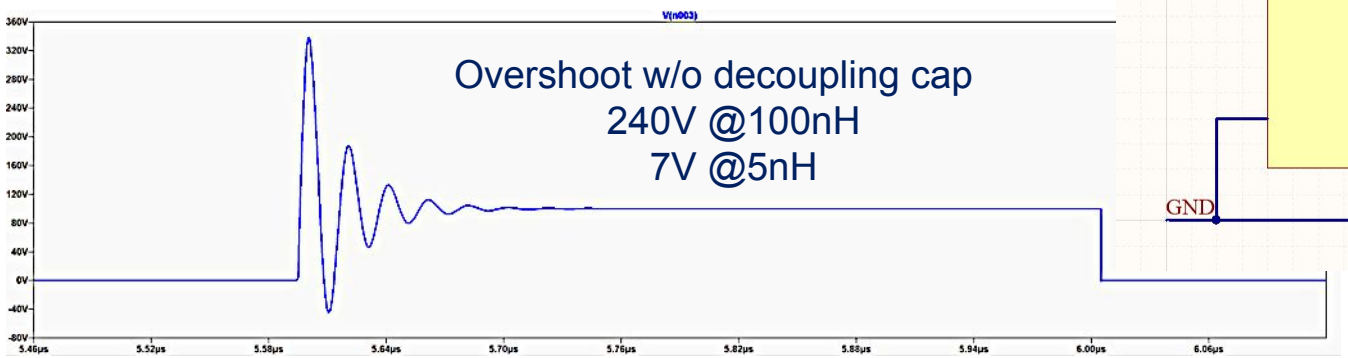
DCHopkins@NCSU.edu
www.PREES.org

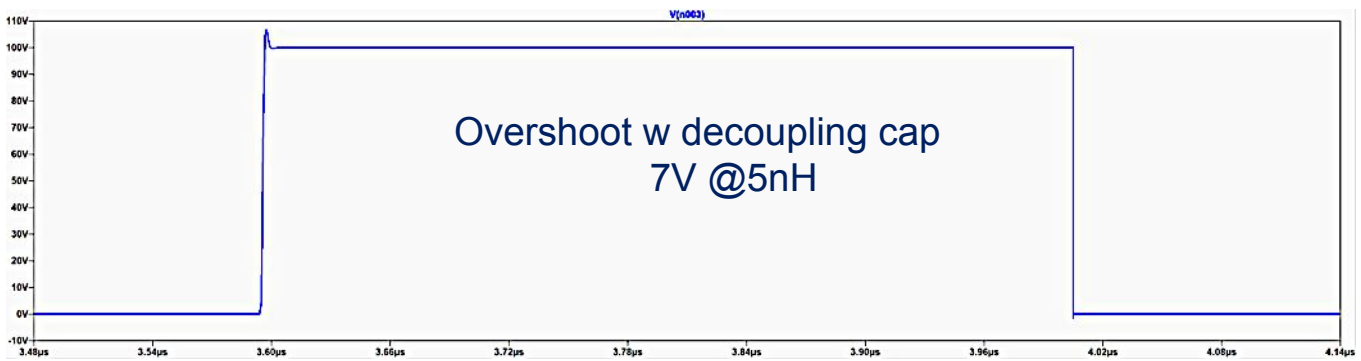
650Vdc/20A ½-bridge IPM based on RISHO Substrate

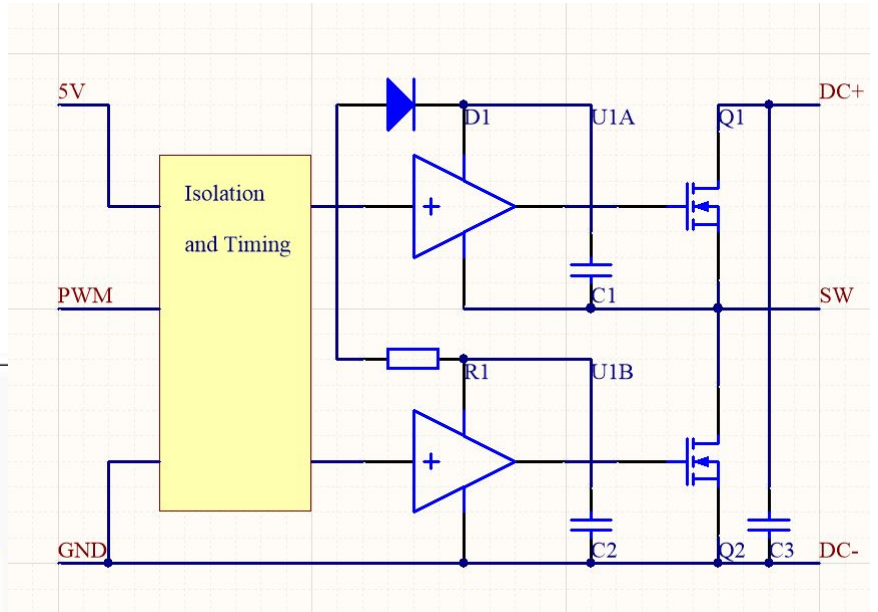
Parameters:

- 650V maximum DC bus voltage
- 20A maximum RMS current per device
- 400V->200V Half-bridge buck
- Internal decoupling cap

IDEAL: Simulation condition: *10A, 100pF C_{oss}*







Parts:
Q1 Q2: Ideal
C1 C2: 10uF 25V X7R
C3: 47nF 1kV X7R
R1: 22Ohm 1/8W
D1: Ideal HF diode
U1: Ideal isolated HB driver

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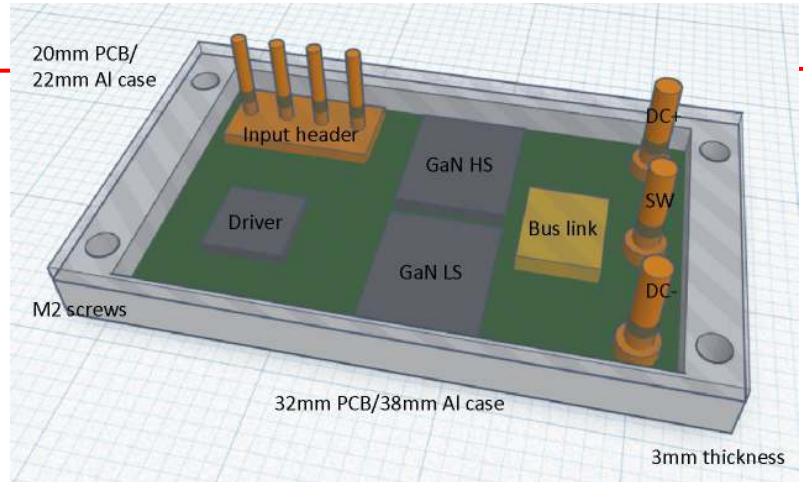
Thermal Analysis



Thermal analysis w/ first order estimation of losses:

P_{rds} = 129m*20A^2 = 51.6W @ Tjmax=150˚C

P_{sw} = 55uJ*0.5MHz = 27.5W @ 400V, 15A

$P_{tot} = P_{rds}+P_{sw}$ = 79.1W

Given:

Die Pad = 6mm X 3mm,

ERCD Substrate thickness = 80µm,

Al case thickness = 0.9mm:

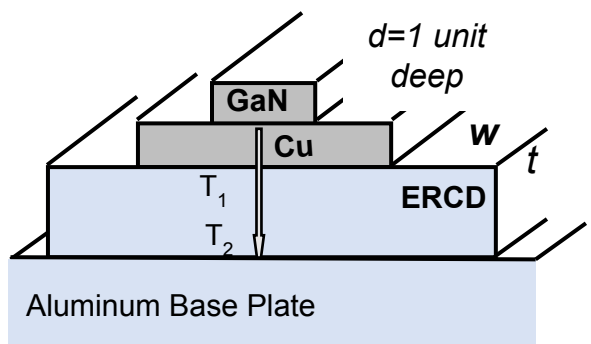
Approximating with 45º rule:

Asub=(6mm+0.04mm)*(3mm+0.04mm)=18.4mm^2

Acase=(6m+0.04mm+0.9mm)*(3mm+0.04mm+0.9mm)=27.3mm

Rsub=0.08mm/18.4mm^2*1000/(10W/m˚C)=0.43 ˚C /W

Rcase=0.9mm/27.3mm^2*1000/(205W/m ˚C)=0.16 ˚C /W



$R_{total} = R_{chip}+R_{sub}+R_{case}$ = 0.5˚C /W+0.43˚C /W+0.16˚C /W = **1.09˚C/W**

At P = 56.5W, T_{case} = 40˚C, Tj = 40˚C+79.1W*1.09˚C/W = 126.2˚C, < Tjmax = 150˚C

Thank you to sponsors:

RISHO

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Inductance & Performance

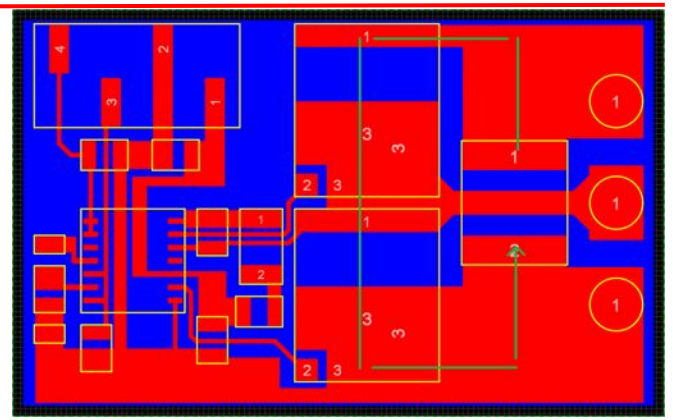
Inductance estimation:

1. Power loop: 6.5nH using rectangle estimation
2. Gate loop: 3.8nH using rectangle estimation

For optimal gate driver at Q=1.5 (0.3V overshoot):

$R = (L/C)^{-1/2} / Q = 2.5\ \Omega,\ L = 3.8nH,\ C = C_{iss} = 0.26nF$

Gate driver has $R_{out} = 2.7\Omega > 2.5$, therefore no R_{ext} is required. Then, simulation shows only 0.26V gate overshoot, well within GaN ratings.



Thank you to GaN Systems, Risho and Electronic Interconnect for supplying parts and processing

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Buck converter with Q1 as switch and Q2 as sync rect.

Full SPICE simulation at 400V->200V 20A:

$L_{pwr\text{-}loop}$ = *6.5 nH*

$L_{gate\text{-}loop}$ = *3.8 nH*

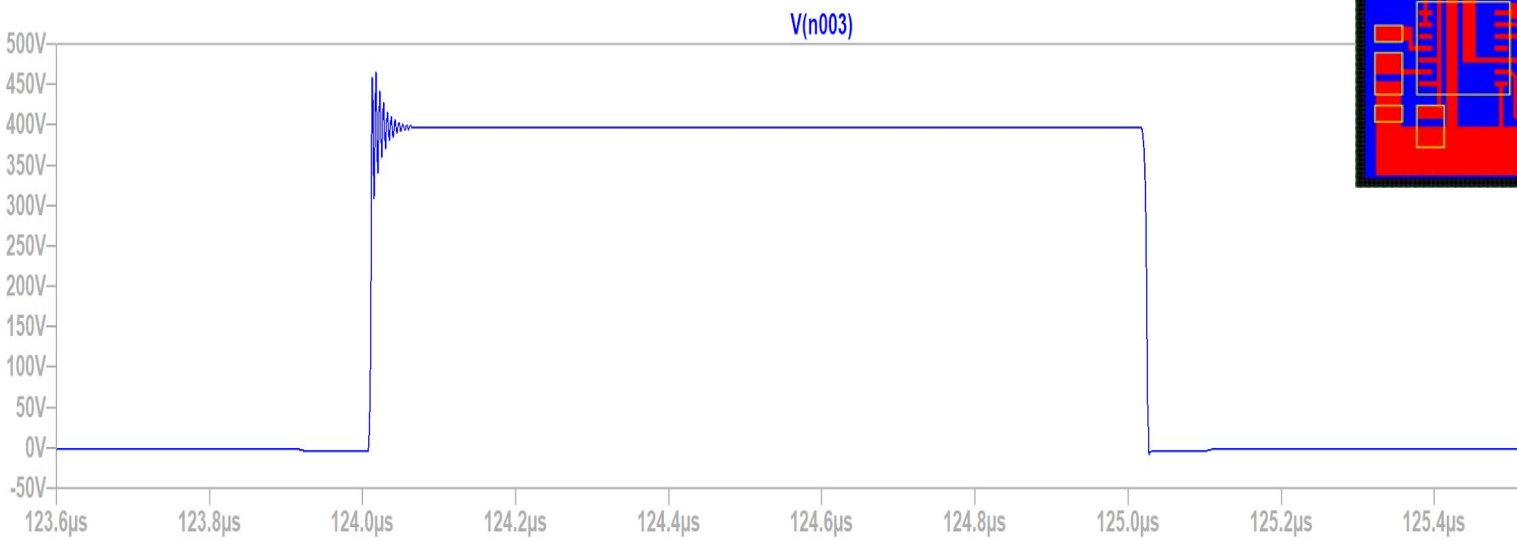
$C_{substrate\ cap}$ = *28.9 pF* (parallel plate method)

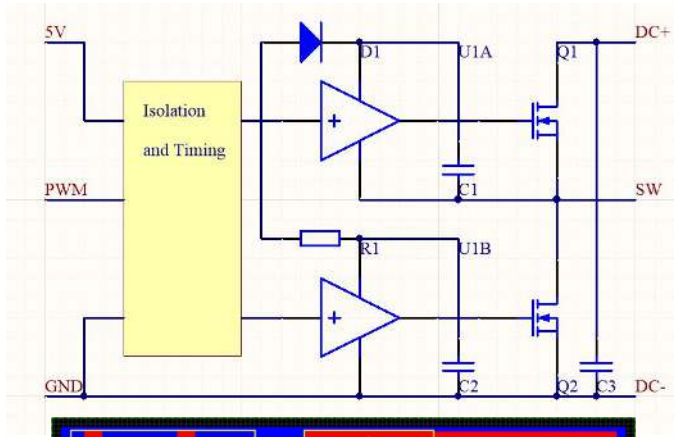
$R_{heatsink}$ = *10Ω* sink-to-Q_{source}

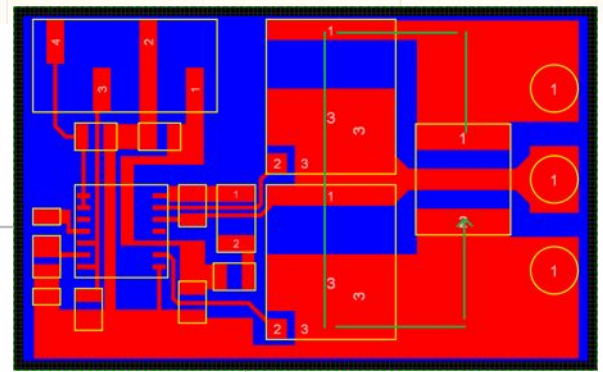
Results:

- P_{loss} = *42.5W* for *Q1, Tj=86.3C*
- P_{loss} = *15.8W* for *Q2, Tj=57.2C*

Switching V_{DS} waveform shows 70 overshoot above the 400V







Parts:
Q1 Q2: GS66508B
C1 C2: 10uF 25V X7R
C3: 47nF 1kV X7R
R1: 22Ohm 1/8W
D1: CURN101-HF diode
U1: Si8274 isolated HB driver
Bottom-side cooled 650V E-mode GaN Systems

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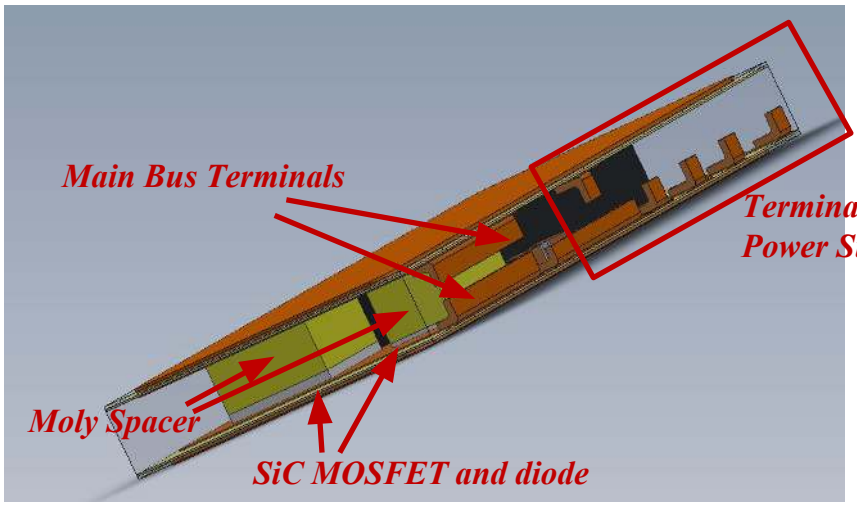
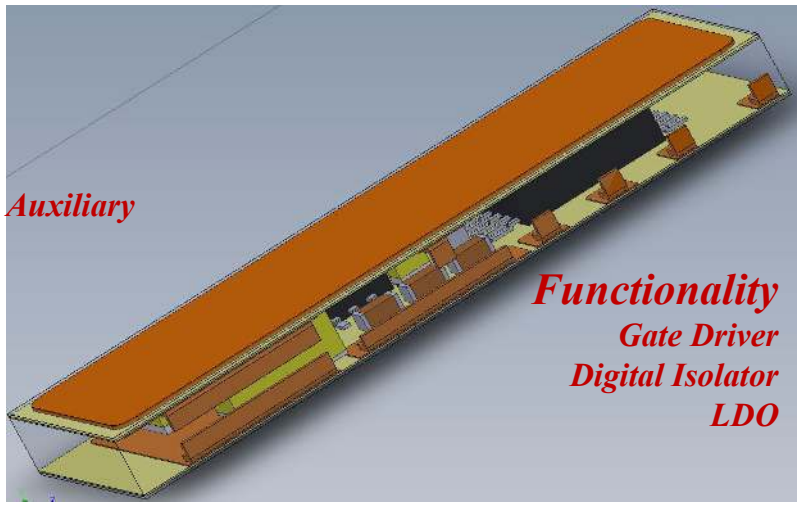
SiC Integrated Power Module Test Design

Excerpt from: Xin Zhao[1] Presentation: “Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,” Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

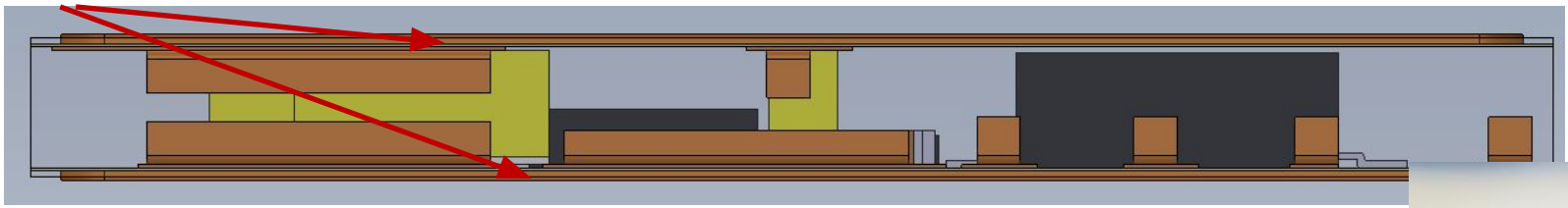
[1] Now at Univ. of Texas at Austin

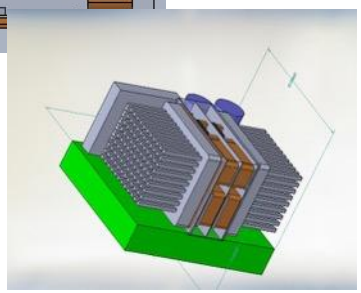
Double Sided Design





Substrates on Double Side



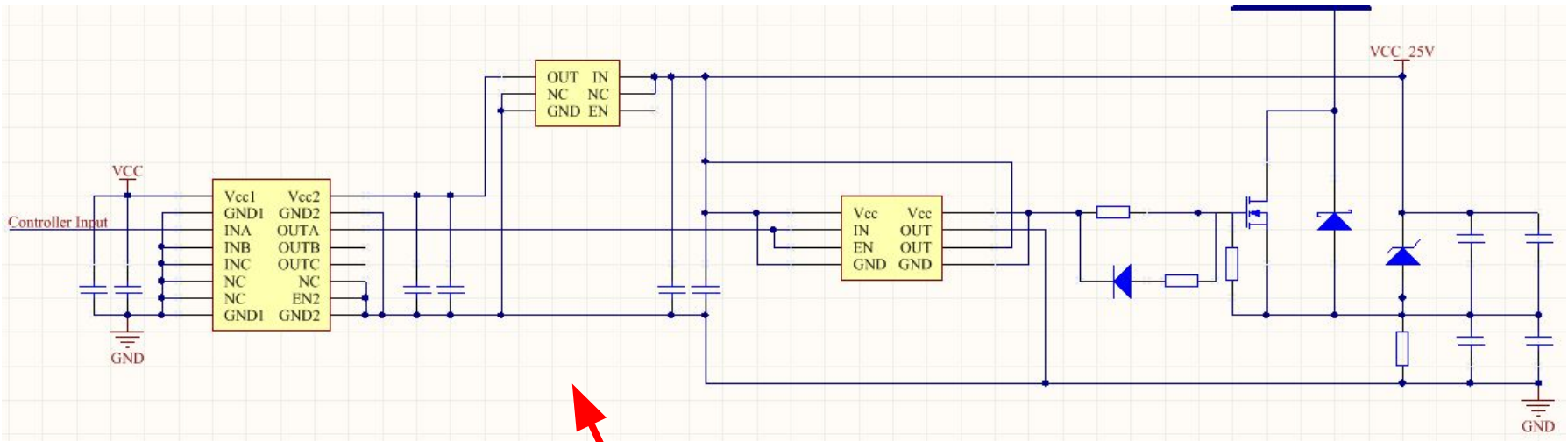


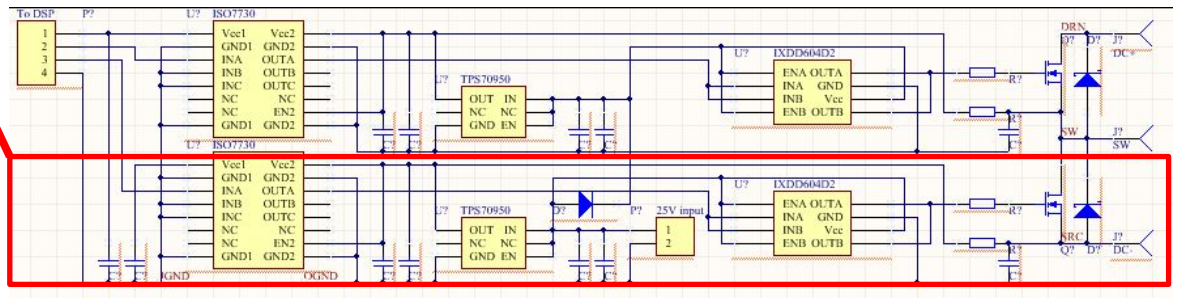
- Volume: 35 mm × 15.5 mm × 3mm
- Power Devices: CPM2-1200-0025B / CPW5-1200-Z050B
- Rating: 800 V/ 40 A
- Auxiliary terminals on single side of the module, allowing for both side heat sink attachment, with terminals able to attached on PCB for interconnections

From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

SiC IPM Design

Circuit Schematic Design





Schematic Design for SiC half bridge IPM

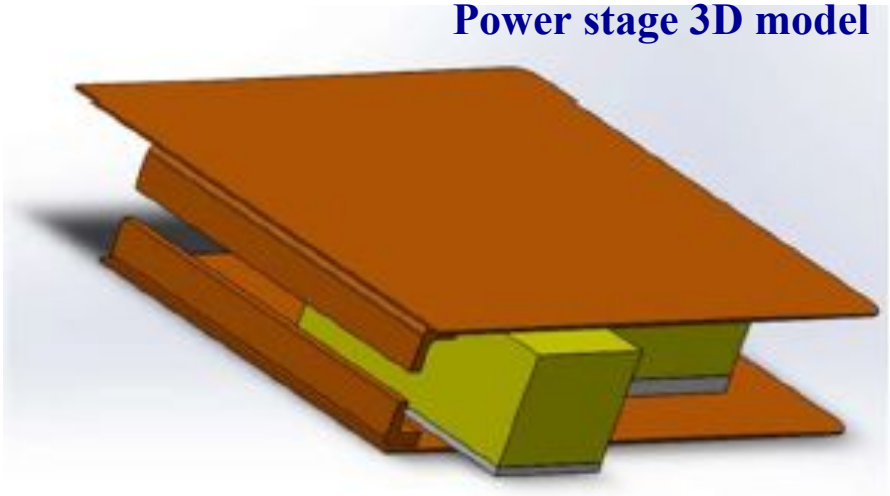
- Boostrap Power Supply
- Digital Isolator
- LDO
- Gate driver Circuits
- -5V turn-off power supply
- Single switch pair IPM is developed as initial investigation

From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

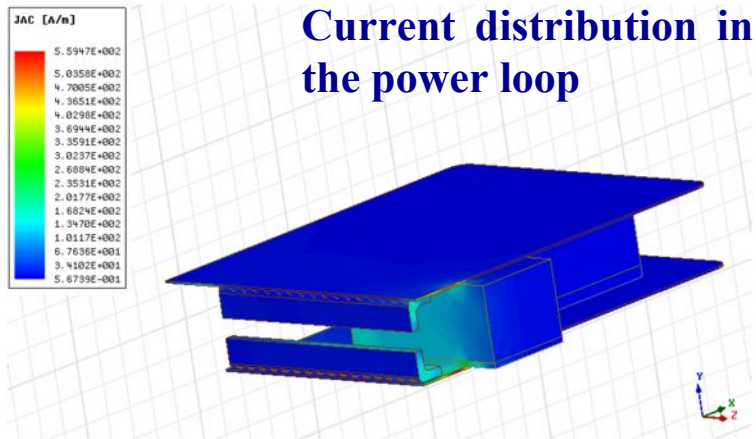
Simulation of the SiC IPM Design

Simulation for Parasitic Extraction

Power stage 3D model



Current distribution in the power loop



Summary of extracted parasitics

Location	Inductance / nH	Resistance / mΩ
DC+ → DC-	0.6	0.22
MOSFET Drain	0.44	0.20
MOSFET Source	0.20	0.10
Diode Anode	1.87	0.38
Diode Cathode	2.23	0.46

- Inductance in the entire loop is 0.6 nH.
- Diode inductance is larger, since it parallels the MOSFET drain to source.
- Applicable for lower losses and higher operation frequency.

From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

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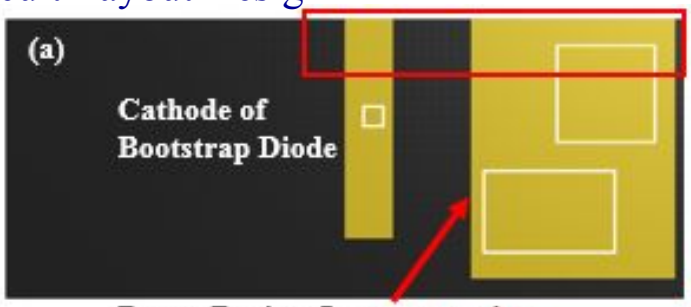
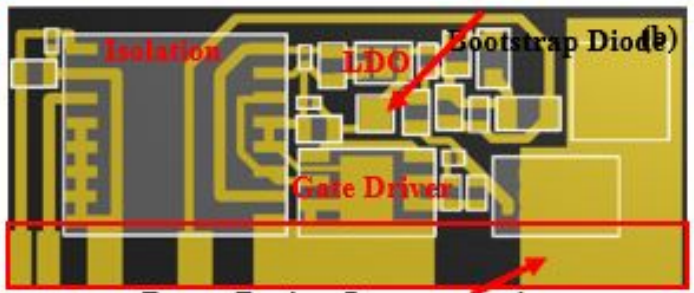
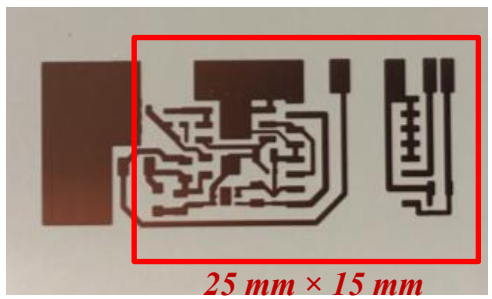
SiC-IPM Layout

Circuit Layout Design

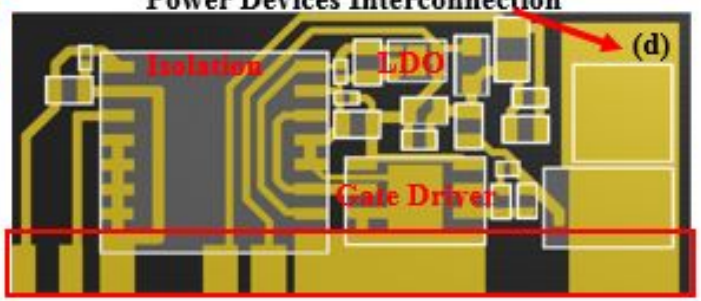


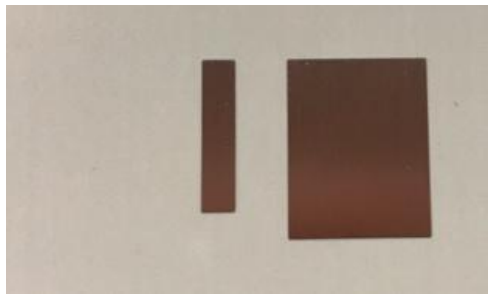




Power Devices Interconnection

Power Devices Interconnection





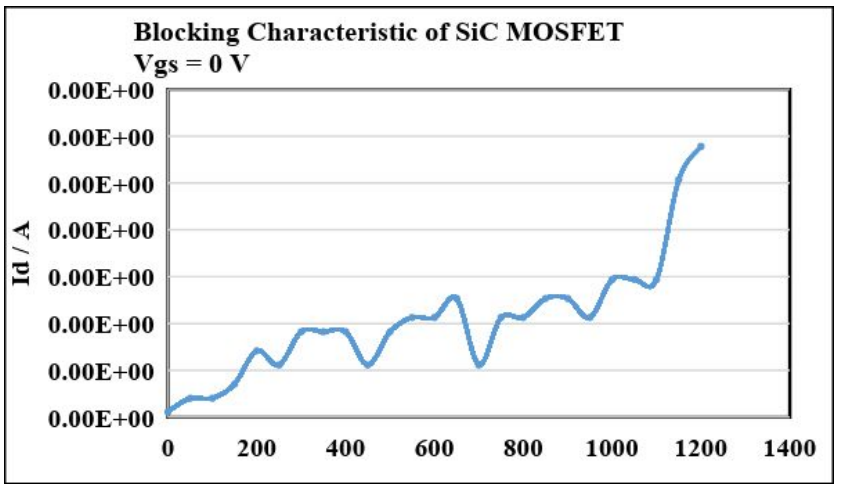
Layout design for the SiC half bridge IPM

- Interconnections are applied to both top and bottom side of substrates
- Interconnection metal in the main power loop is a copmprise between thermal spreading and EMI nosie reduction
- Only the layout (c) and (d) are discussion in the presentation for the single switch module
- The layout design is not optimized and the long gate loop trace on the plane, results in excessive noise during switching
- Jumper wire minimizes gate loop length during the fabrication for demonstration of the design

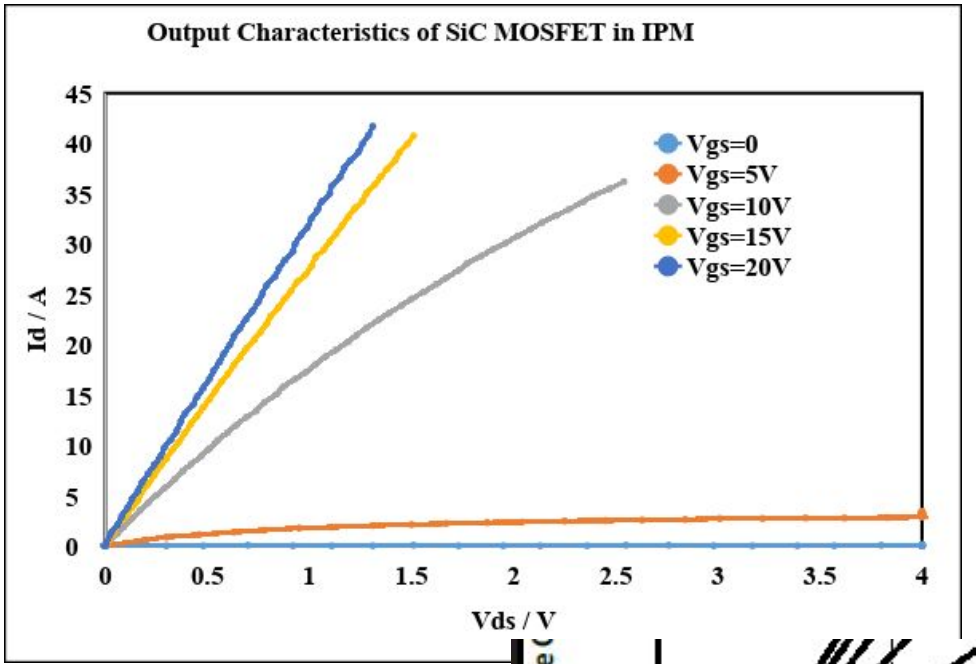
From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

SiC IPM Fabrications & Measurements

Module Assembly & MOSFET Statics Test

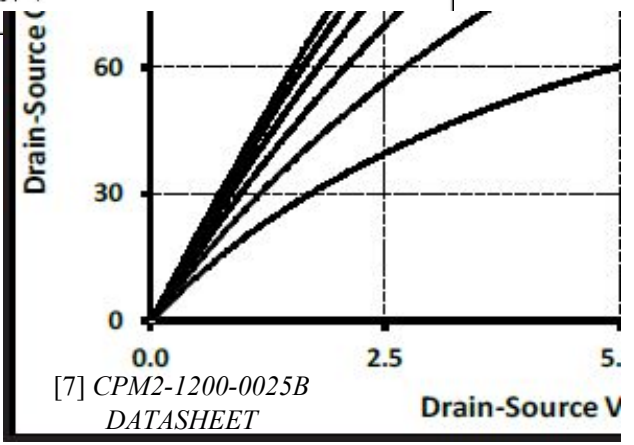


I_{DSS}	Zero Gate Voltage Drain Current		2	100	μA



The forward and reverse characteristics of SiC MOSFET is similar with data shown on the datasheet[7].

The proposed module fabrication and assembly process, including the topside metallization process of SiC devices, can fully exhibits the initial performance of the SiC devices



[7] *CPM2-1200-0025B DATASHEET*

From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

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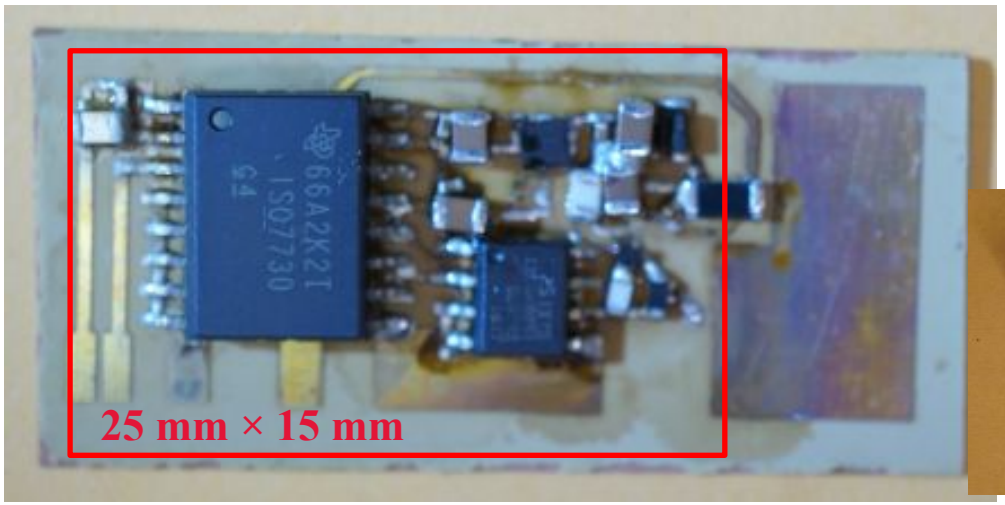
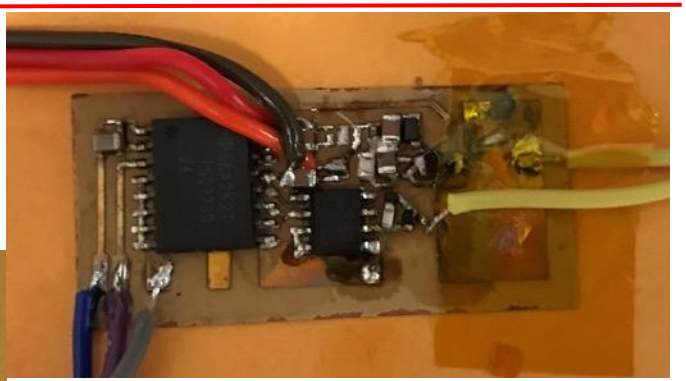
SiC IPM Fabrications & Measurements

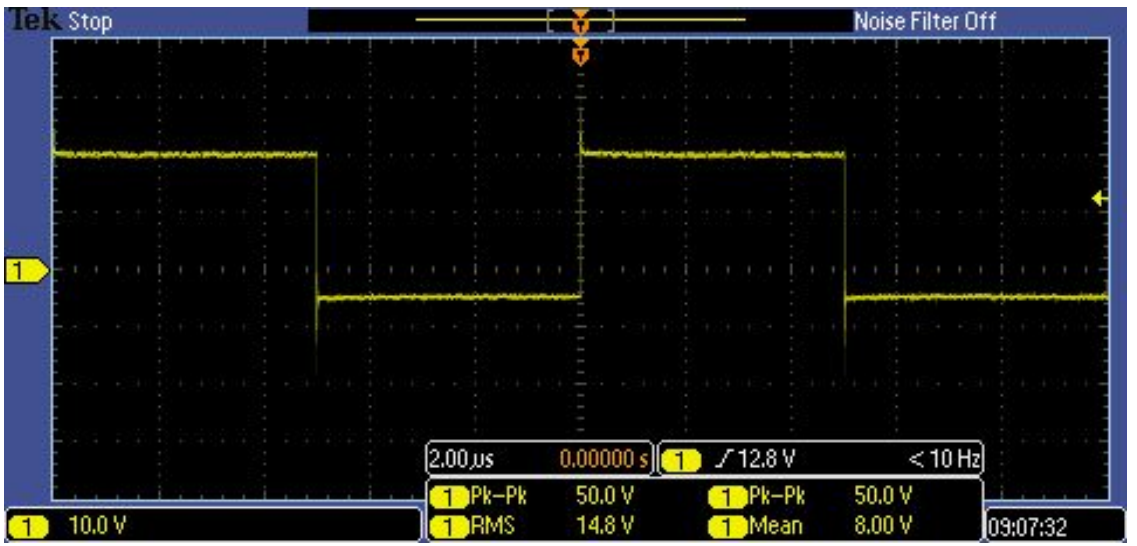
Module Assembly & Driver Circuits Test





- Gate pad is on same plane as gate driver, output signal verified for -5V turn-off and 20V turn-on of MOSFET

- Flip-chip assembly for SiC MOSFET and Diode
- Underfill applied for 1200V isolation
- Large terminals for testing



From Xin Zhao Presentation: "Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, Yifan Jiang, Bo Gao, Kenji Nishiguchi, Yoshi Fukawa, Douglas C. Hopkins, IEEE 67th ECTC, Orlando, FL May 30 – Jun 02, 2018

DCHopkins@NCSU.edu
www.PREES.org

Conclusions

- Selection Criterion of Thin dielectric substrate material is set up based on design requirements of 1200V WBG device based IPMs.
- A 120μm recently developed flexible epoxy-resin based dielectric, by Risho Kogyo Co., Ltd., is investigated, and proved to be suitable for power module substrate in terms of electrical, thermal, mechanical properties, cost, and reliability.
- A high-density half-bridge SiC power module is designed with ultra-low parasitics, utilizing epoxy-resin based dielectric, for high-frequency and low-loss applications.
- Fabrication process of double-side solderable SiC MOSFETs and diodes is developed, capable of deposition of metallization layer up to 2μm.
- A single-switch SiC power module with more functionality is fabricated, allowing for double-side cooling functions, verified by static measurements.
- The proposed substrate material, and designed WBG IPM with ultra-low parasitics, high functionality and double-side cooling is verified and show potential for high frequency and high power density applications.

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End

Prof. Douglas C. Hopkins, Ph.D.
Director – PREES Laboratory
FREEDM System Center
North Carolina State Univ.
1791 Varsity Dr., Suite 100
Raleigh, NC 27606-7571
919-513-5929
DCHopkins@NCSU.Edu
www.prees.org