FREEDM SYSTEMS CENTER

Medium-Voltage Modular Extreme Fast Charging System

Our webinar will begin in a few minutes.

Introduction

- Welcome
- FREEDM Overview
- Zoom Functionality

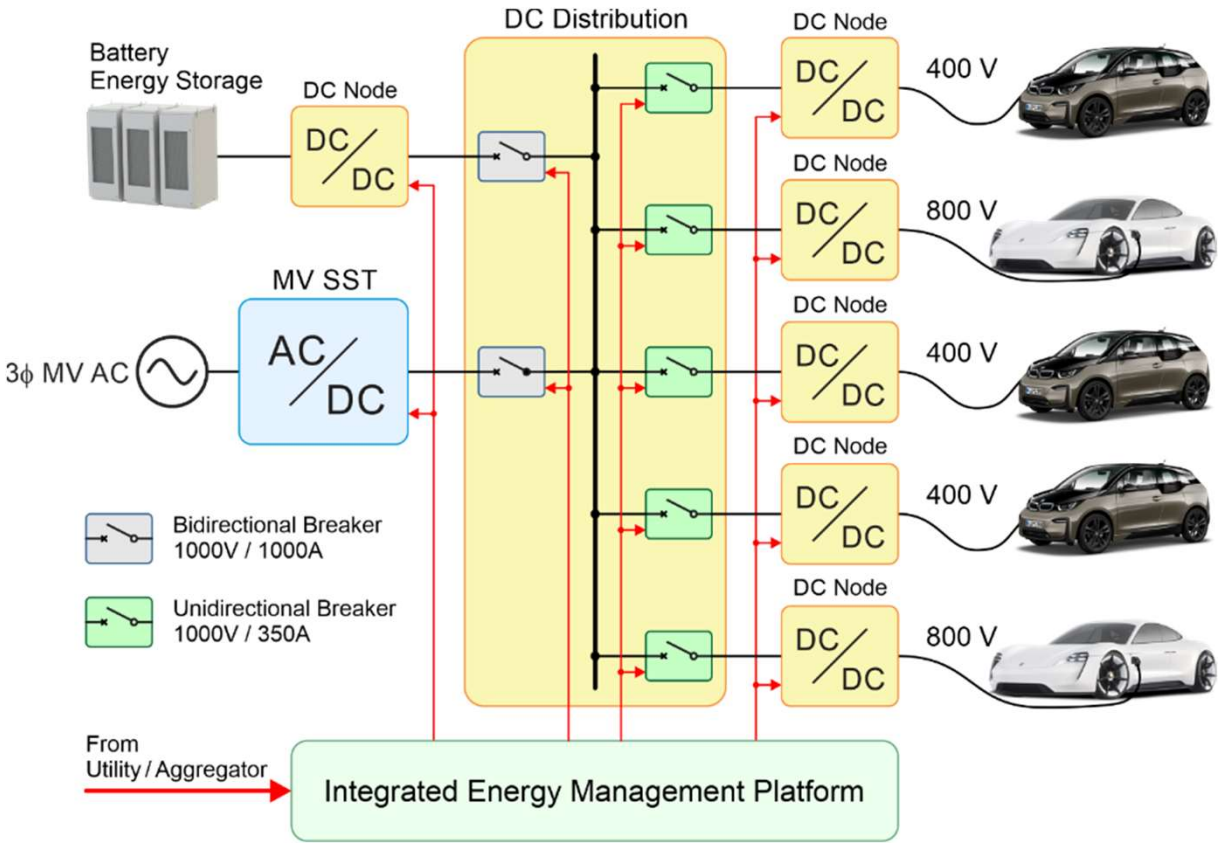
freedm.ncsu.edu

Technical Overview

Develop and deploy a 1 MW medium voltage XFC station:

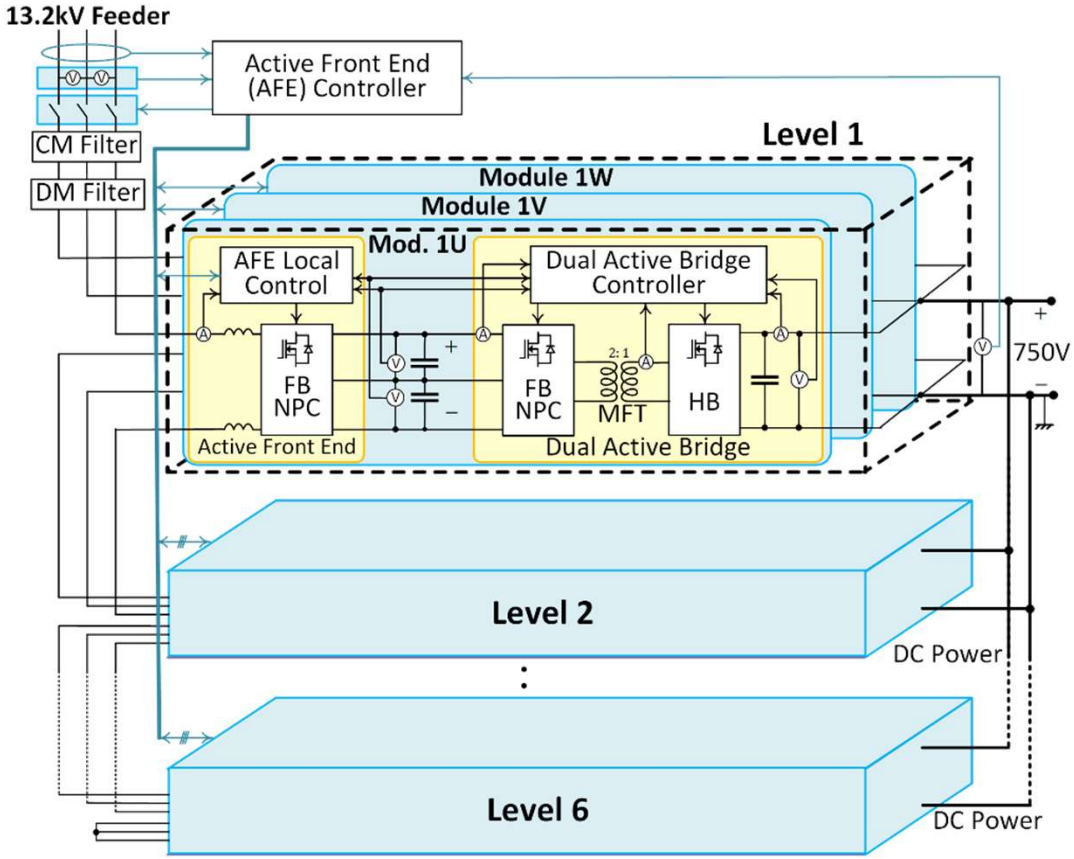
- Shared bi-directional Solid State Transformer (SST) connecting directly to the medium voltage (MV) distribution system
- DC distribution network with solid-state DC protection
- Energy management platform
- DC Nodes for local isolation and DC/DC conversion

Technical Overview



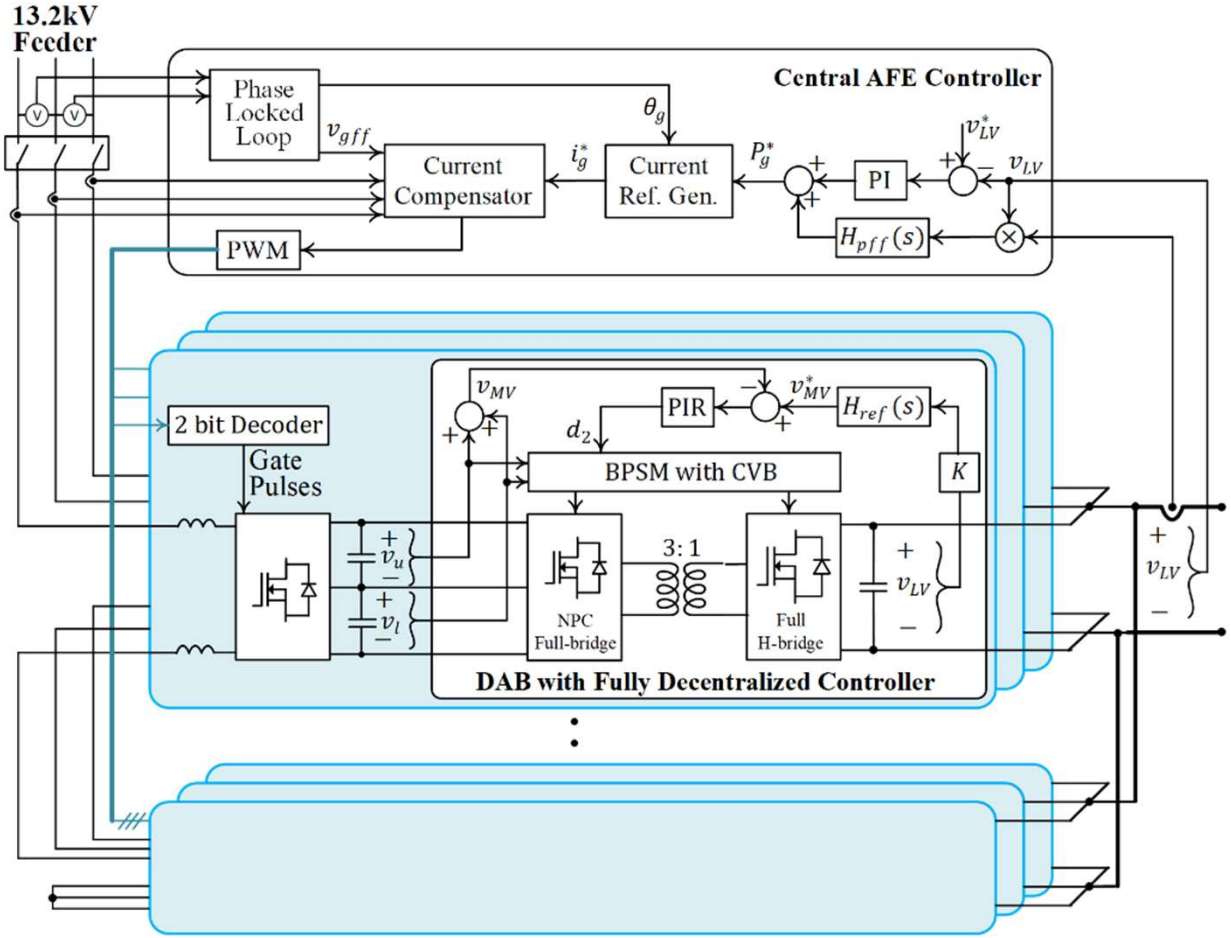
SST Architecture

- The SST connects to three-phase 13.2kV$_{LL}$ input and delivers 750V DC
- A total of 18 modules are arranged in 6 levels using input-series output-parallel configuration
- Each level is made up of three modules processing three-phase power on the input and delivering DC power at the output
- Each module consists of an active front end (AFE) and dual-active-bridge (DAB) isolated DC-DC stage



Design Approach & Control Architecture

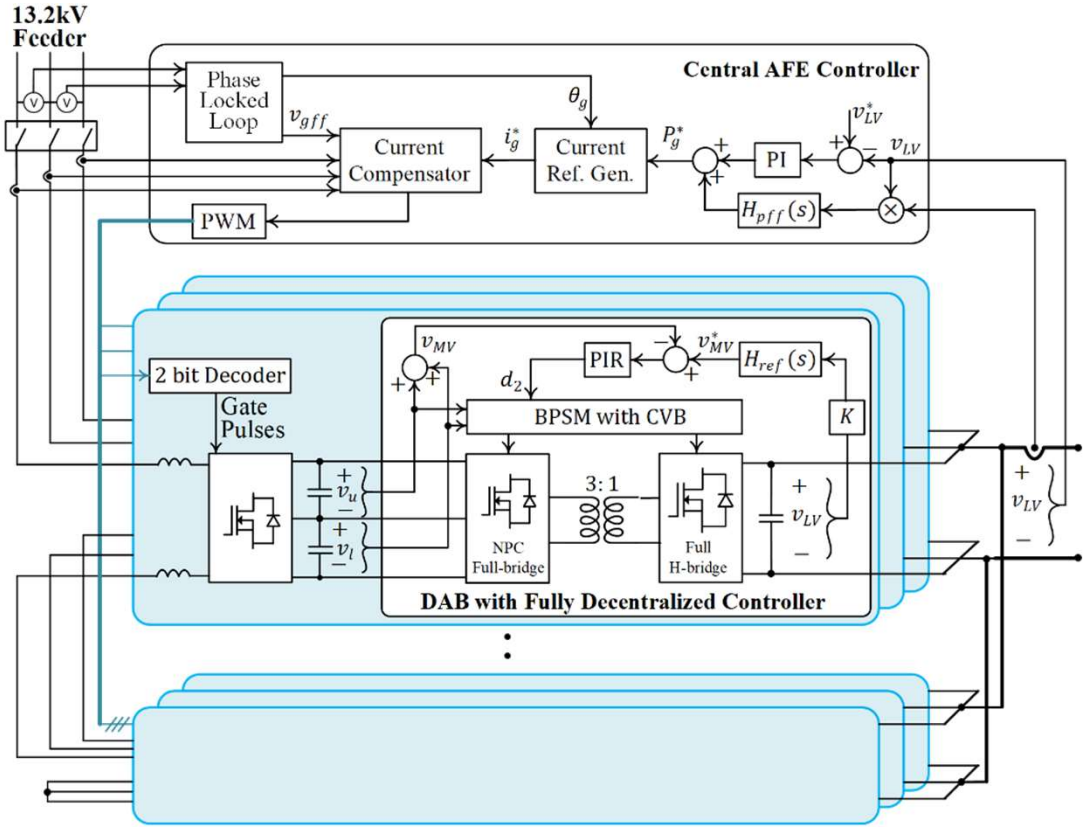
- Each Dual active bridge (DAB) autonomously regulates its medium voltage (MV) bus, minimizing communication requirements
- Centralized controller for all AFEs with local protection and decoding
- Interleaved modulation of AFEs and low voltage (LV) side bridges of DABs
- DABs designed for sinusoidal power flow, minimizing storage requirements on MV DC capacitors
- Solid-state protection on MV and LV



$H_{ref}(s)$ and $H_{pff}(s)$ are low-pass filters
PIR -- Proportional Resonant Integral Controller
BPSM with CVB -- Bidirectional phase-shift modulator with capacitor voltage balancing

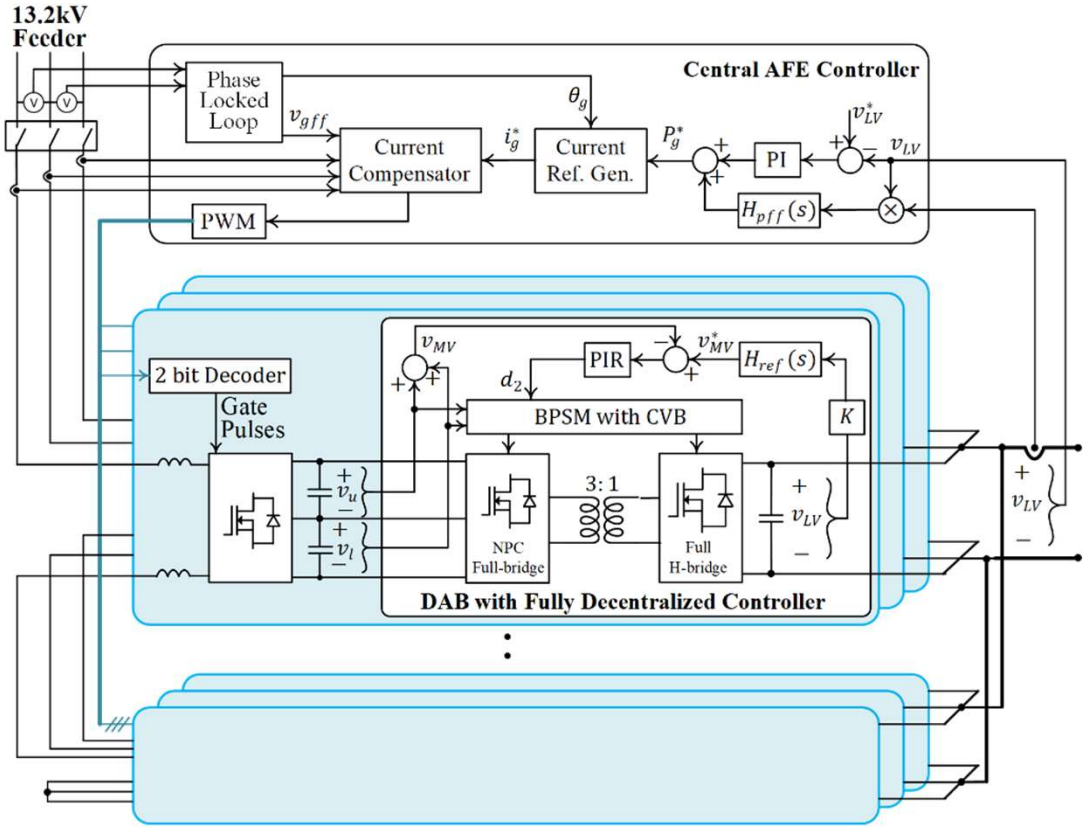
AFE Control

- A central controller is used for the active front-end converter stages
- Based on the LVDC bus voltage feedback, grid power reference P_g^* is generated ; load current measurement of the LVDC bus is used as a feedforward
- A stationary frame current compensator is used
- 2-bit encoded PWM signal sent to each AFE stage



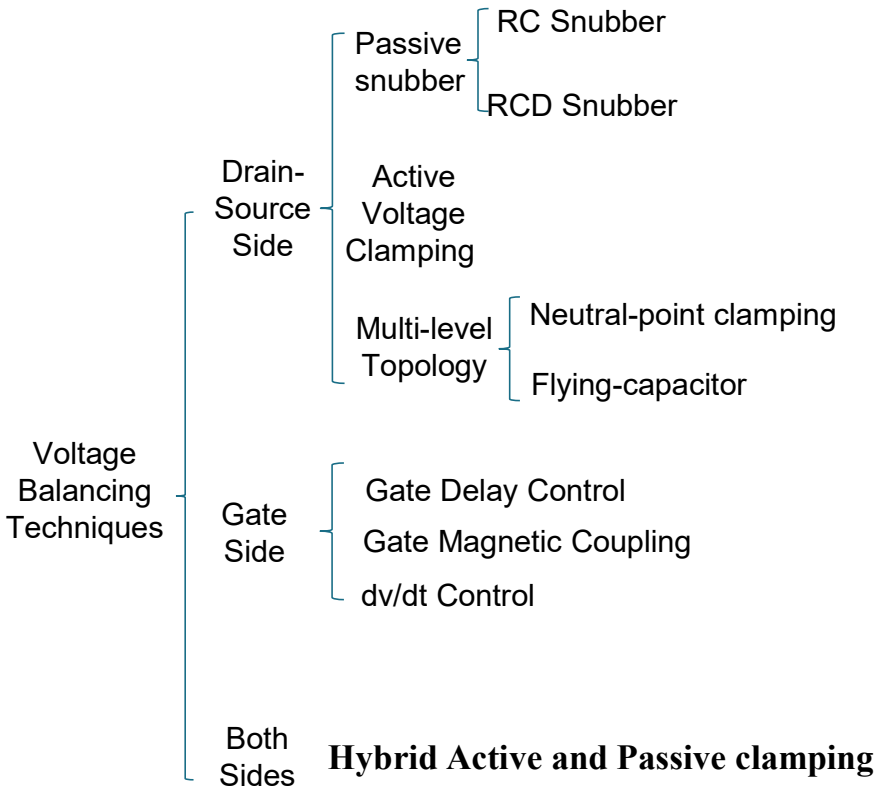
Background for AFE

- For Active Front-end
  - A total of 18 modules are arranged in 6 levels for 3 phase
  - 85kW for each module
  - 2.15kV DCBUS for each module
  - Unavailable commercial SiC MOSFETs above 1.7kV



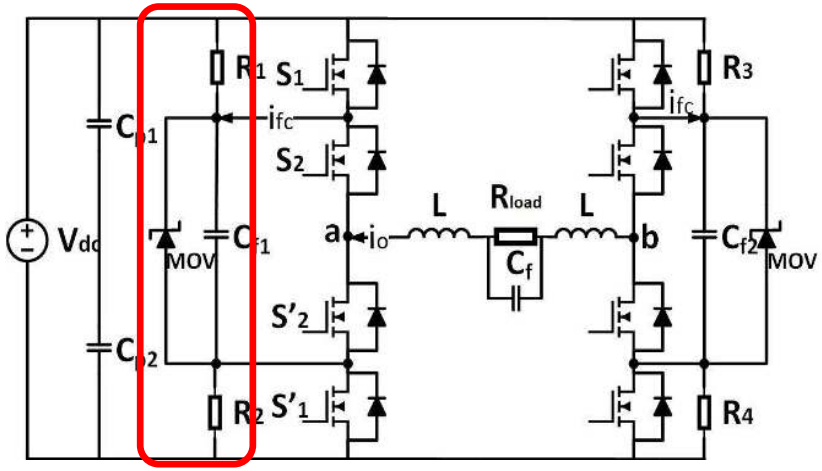
Series-Connection State-of-the-art

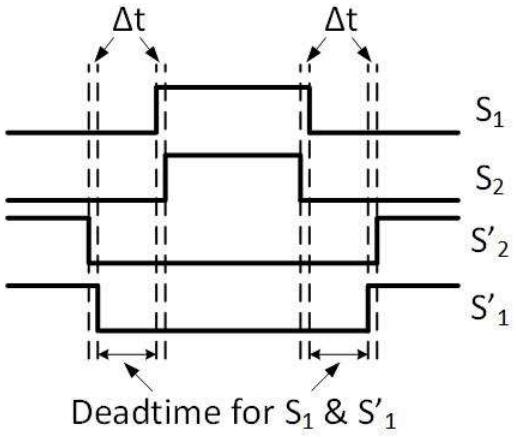
- Drain-source side solution suffers high power loss, bulky passive snubbers
- Gate-side solution suffers complex voltage sensing and advanced gate driver
- The proposed solution has small passive snubbers and eliminated the complex voltage sensing



Proposed Hybrid Series-Connection Technique

- For passive clamping
  - One clamping circuit for four switches
  - Power loss is around 1W for 10kW output power (0.01%)
- For active gating
  - Standard gate driver and DSP with HRPWM
  - Pre-defined modulation based on Rectifier Effect of FC
  - No voltage/current sensing
  - No voltage balancing control

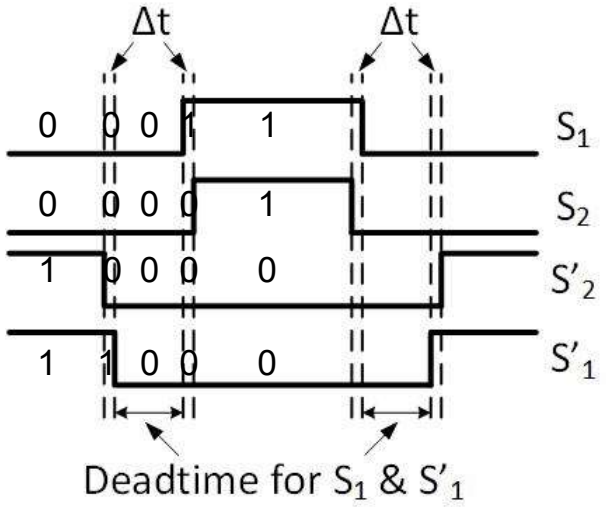


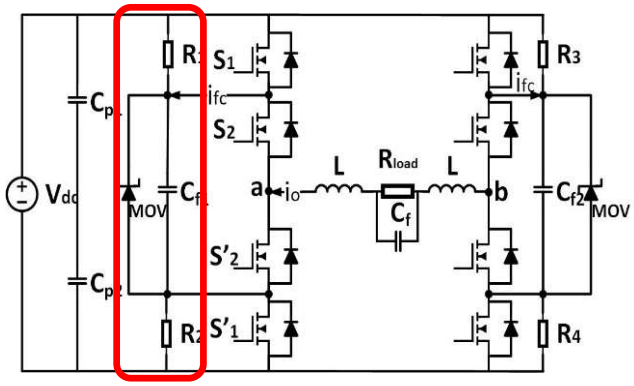


Operating Principle Based on Rectifier Effect

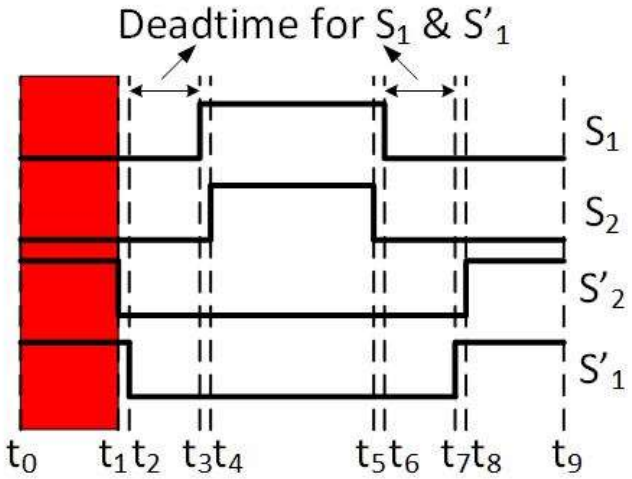
- **Rectifier Effect** of flying capacitor topology
  - Predefined modulation scheme eliminates 4 switching states, while keeping the full control capability of the switches in series
  - Remained 5 switching states ensure ifc rectified from AC current during a very short interval, which is independent of voltage, power factor, and current

No.	S_1	S_2	S'_2	S'_1	i_o	i_{fc}
1	1	1	0	0	+ / -	0 / 0
2	1	0	1	0	+ / -	+ / -
3	0	1	0	1	+ / -	- / +
4	0	0	1	1	+ / -	0 / 0
5	1	0	0	0	+ / -	+ / 0
6	0	1	0	0	+ / -	- / 0
7	0	0	1	0	+ / -	0 / -
8	0	0	0	1	+ / -	0 / +
9	0	0	0	0	+ / -	0 / 0

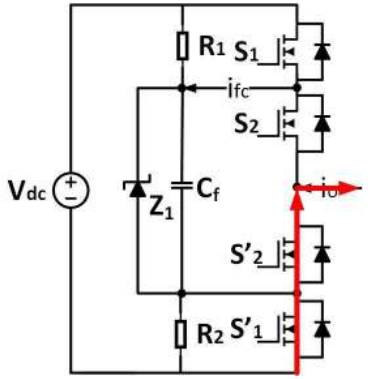




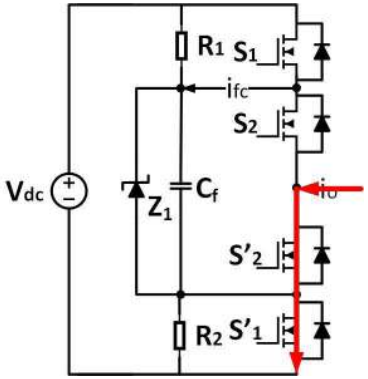
Operating Principle Based on Rectifier Effect



S_1	S_2	S'_2	S'_1	i_o	i_{fc}
0	0	1	1	+ / -	0 / 0
0	0	0	1	+ / -	0 / +
0	0	0	0	+ / -	0 / 0
1	0	0	0	+ / -	+ / 0
1	1	0	0	+ / -	0 / 0
1	0	1	0	+ / -	+ / -
0	1	0	1	+ / -	- / +
0	1	0	0	+ / -	- / 0
0	0	1	0	+ / -	0 / -

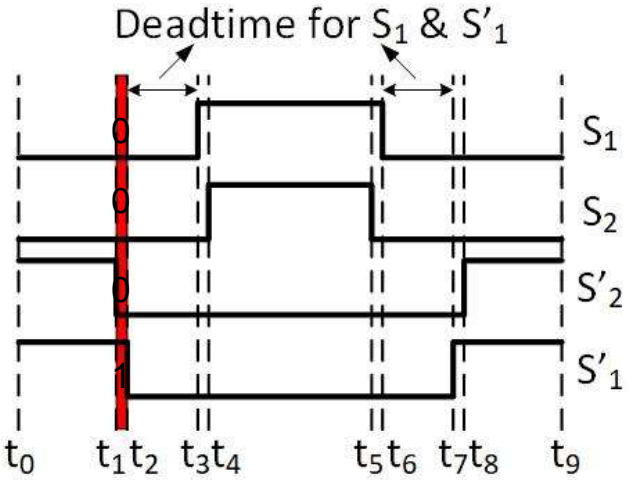


$i_o > 0$

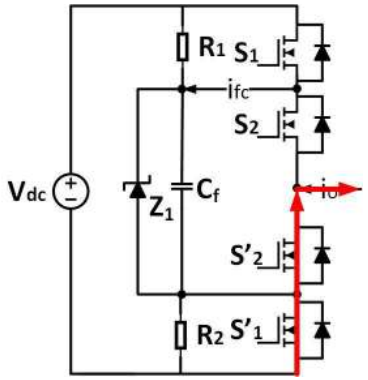


$i_o < 0$

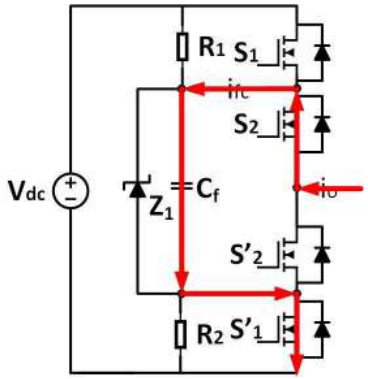
Operating Principle Based on Rectifier Effect



S_1	S_2	S'_2	S'_1	i_o	i_{fc}
0	0	1	1	+ / -	0 / 0
0	0	0	1	+ / -	0 / +
0	0	0	0	+ / -	0 / 0
1	0	0	0	+ / -	+ / 0
1	1	0	0	+ / -	0 / 0
1	0	1	0	+ / -	+ / -
0	1	0	1	+ / -	- / +
0	1	0	0	+ / -	- / 0
0	0	1	0	+ / -	0 / -

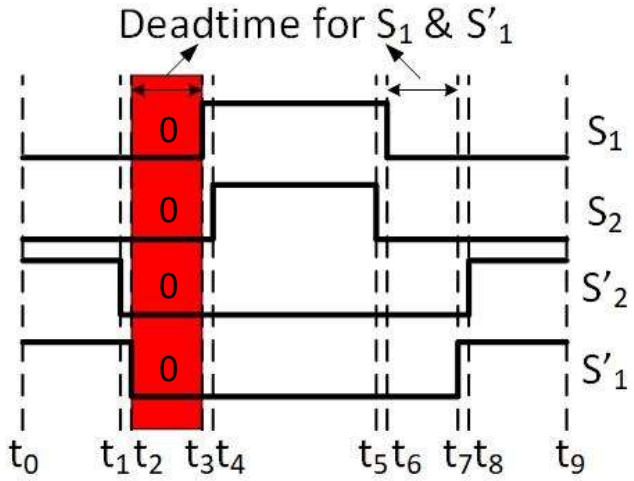


$i_o>0$

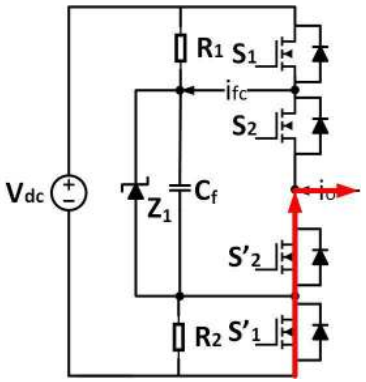


$i_o<0$

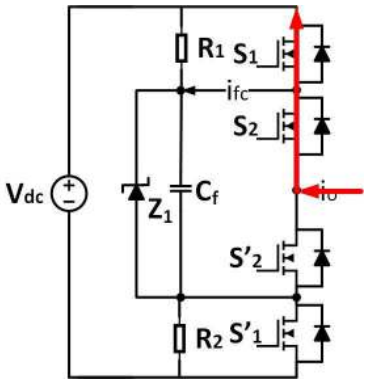
Operating Principle Based on Rectifier Effect



S_1	S_2	S'_2	S'_1	i_o	i_{fc}
0	0	1	1	+ / -	0 / 0
0	0	0	1	+ / -	0 / +
0	0	0	0	+ / -	0 / 0
1	0	0	0	+ / -	+ / 0
1	1	0	0	+ / -	0 / 0
1	0	1	0	+ / -	+ / -
0	1	0	1	+ / -	- / +
0	1	0	0	+ / -	- / 0
0	0	1	0	+ / -	0 / -

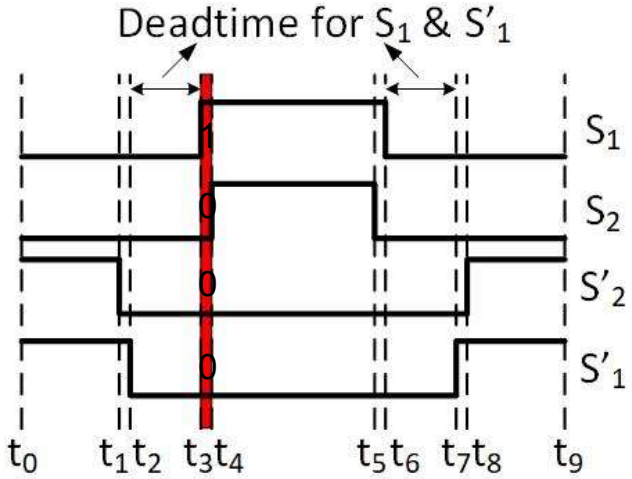


$i_o>0$

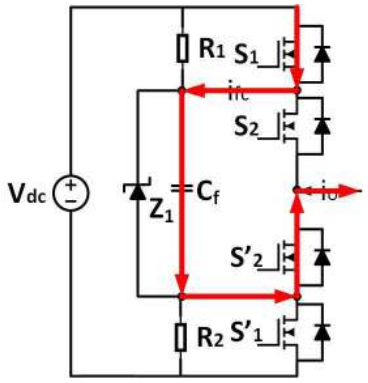


$i_o<0$

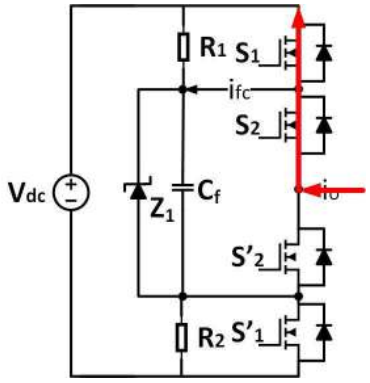
Operating Principle Based on Rectifier Effect



S_1	S_2	S'_2	S'_1	i_o	i_{fc}
0	0	1	1	+ / -	0 / 0
0	0	0	1	+ / -	0 / +
0	0	0	0	+ / -	0 / 0
1	0	0	0	+ / -	+ / 0
1	1	0	0	+ / -	0 / 0
1	0	1	0	+ / -	+ / -
0	1	0	1	+ / -	- / +
0	1	0	0	+ / -	- / 0
0	0	1	0	+ / -	0 / -

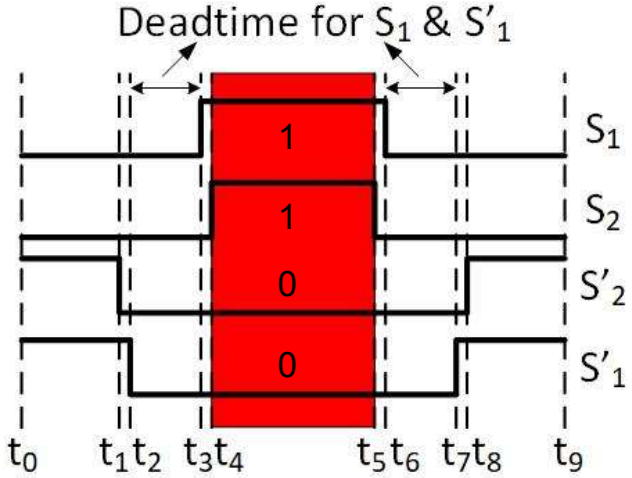


$i_o > 0$

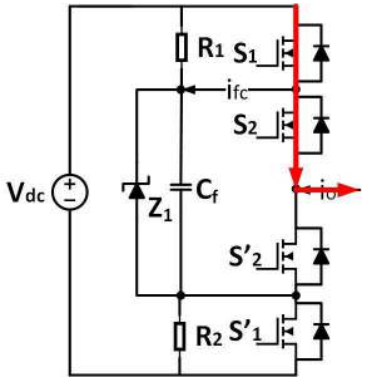


$i_o < 0$

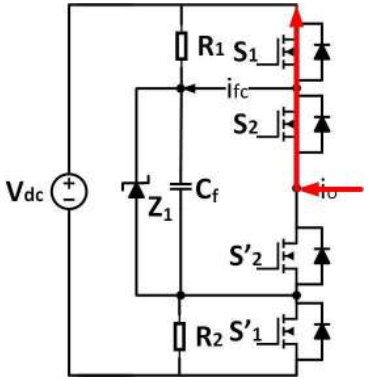
Operating Principle Based on Rectifier Effect



S_1	S_2	S'_2	S'_1	i_o	i_{fc}
0	0	1	1	+ / -	0 / 0
0	0	0	1	+ / -	0 / +
0	0	0	0	+ / -	0 / 0
1	0	0	0	+ / -	+ / 0
1	1	0	0	+ / -	0 / 0
1	0	1	0	+ / -	+ / -
0	1	0	1	+ / -	- / +
0	1	0	0	+ / -	- / 0
0	0	1	0	+ / -	0 / -



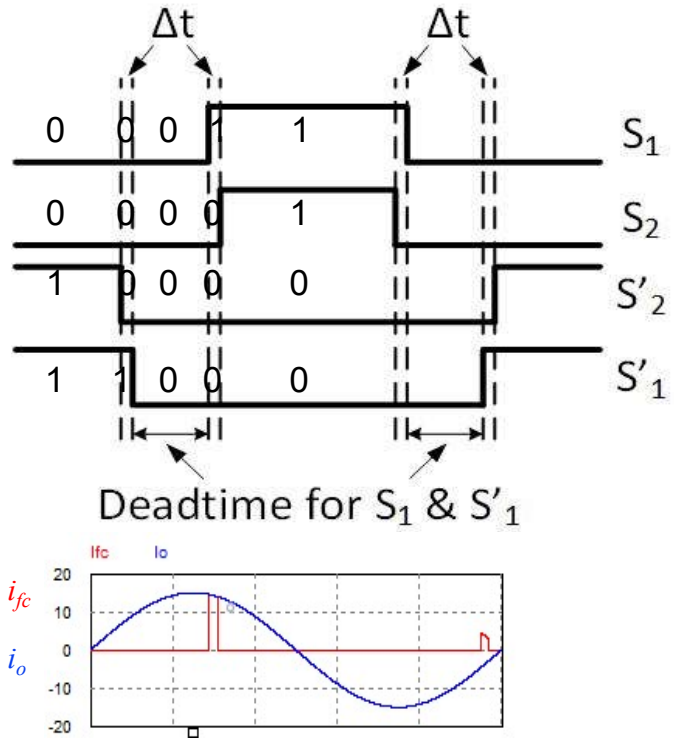
$i_o>0$



$i_o<0$

Operating Principle Based on Rectifier Effect

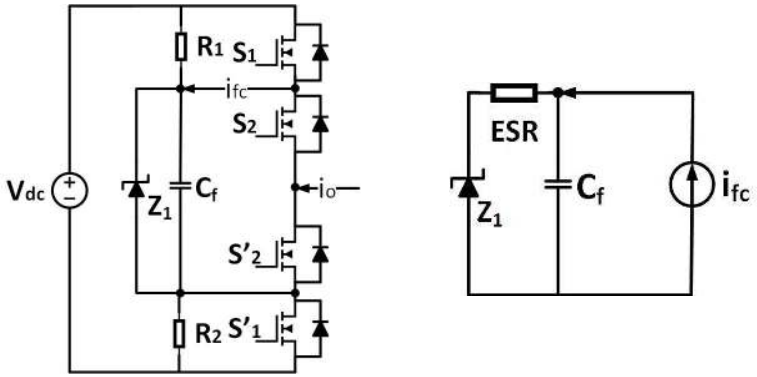
- Simple law of rectifier effect
  - $i_{fc} \geq 0$ as long as $\Delta t > 0$
  - Always turn on outer switches first and turn off inner switches first
- *Δt* is the effective time interval to charge flying capacitor. The shorter *Δt,* the less power loss on clamper
- If i_o direction unchanged within one switching period, two of four *Δt* will be zero and the other two equal to load current within *Δt*

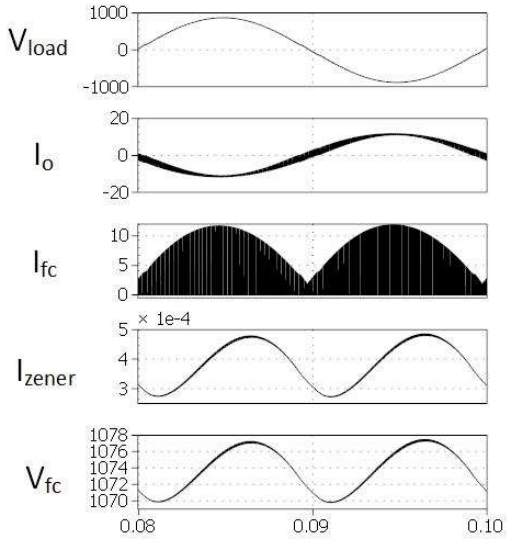


Clamping Circuit Design

- Clamping voltage is approximately half of nominal DCBUS voltage
- Flying cap and clamper ESR act like low-pass filter for current source i_{fc} to suppress the current spike
- Based on simulation, adjust C_f to make the voltage ripple less than 1% of rated voltage at full power
- Start-up resistors are less than resistance of Z_1 below breakdown voltage and large enough to limit the leakage current

Parameters	Value	Parameters	Value
C_{f1}	68nF	DCBUS voltage	2kV
V_{zener}	1060V	Switching frequency	20kHz
R_{zener}	$36k\Omega$	Deadtime	0.5us
$R_1 \& R_2$	$10M\Omega$	Δt	1ns
SiC MOSFET	$1700V/45m\Omega$	Load current	8.3A





Power Loss on Clamping Circuit

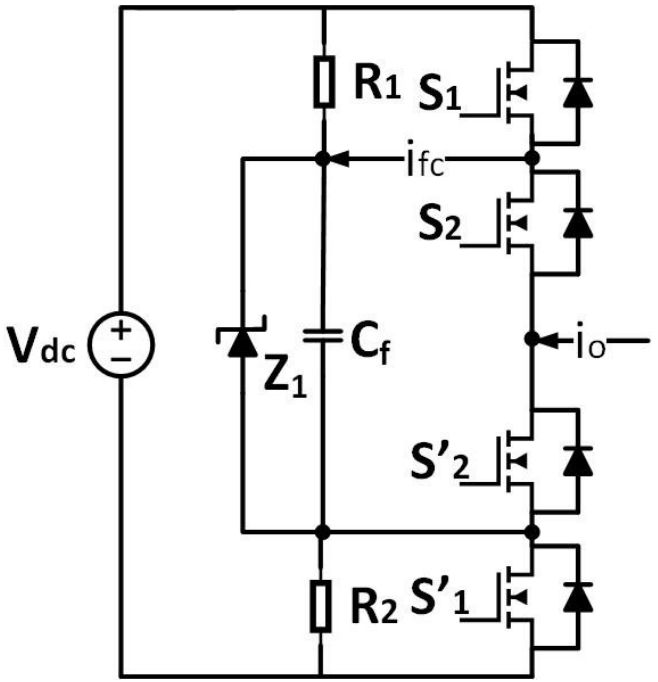
- Assumptions:
  - i_o direction unchanged within one switching period
  - Deadtime is negligible compared to switching period
- Start-up circuit leakage current

$$I_{start-up} \approx \frac{V_{dc} - V_{cf}}{10M\Omega} \approx 0.1mA.$$

- Average value of clamper current

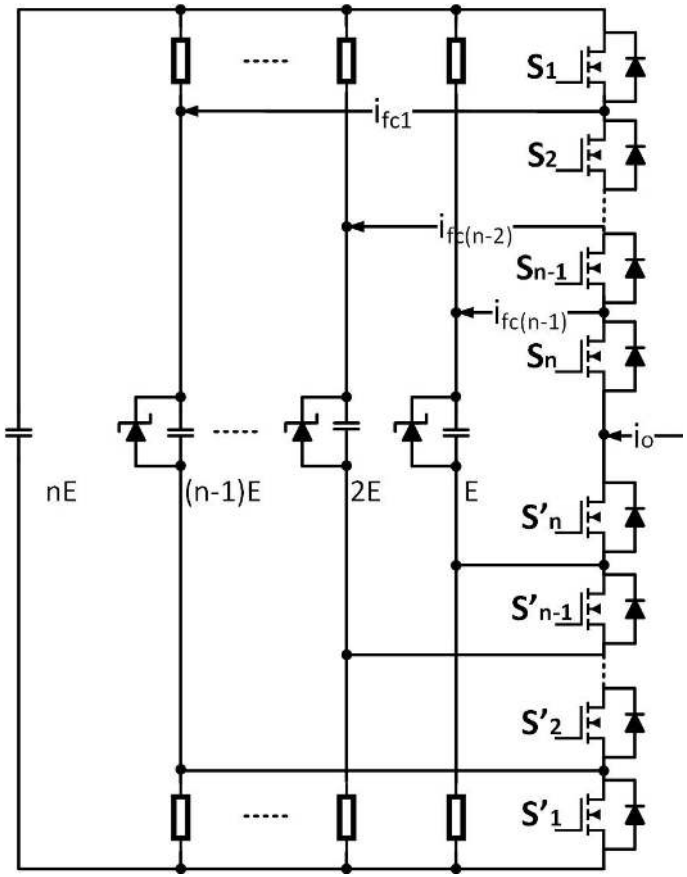
$$\bar{I}_{clamper} \approx 2 \cdot \Delta t \cdot f_s \cdot \bar{I}_o + I_{start-up}$$

- When *Δt=1ns, f=20kHz, I_{avg}=7.5A (I_{rms}=8.3A), $I_{clamper}$≈0.4mA, P_{loss} ≈ 0.4W*

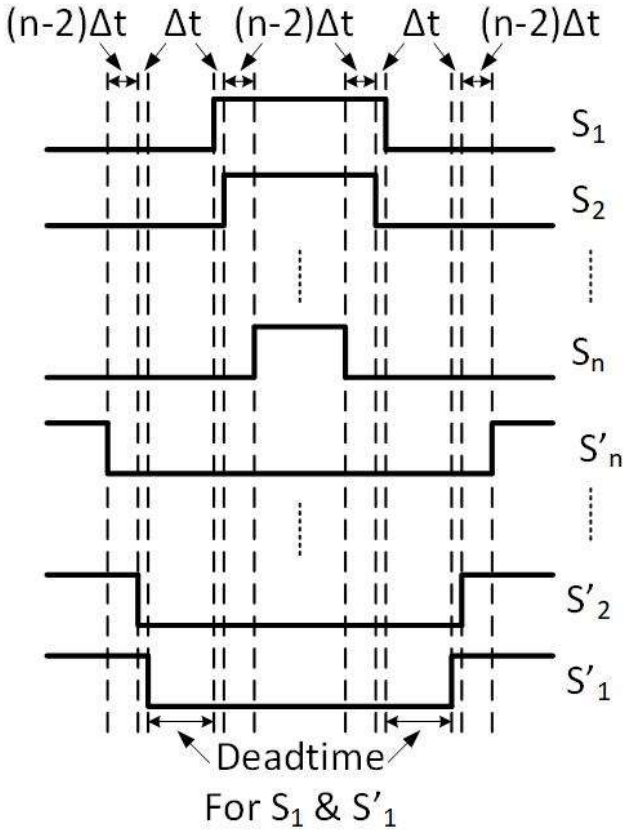


Extension to series-connection of 2n SiC MOSFETs

(n-1) clamping circuits for 2n SiC MOSFET

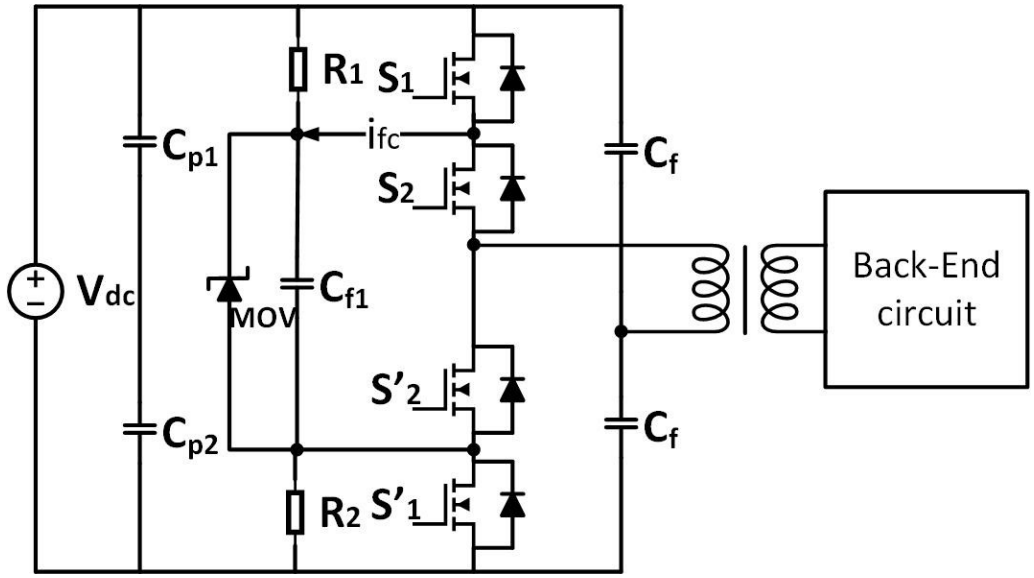


Pre-defined modulation scheme



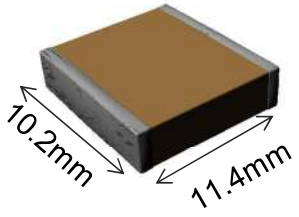
Extension to series-connection of 2n SiC MOSFETs

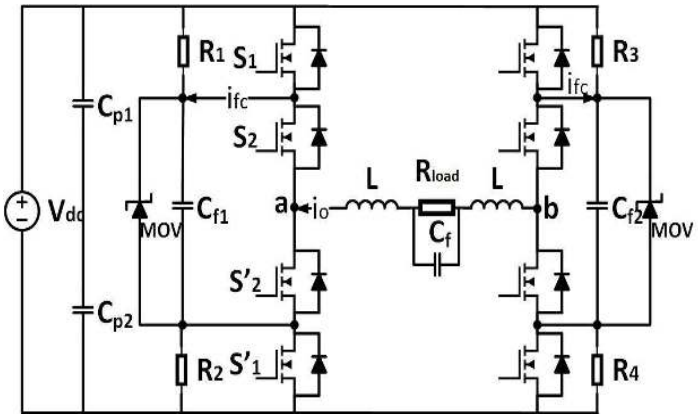
- Extension to DC-DC topologies
  - Isolated resonant dc-dc converters
  - Isolated DAB converters
  - Other multi-level isolated dc-dc converters



Hardware Parameters

Parameters	Value	Parameters	Value
C_{f1}	**68nF**	DCBUS Voltage	2kVDC
Zener Voltage	1060V	Load Voltage	1.2kVAC
Zener Resistance	36kΩ	Load Current	8.7A
R_2&R_3	10MΩ	Deadtime	0.5us
SiC MOSFET	1700V/45mΩ	Δt	1ns
Inductor	6mH	Switching freq	20kHz





Waveforms under rated current and rated DCBUS voltage

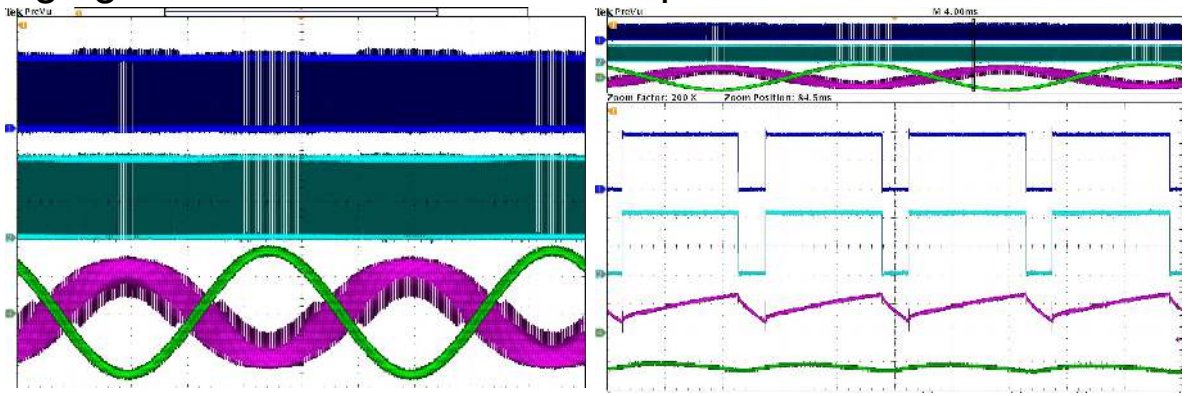
- Validate the effectiveness of proposed hybrid clamping technique under any current, voltage, power factor
- Negligible voltage spike for inner MOSFET due to minimized commutation loop. Voltage ringing for outer MOSFET will be optimized.

CH1: V_{ds1} 500V/div

CH2: V_{ds2} 500V/div

CH3: I_o 10A/div

CH4: V_o 1kV/div

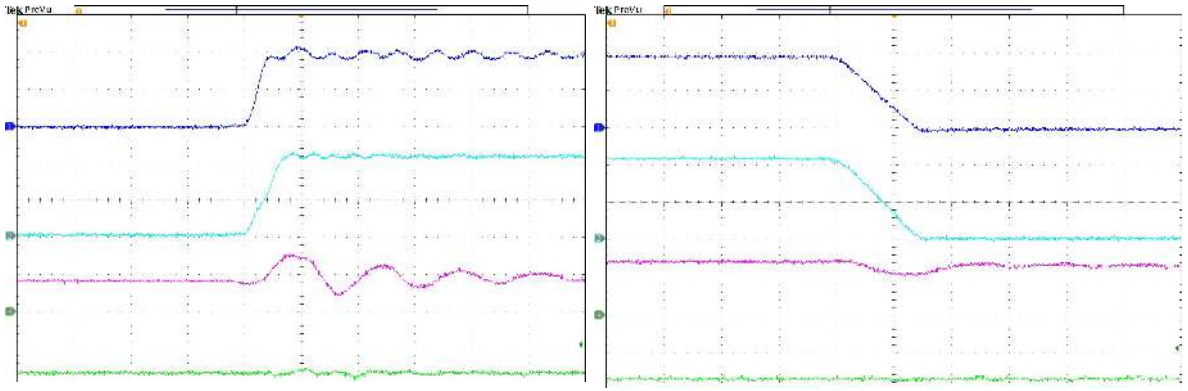


CH1: V_{ds1} 500V/div

CH2: V_{ds2} 500V/div

CH3: I_o 10A/div

CH4: V_o 1kV/div



Low power dissipation on clamping circuit

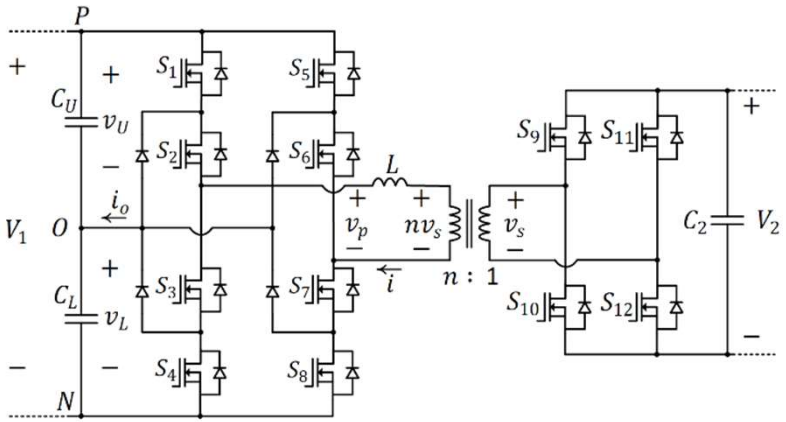
- Power dissipation on zener diodes is around 0.5W
- Power dissipation on start-up resistors is around 0.1W

Temperature of TVS under different leakage current

V_{MOV}/**V**	i_{MOV}/mA	P_{MOV}/W	Temperature/°C
834	0.23	0.123	31
540	0.52	0.281	36
550	1.10	0.605	50

Dual Active Bridge Design

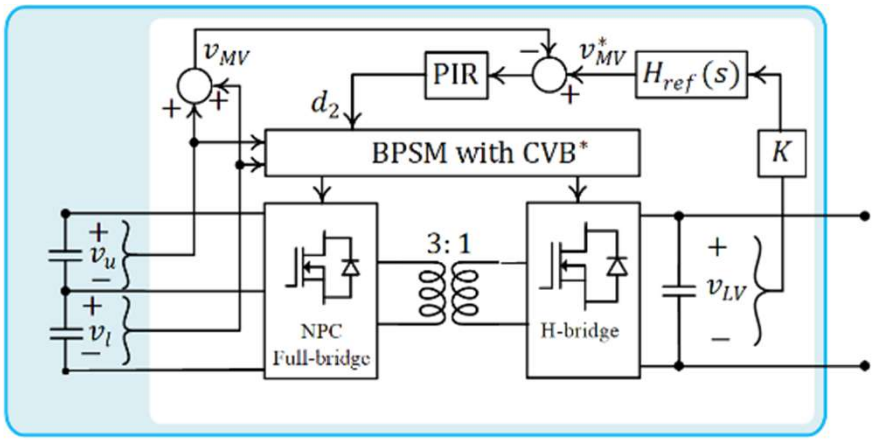
- Dual active bridge topology
- Leakage inductance selected to allow soft switching over entire operating range
- Transformer turn ratio of 3:1
- All-SiC solution with 1700V modules on MV and 1200V modules on LV side
- Switching frequency of 20kHz, with module interleaving on the LV bus



DAB Converter	
Input & Output voltage	2150 V & 750 V
Power level	nominal 83.3 kW
f_{sw}	20 kHz

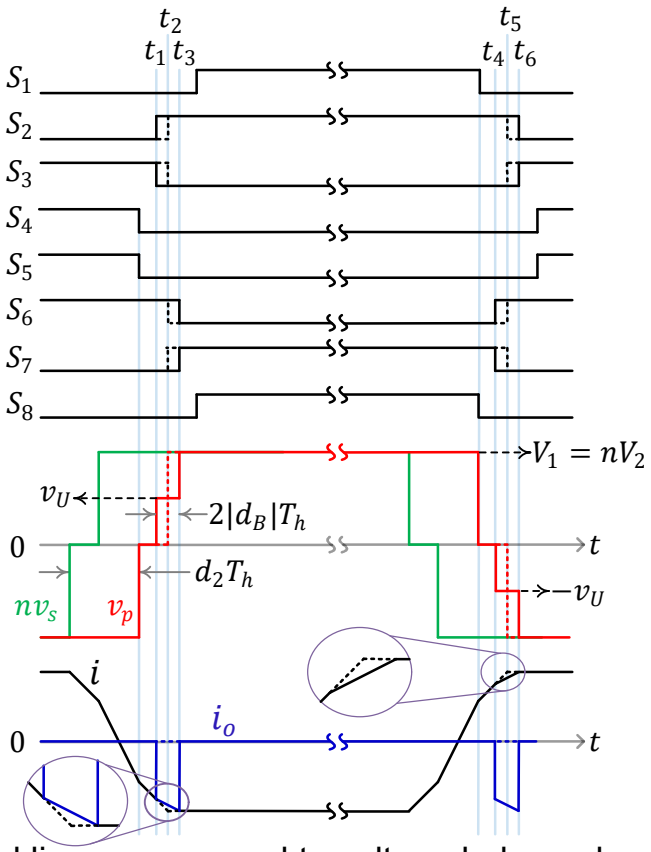
DAB Control and Modulation

- A proportional-integral-resonant (PIR) compensator eliminates 2nd harmonic oscillation on the MV DC bus
- A bidirectional phase-shift modulator (BPSM) with capacitor voltage balancing (CVB) generates the gate pulses for the primary and secondary bridges of the DAB

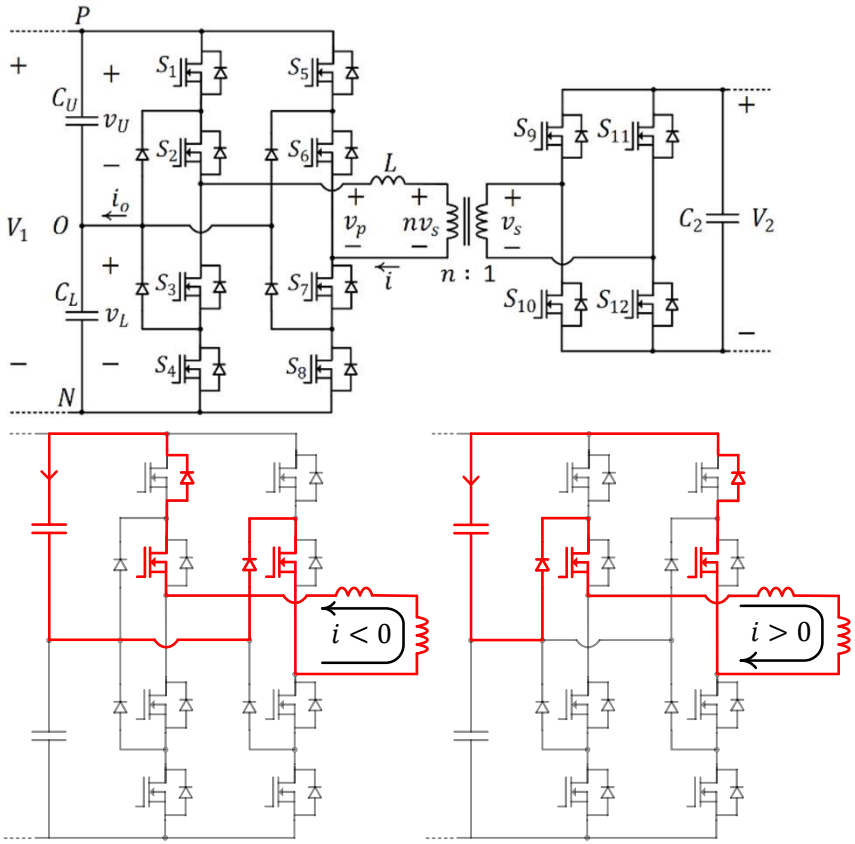


Dual Active Bridge (DAB) with Decentralized control

Capacitor Voltage Balancing



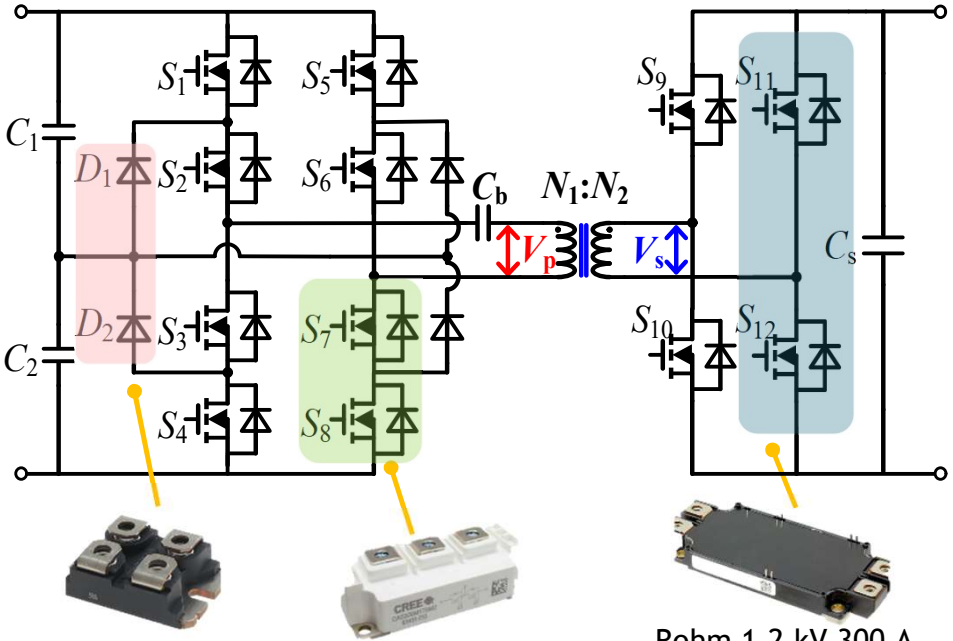
Dashed lines correspond to voltage balanced operation ($v_U = v_L$) and solid lines show correspond to $v_U < v_L$



Charging the upper capacitor irrespective of direction of transformer current

Power Stage Design

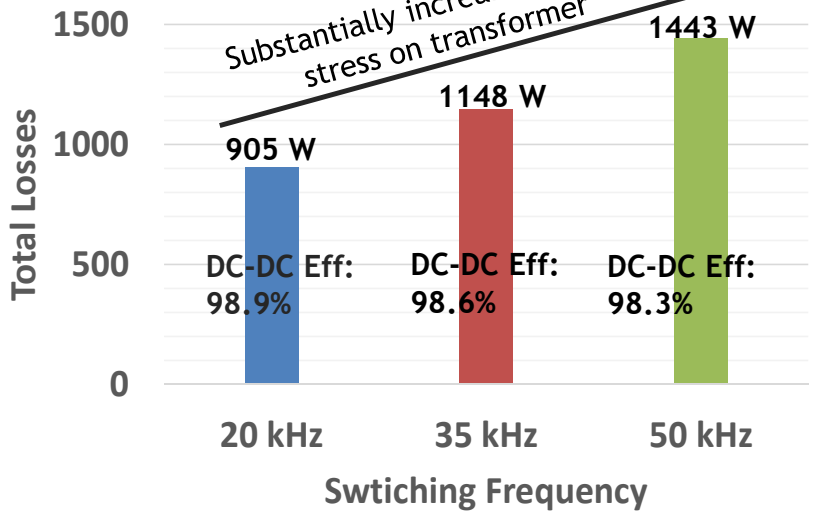
- Target efficiency is 98.9% at the cost of lower power density and underutilized switching capability of SiC devices; 20 kHz is selected based on loss analysis



IXYS 1.8 kV 25 A
Si diode module

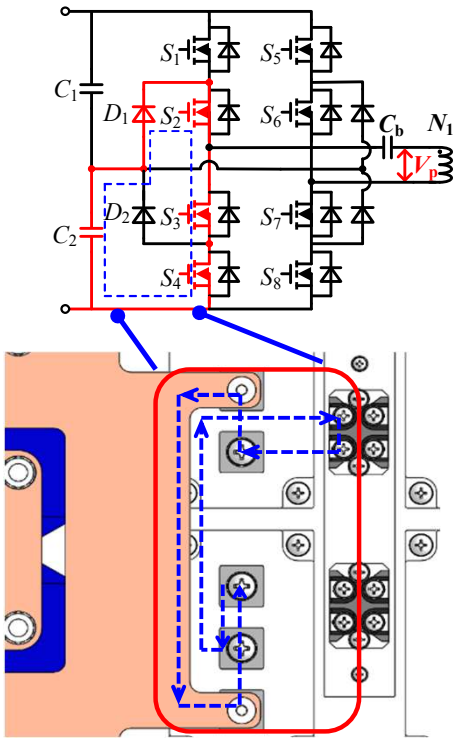
Cree 1.7 kV 325 A
SiC MOSFET

Rohm 1.2 kV 300 A
SiC MOSFET

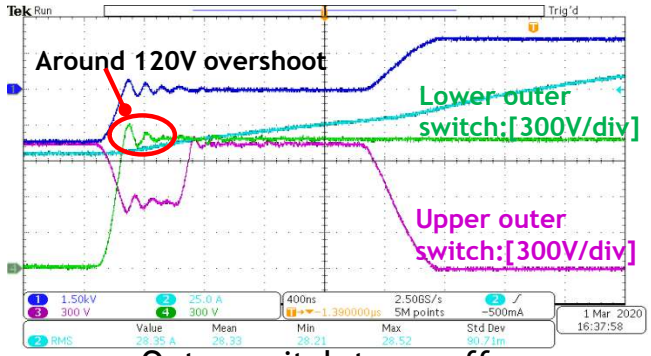


Commutation Loop Optimization

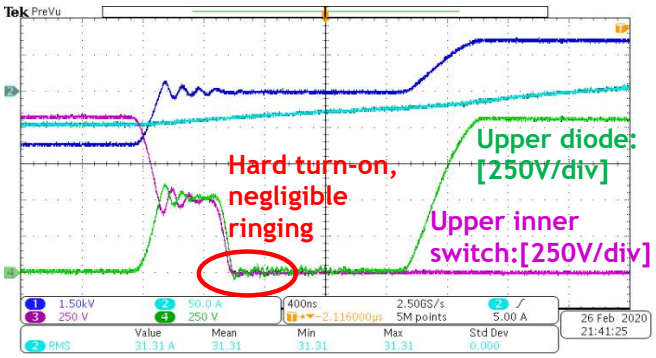
- Innovative multi-layer implementation minimizes the parasitic inductance in this loop, minimizing voltage overshoot and therefore device stress



Commutation loop in physical setup



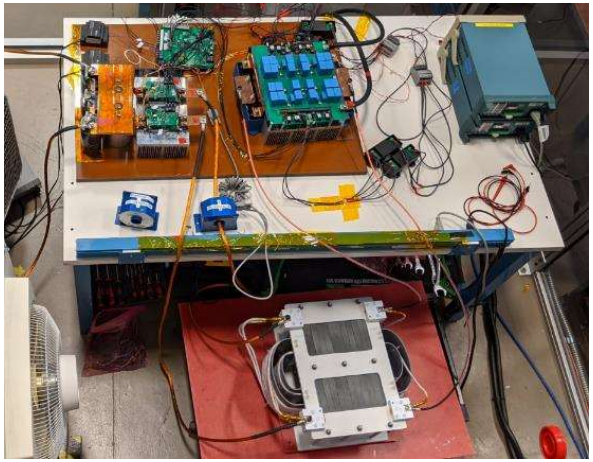
Outer switch turns off

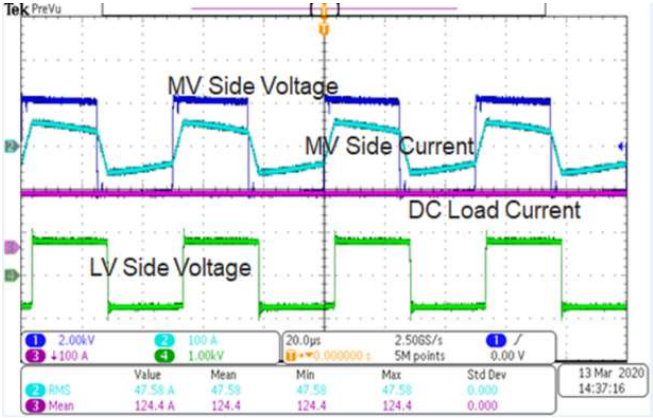


Inner switch turns on

DAB Stage Testing

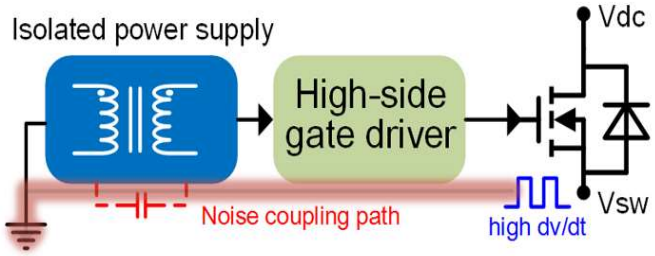
- Successfully tested DAB stage at 95 kW (115% of rated load)
- Efficiency is measured at 98.9%
- Hotspot below 70ºC in steady-state (less than 50ºC temperature rise)
- Low voltage overshoot on device drain-to-source voltage



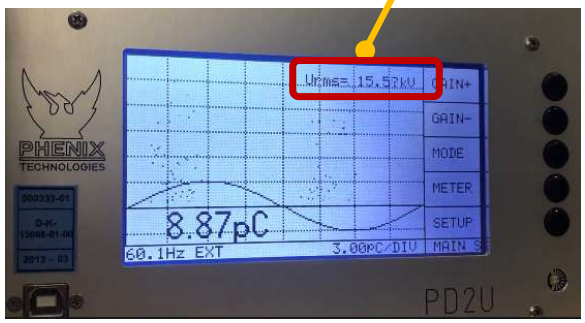


High Isolation Power Supply

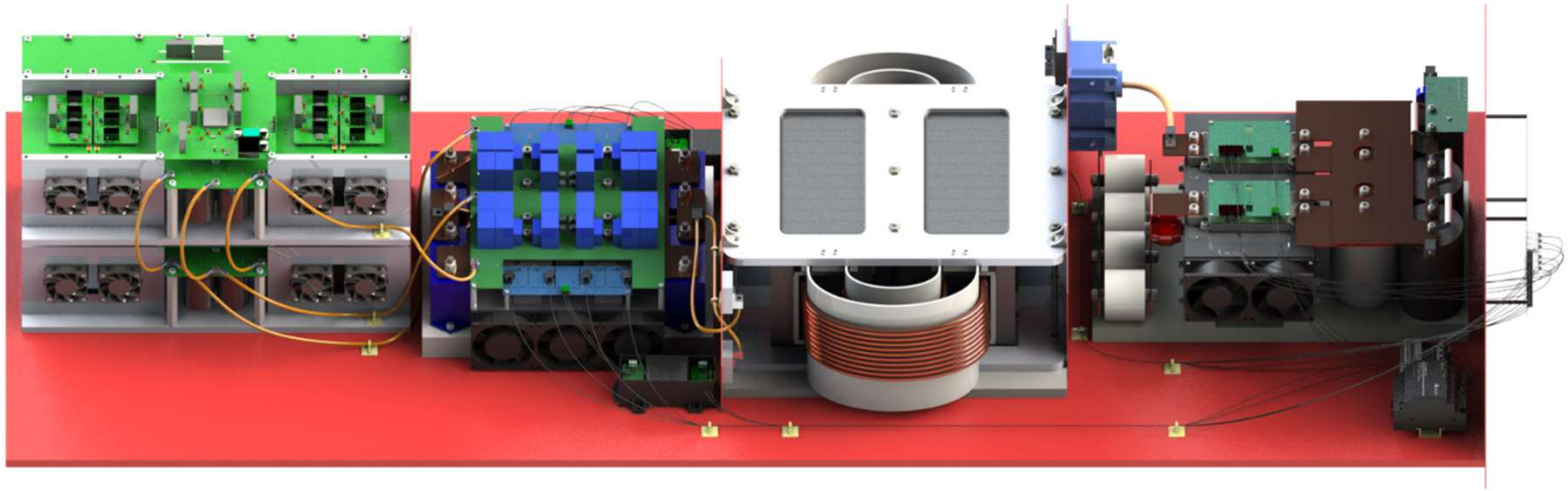
- High isolation voltage is achieved through loosely coupled transformer.
- The partial discharge inception voltage reaches 15 kV (target 40kV). Extinction voltage above 10 kV.
- Small parasitic capacitance (1.2pF) provides superior common mode noise rejection.
- Developing potting procedure that allows for reliable and repeatable results.

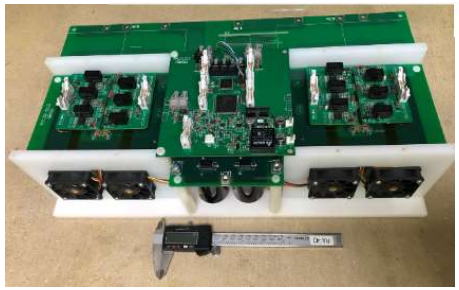


Charge goes beyond 15.6 kV at 10 pC

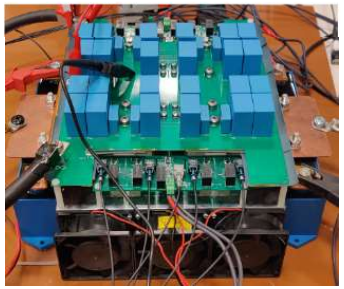


SST Module Prototype

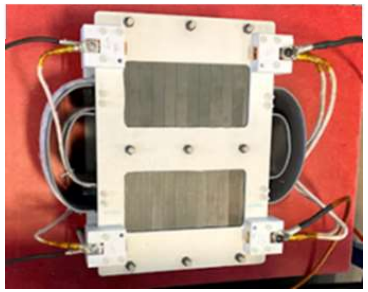




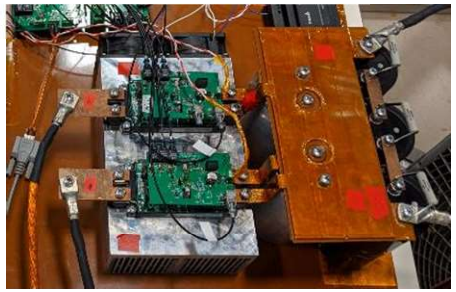
Active front-end



DAB MV side



Transformer



DAB LV side

References

Source: M.A. Awal, Md. Bipu, O. Montes, H. Feng, I. Husain, W. Yu and S. M. Lukic, Capacitor Voltage Balancing for Neutral Point Clamped Dual Active Bridge Converters, *IEEE Transactions on Power Electronics*, doi: 10.1109/TPEL.2020.2988272.

D. Wang and W. Yu, "Series Connection of SiC MOSFETs with Hybrid Active and Passive Clamping for Solid State Transformer Applications," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 12-19, doi: 10.1109/WiPDA46397.2019.8998791.

Thanks!