



Next Generation SiC EV Inverter with Ultra-High Efficiency and Voltage Slope Control

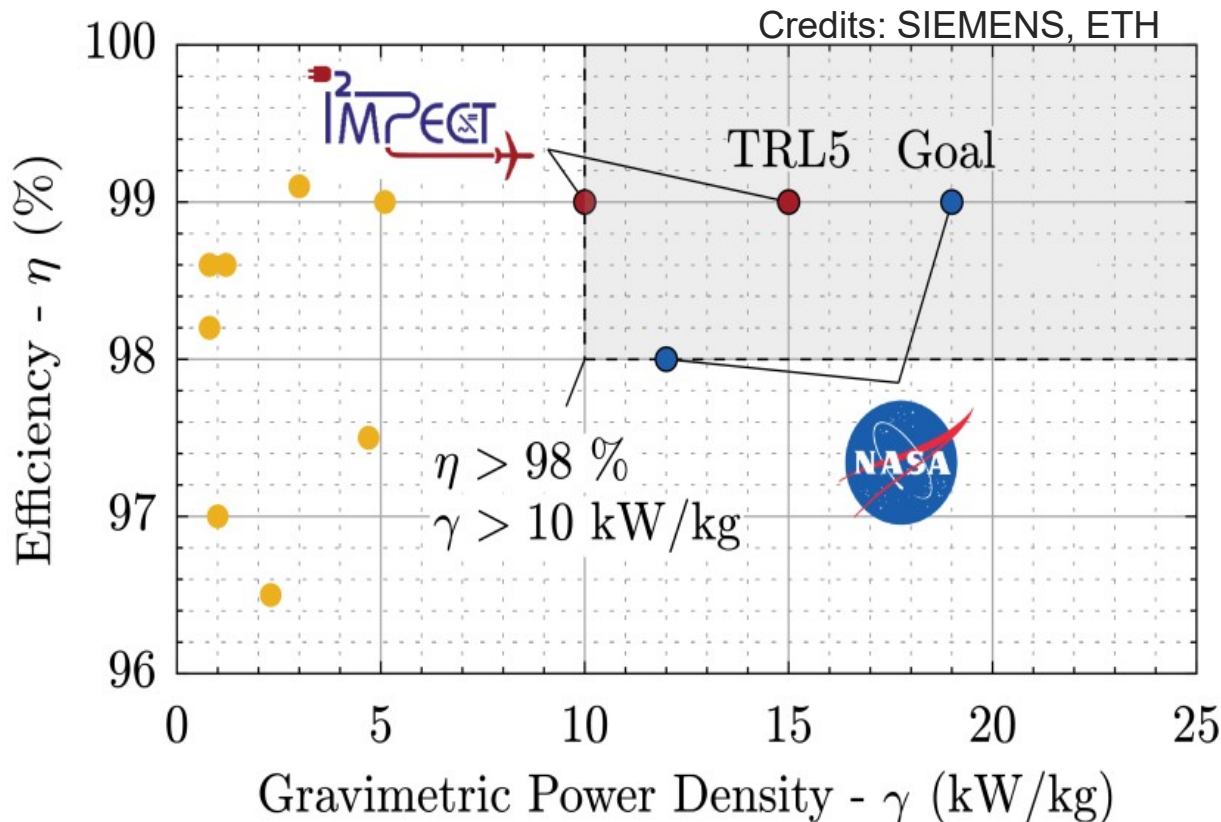
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2-20-2023

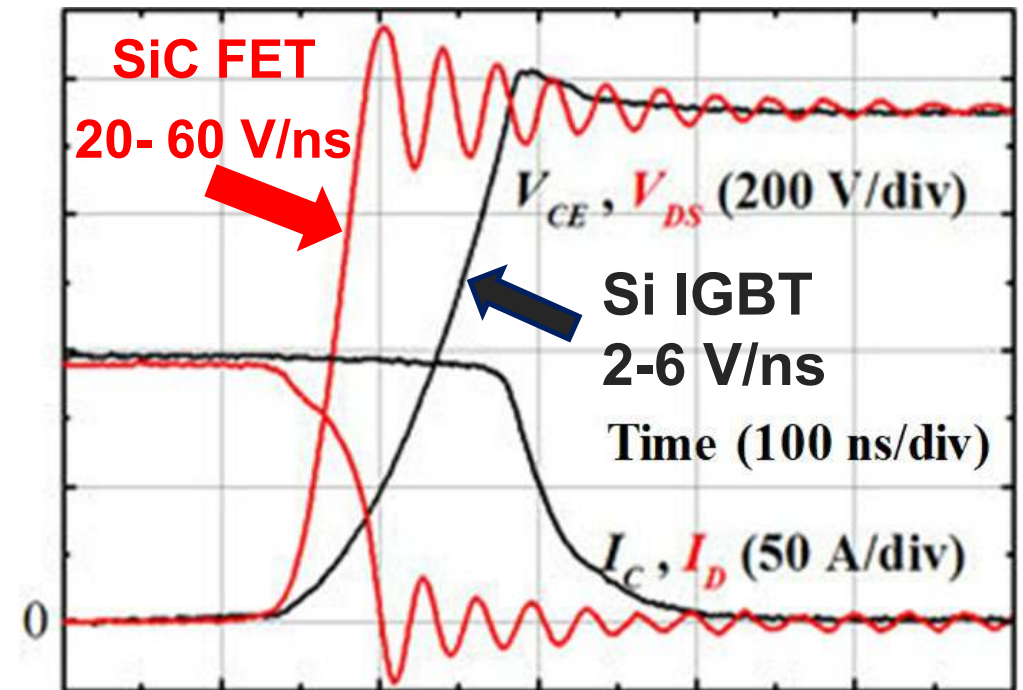
❑ Much better efficiency and power density

- SiC-MOSFET reduces switching loss and conduction loss at partial load compared to Si-IGBT
- SiC-MOSFET enables high efficiency, high power density and high frequency operation



❑ Extremely high dv/dt challenge

- Si-IGBT: $dv/dt = 2-6$ kV/ μ s
- SiC MOSFET: $dv/dt = 20-60$ kV/ μ s
- Issues: motor insulation stress, bearing current, EMI



Objectives:

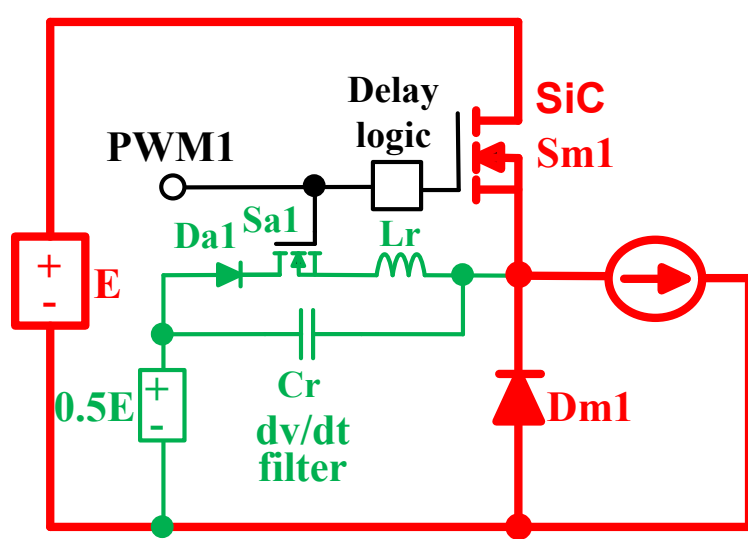
- Develop and demonstrate a technical readiness level (TRL) 5, three-phase, fully functional SiC inverter hardware and firmware with 100 kW output power for Motor drives, the goals are
 - **99.2% or higher peak efficiency, and**
 - **Better (less) than 6 kV/ μ s voltage slope**

Expected Outcomes and Impacts:

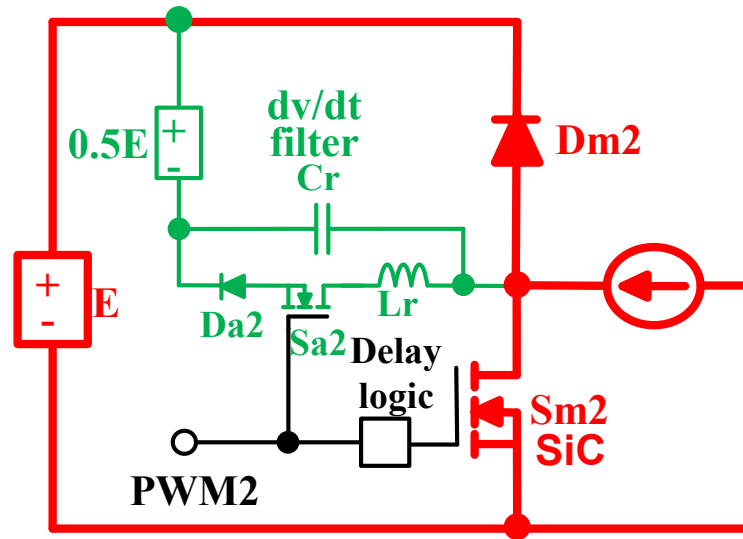
- 50% total power loss savings compared with hard-switching SiC motor drives
- Ensured dv/dt compatibility with NEMA standards
- Minimized stress on motor insulation with longevity of the electric motor
- Improved EMC, better noise immunity of sensors, gate drivers and controllers
- Simplified thermal management, easier integration of inverter and motor
- Reduced motor loss with the increased frequency of the inverter

Name	Organization	Roles
Wensong Yu	NC State University	Lead PI, Research, develop and deploy the SiC inverter with soft-switching filter system
Iqbal Husain	NC State University	Co-PI, Providing the electric machine related inputs
Douglas Hopkins	NC State University	Co-PI, packaging of electronic drive development
Dakai Wang	NC State University	PhD Research Assistant, Hardware/software development and test
Pranit Pawar	NC State University	PhD Research Assistant, Hardware/software development and test
Kevin Speer	Microchip Technology	Senior Manager, Commercialization management
Xuning Zhang	Microchip Technology	Senior Tech. Engineer, SiC PM and AE
Steven Chenetz	Microchip Technology	Senior Tech. Engineer, AE support
Dennis Meyer	Microchip Technology	Principal Engineer, AE support
Mingyu Li	Microchip Technology	Principal Engineer, SiC device support
Yifan Jiang	Microchip Technology	Senior Engineer, SiC device support

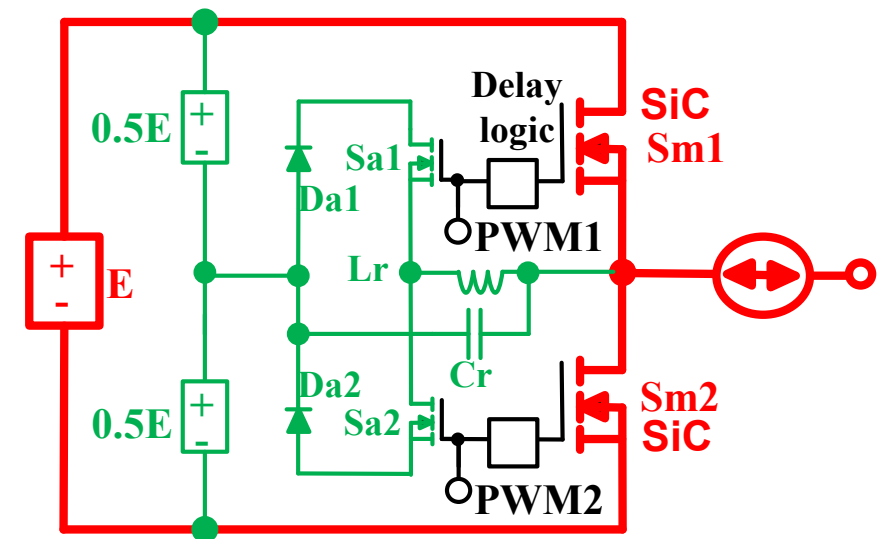
- Active small dv/dt filter (shown **in green**) operates in a very short time ($< 1\mu s$). Its average current is significantly lower than ($< 5\%$) the current stress of the main circuit (shown **in red**).
- All main switches (shown **in red**) operate at nearly perfect zero-voltage-switching under any input or output voltage and output current conditions with significantly reduced switching loss
- Using the simplest gating signals (shown **in black**), as simple as signals in classic inverters



Buck with soft-switching dv/dt filter



Boost with soft-switching dv/dt filter



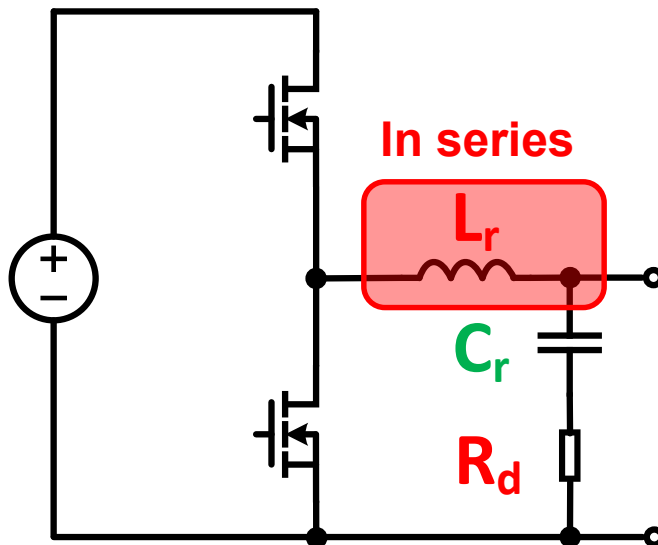
Inverter with soft-switching dv/dt filter

- For classic dv/dt filter, the bulky inductor is connected in series with load. Lossy damping resistor R_d is needed
- For state-of-art dv/dt filter, lossy damping resistor R_d is deleted with penalty of the triple gating
- For proposed dv/dt filter, the inductor is connected in parallel with load. **Inductor current remains zero for >90% time.** The filter volume is reduced around 10 times compared to the series-inductor solutions.

Classic dv/dt filter

X Bulky inductor L_r

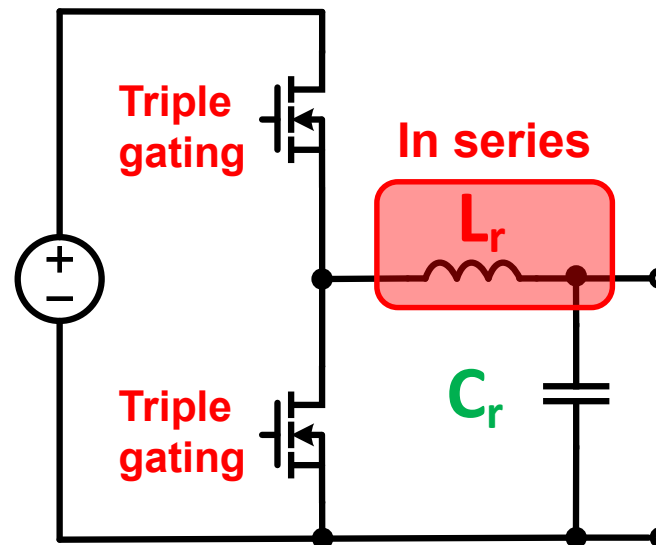
X Lossy damping R_d



State-of-art dv/dt filter

X Bulky L_r

✓ No R_d

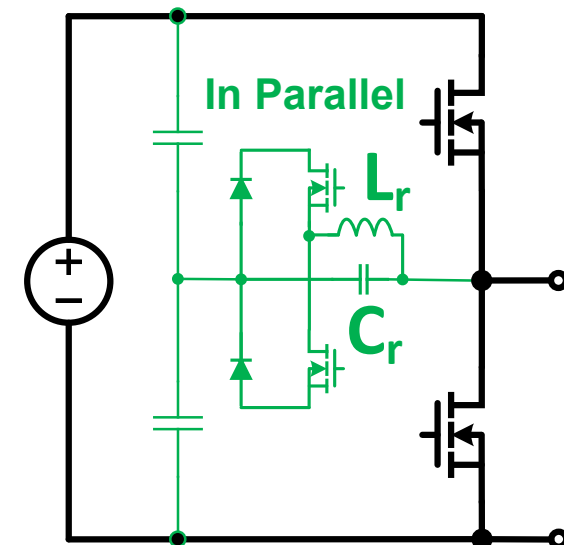


Proposed dv/dt filter

✓ Small L_r

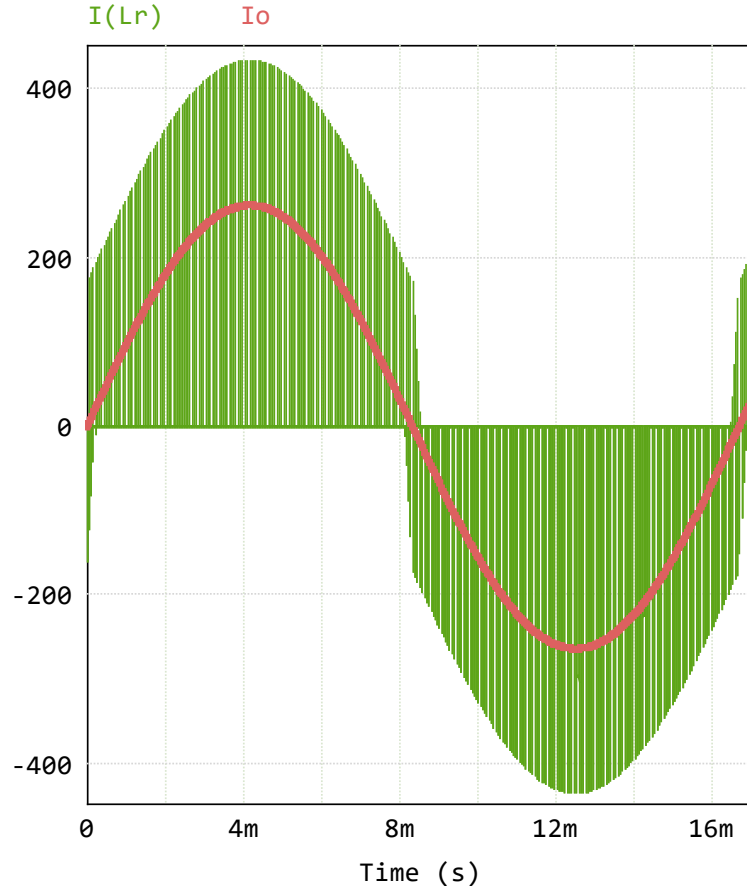
10X reduced
filter volume!

✓ No R_d

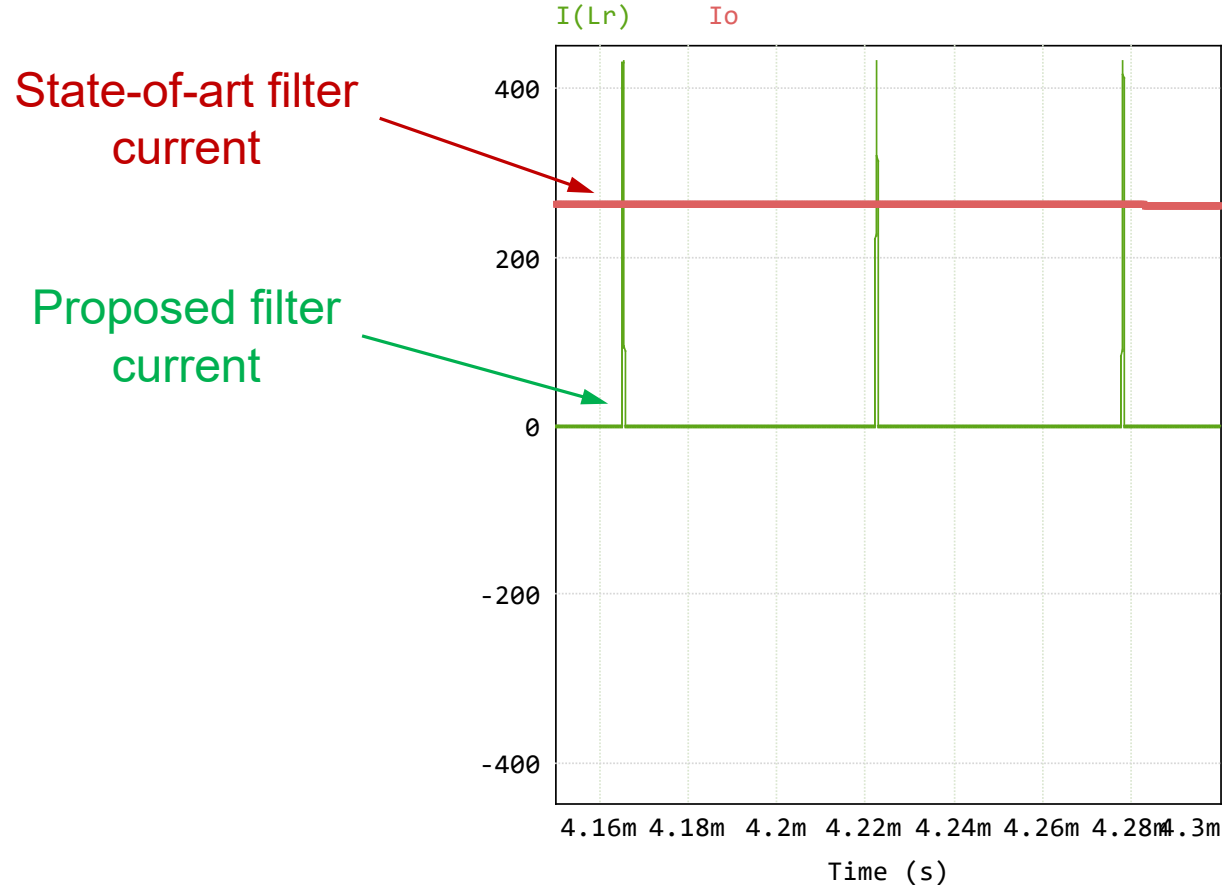


- Because of the proposed dv/dt filter with parallel configuration, conduction duration of the inductor reduces more than 50 times compare to the state-of-art dv/dt filter solutions with series configurations.
- RMS current of the inductor is 26A in the proposed filter at 150 kW power and 18kHz switching frequency, which is a 7 times reduction compared to the 186A RMS current in the classic and state-of-art solutions .

@ Motor fundamental cycle (60Hz)

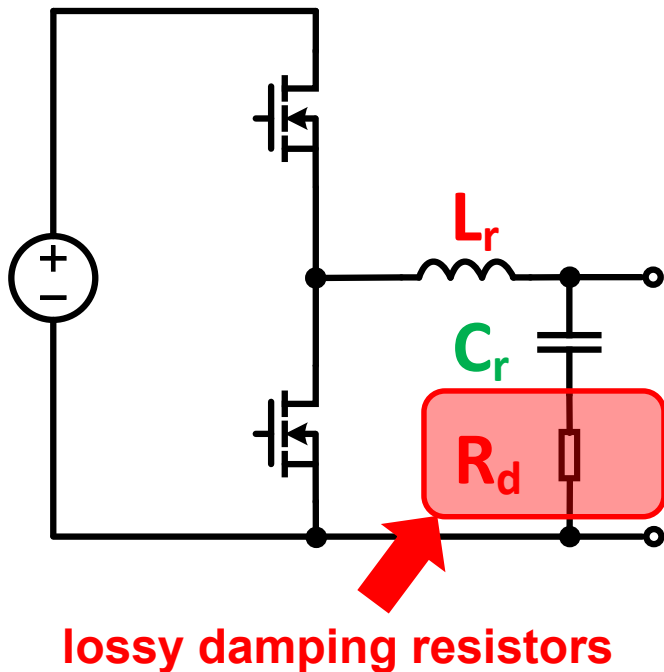


@ SiC FET switching cycle (18 kHz)

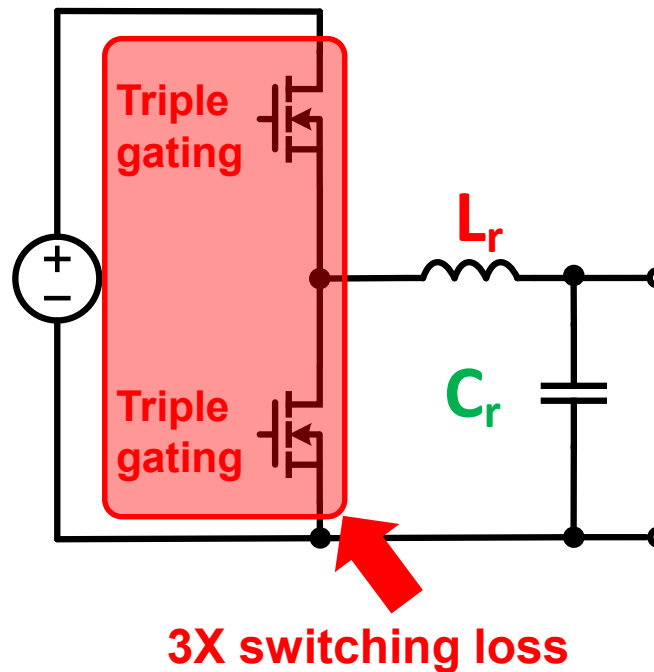


- Classic dv/dt filter requires bulky and lossy damping resistors to dissipate the extra oscillation energy.
- State-of-art dv/dt filter eliminates the damping resistor but triples the switching loss.
- The proposed dv/dt filter can not only recover the energy in the filter but also significantly reduce the switching loss of the main switch in the high-power inverter.

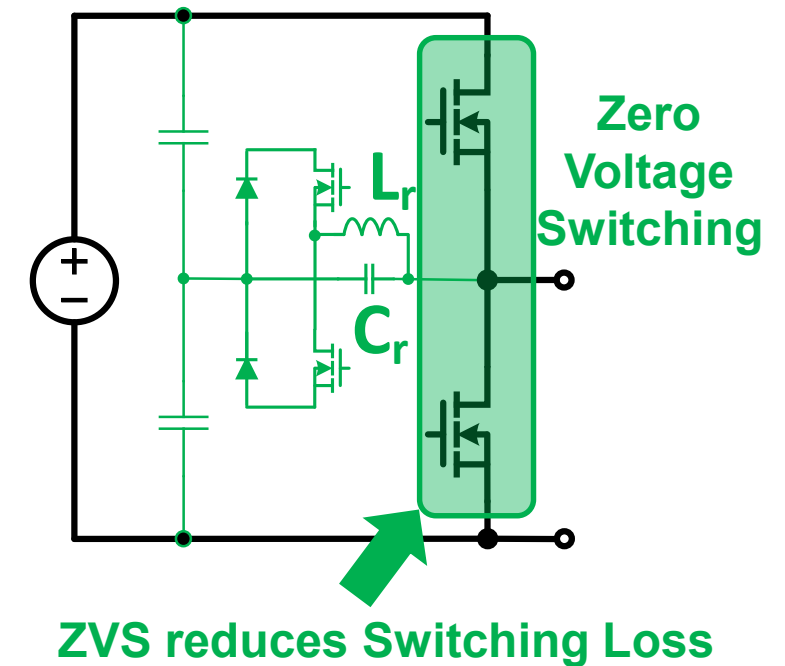
Classic dv/dt filter



State-of-art dv/dt filter



Proposed dv/dt filter

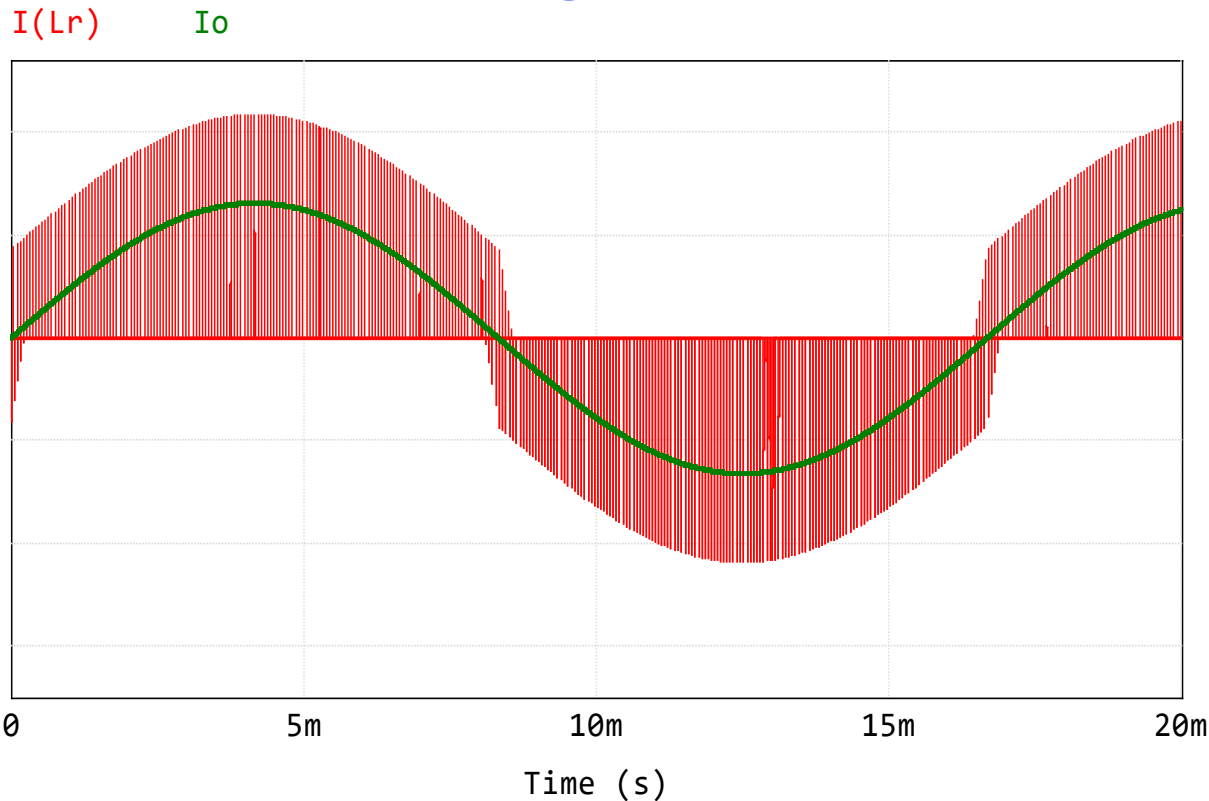


- 100 kW SiC inverter with series inductor and damping resistor dv/dt filter dissipates the extra 346.7 W power loss. The total loss of this inverter is estimated at 1260 W.
- 100 kW SiC inverter with state-of-art dv/dt filter no need of damping resistor triples the switching loss. At 18kHz, the total loss of the inverter is estimated at 1844 W.
- Total power loss of inverter with the proposed soft-switching dv/dt filter is estimated at 590 W with >50% savings.

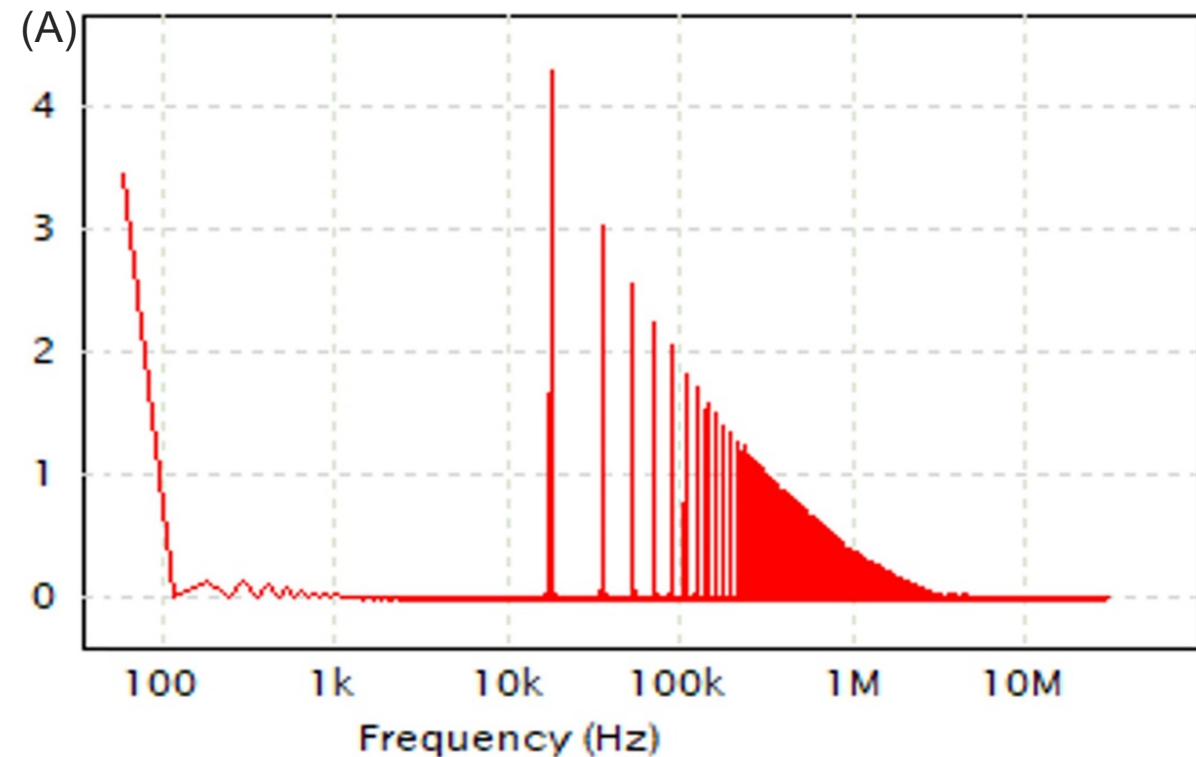
Inverter with dv/dt Filter	Main switch switching loss (W)	Main switch conduction loss (W)	Resistor Loss (W)	Inductor Loss (W)	Auxiliary switch conduction loss (W)	Auxiliary switch switching loss (W)	Total Loss (W)
The classic	417	469.4	347	26	0	0	1260
The state-of-art	1265	545	0	34	0	0	1844
The proposed	53	430	0	19	81	7	590

- The filter inductor current spectrum has low-frequency (10s-100s Hz) and high-frequency (10s-1000s kHz) components
- The highest frequency of interest: 2MHz
- Litz wire with 48 AWG is used in filter inductor

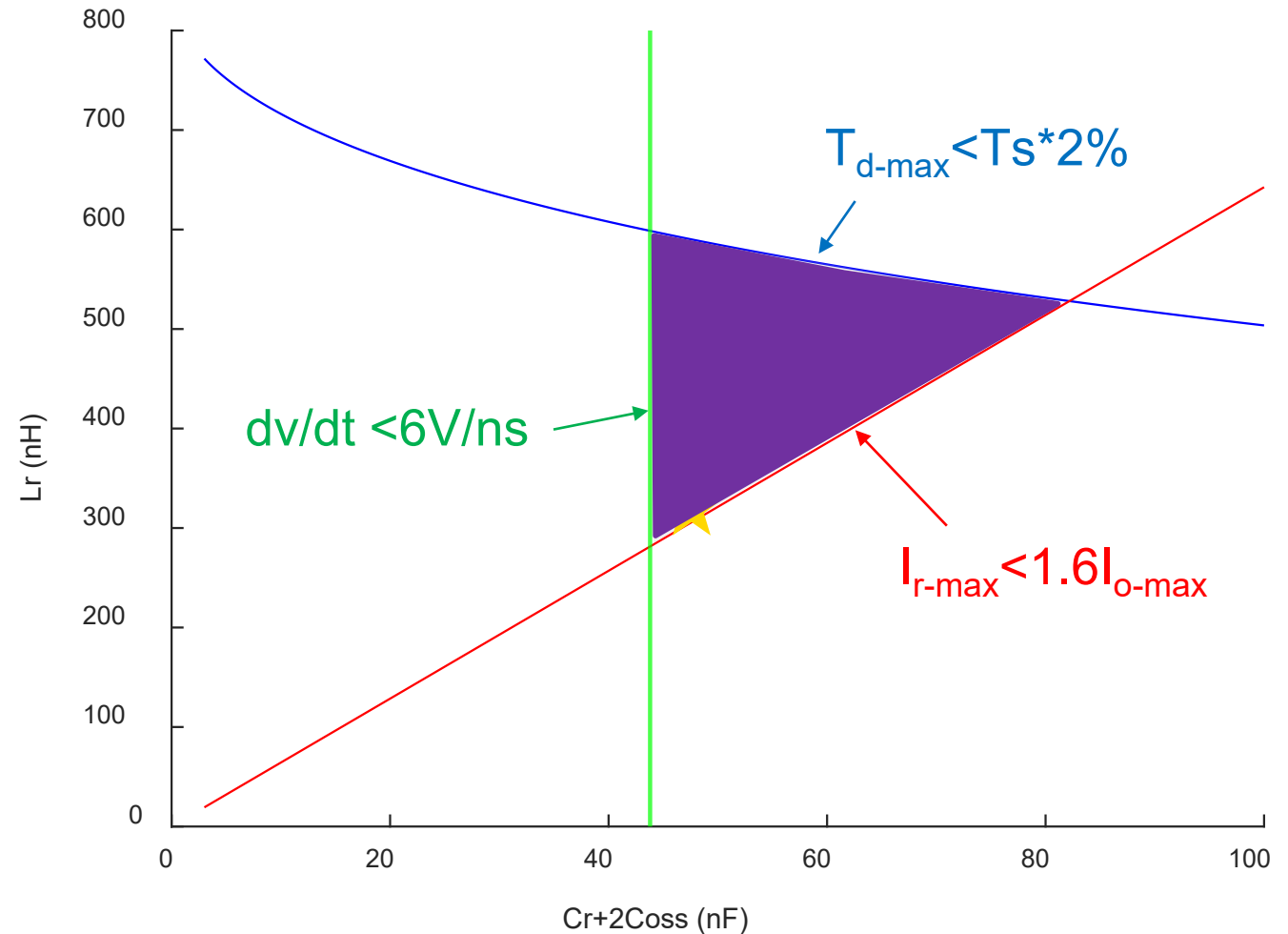
Inductor current @ time domain



Inductor current @ frequency domain

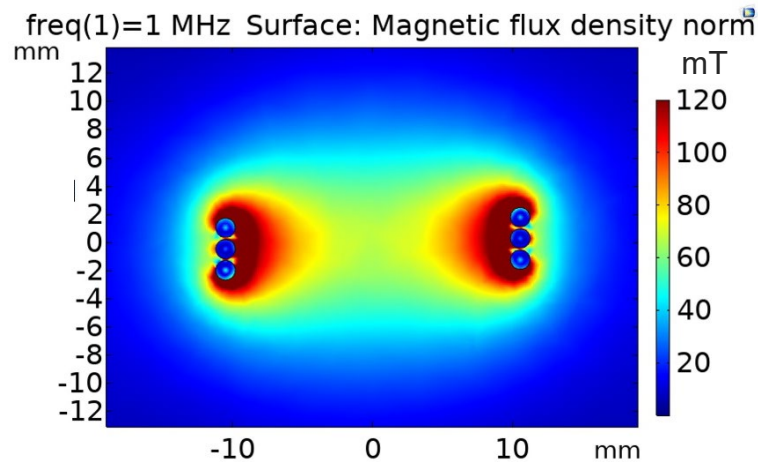
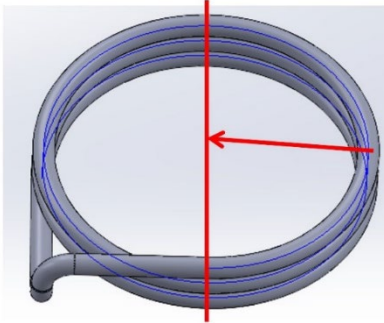


- Resonant capacitance value is determined by dv/dt limitation at peak load current (shown in green line).
- Resonant inductance value is constrained by deadtime limitation (shown in blue line) and peak current limitation for the auxiliary circuit (shown in red line).
- The **feasible area** of the dv/dt filter parameter design is shown in purple.
- The finalized C_r value is **7x6.8 nF** (47.6 nF) and finalized L_r value is **320 nH** to minimize the size of dv/dt filter.

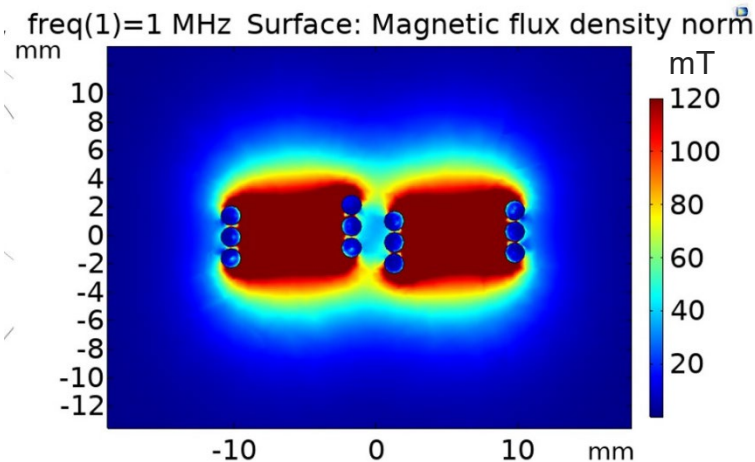
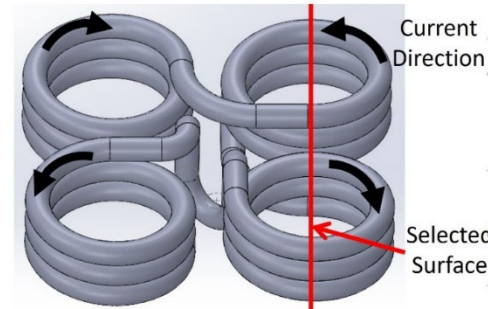


- A matrix coreless inductor is proposed and simulated with near field leakage flux cancellation

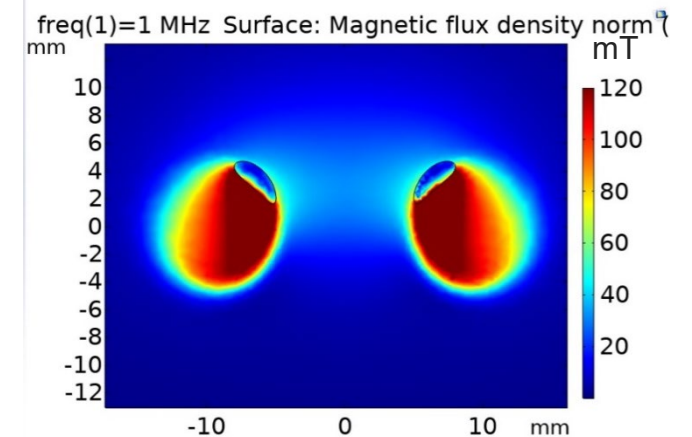
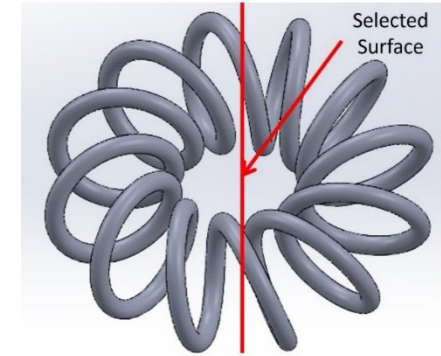
- Existing solenoid coreless inductors



- Proposed matrix coreless inductors

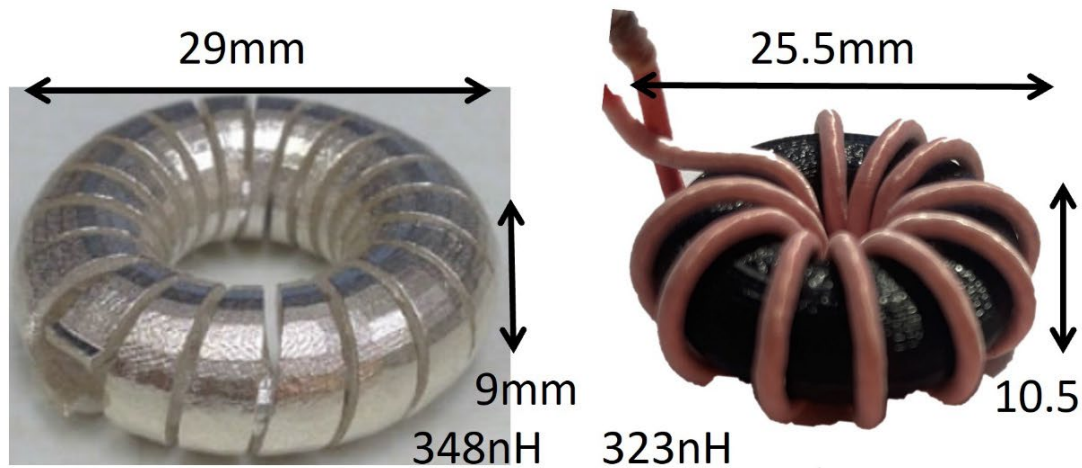


- Existing toroid coreless inductors



- ❑ A matrix coreless inductor is fabricated and verified with **2 times of energy density** compared to the state-of-art toroid coreless inductors.
- ❑ The **tested quality factor (Q)** of the matrix coreless inductor is up to **124 at 1MHz** frequency.

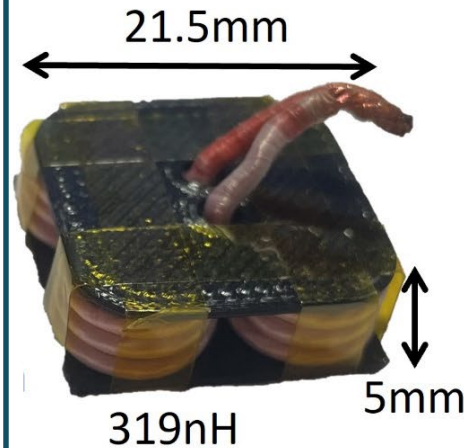
- State-of-art toroid coreless inductors



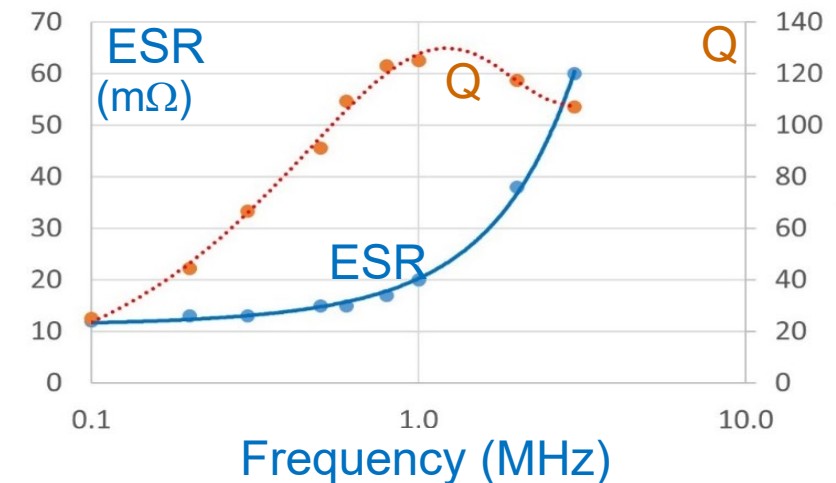
(a) with foil winding

(b) with Litz wire winding

- Proposed matrix coreless inductors



(c) Matrix Litz winding

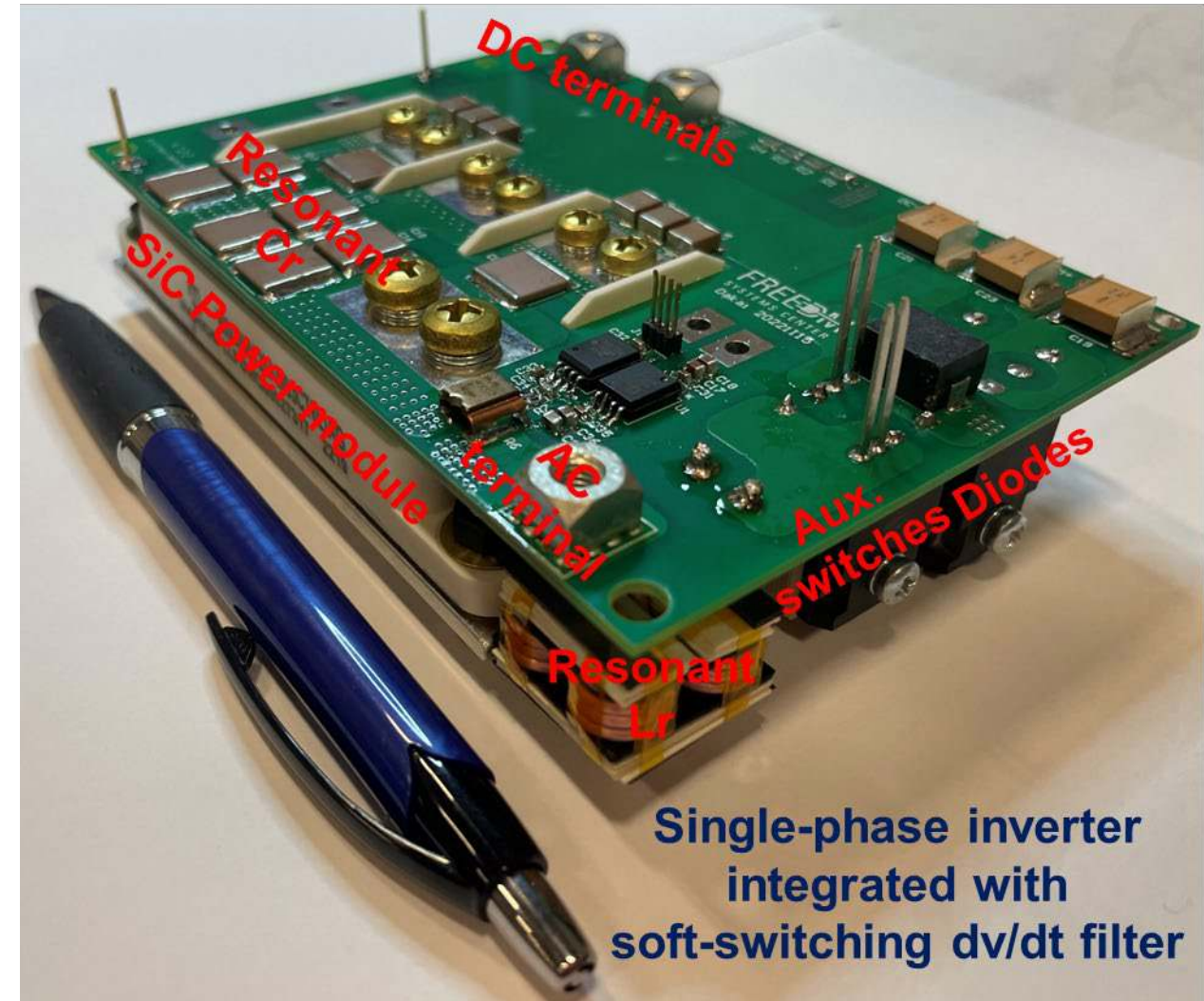
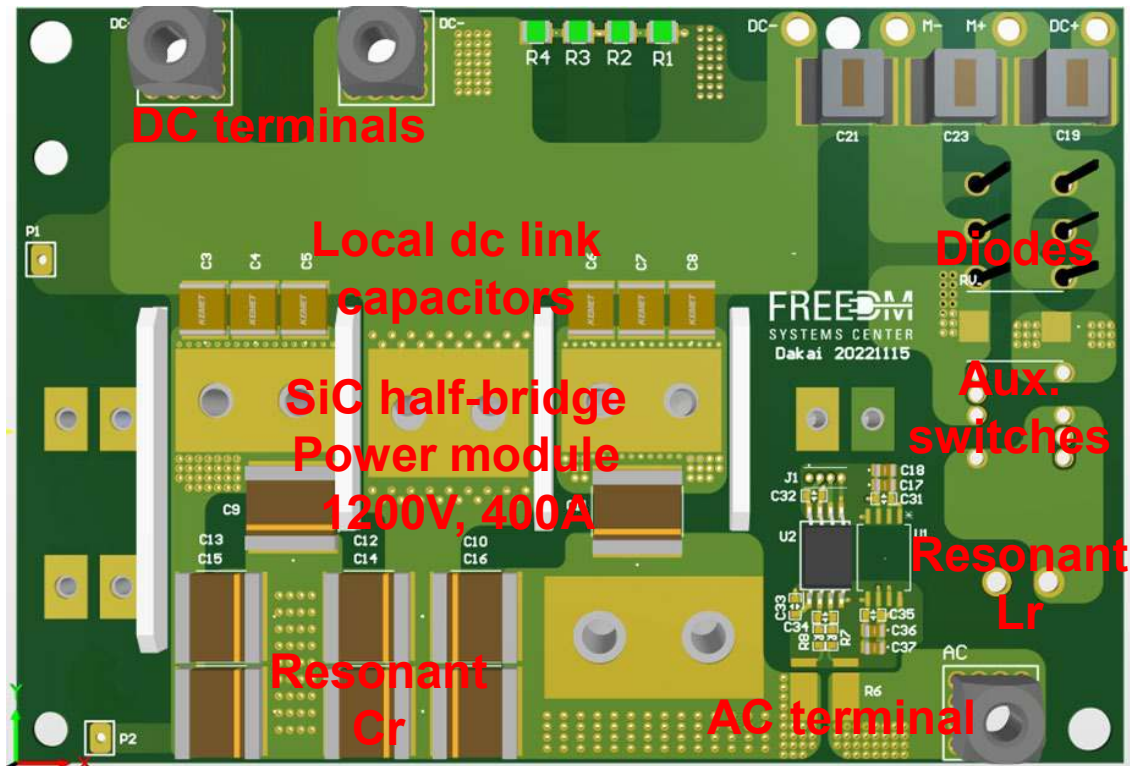


(d) ESR and Q measurement

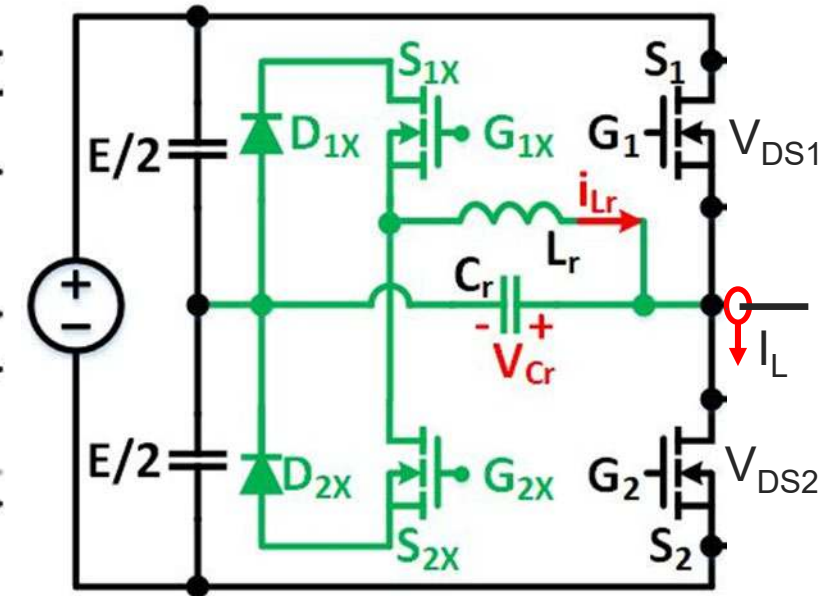
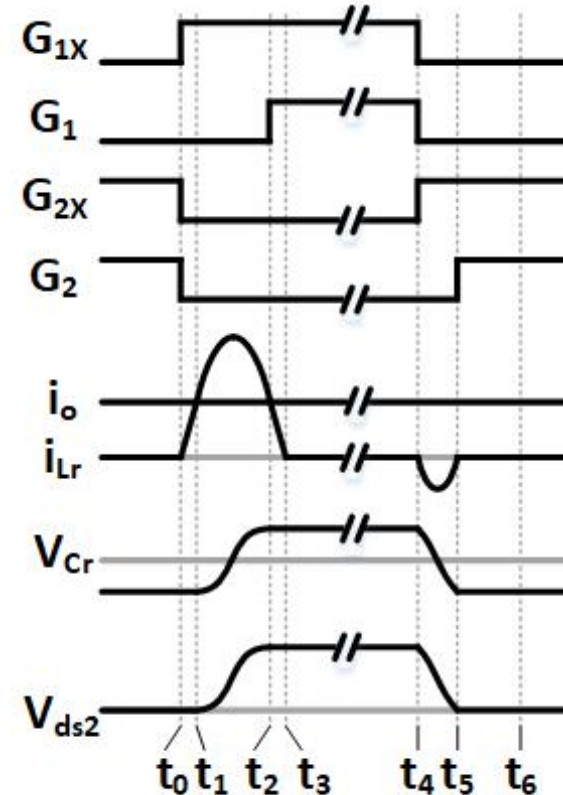
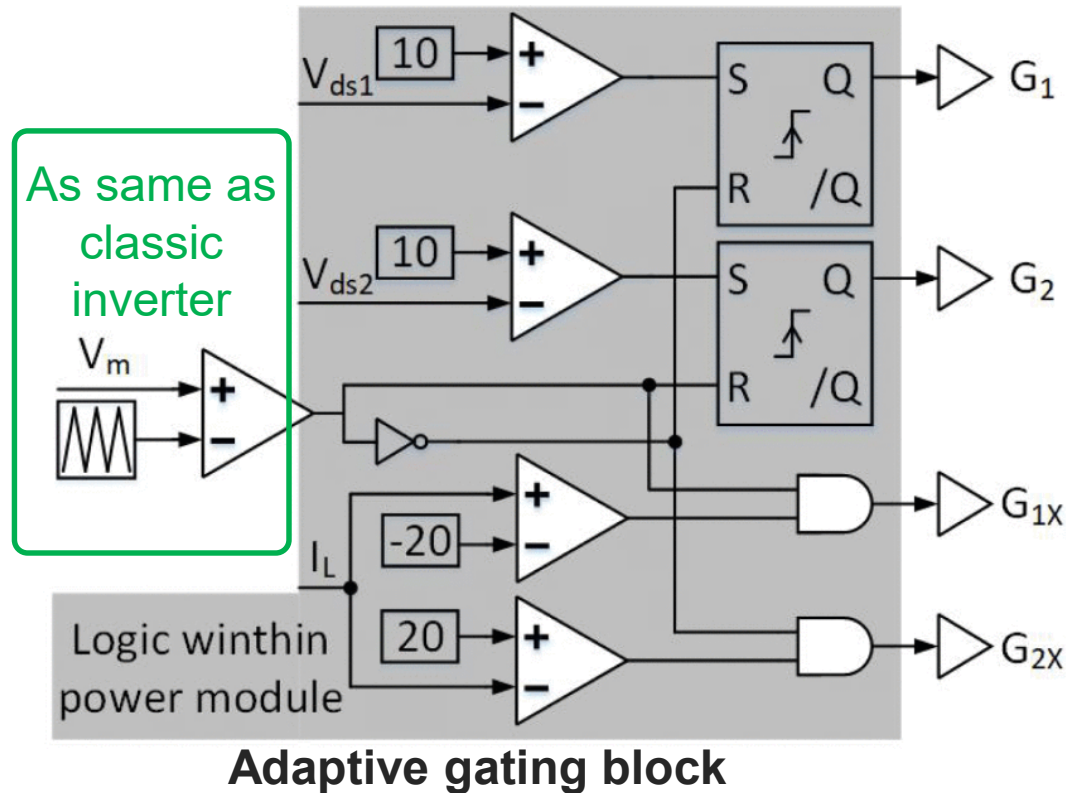
Prototype of SiC Inverter Integrated with Proposed dv/dt Filter

- Single-phase SiC inverter parameters

L_r : 0.32 μ H, C_r : 47.6 nF
 S_a : 2X TO247-4, 1.2 kV/16 m Ω
 D_a : 2X TO247, 0.75 V/50 A
 S_m : Half-bridge, SiC 1.2 kV/4.3 m Ω

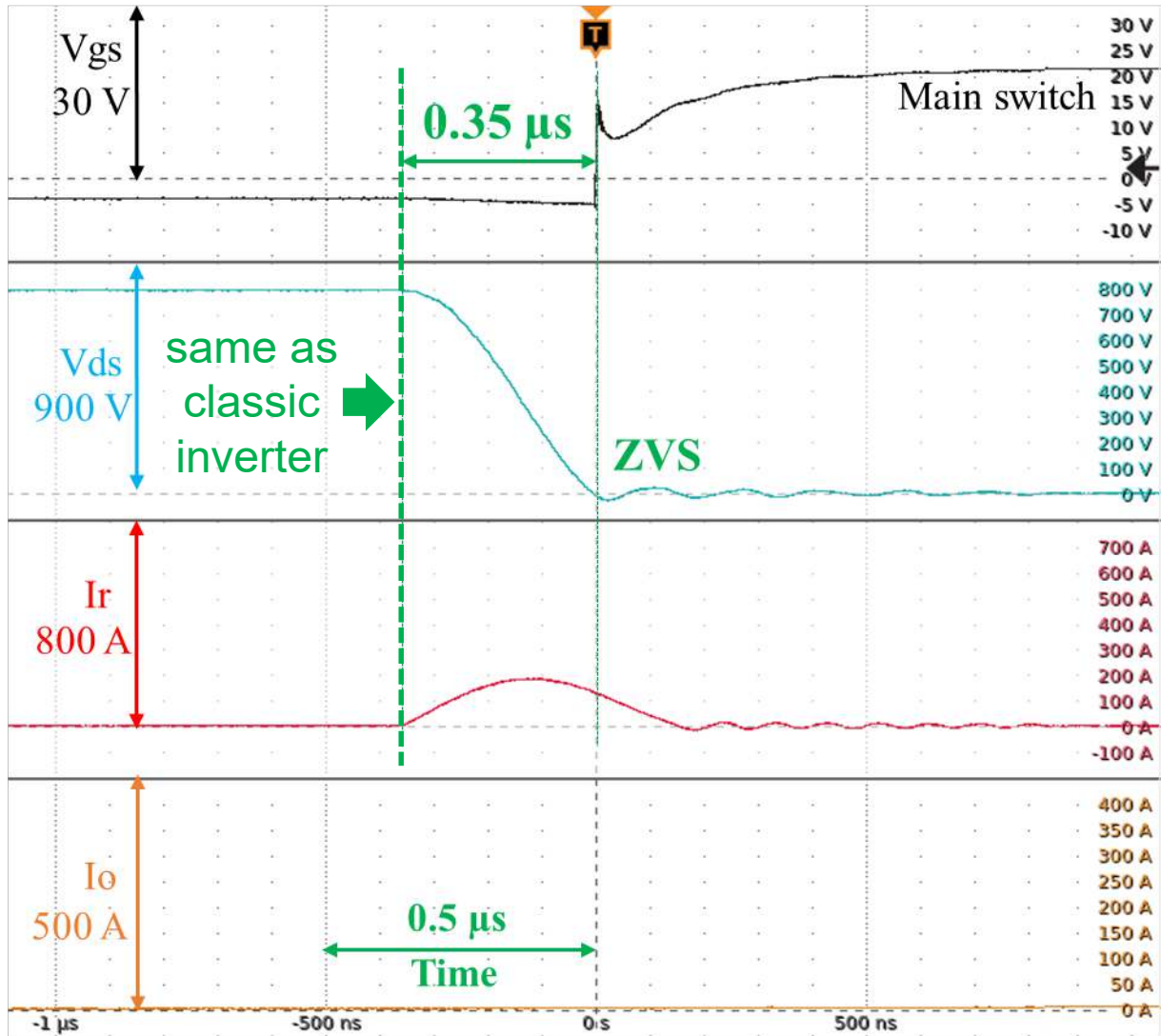


- The control signals are simplified as same as classic inverter by using the proposed adaptive gating block shown in the gray

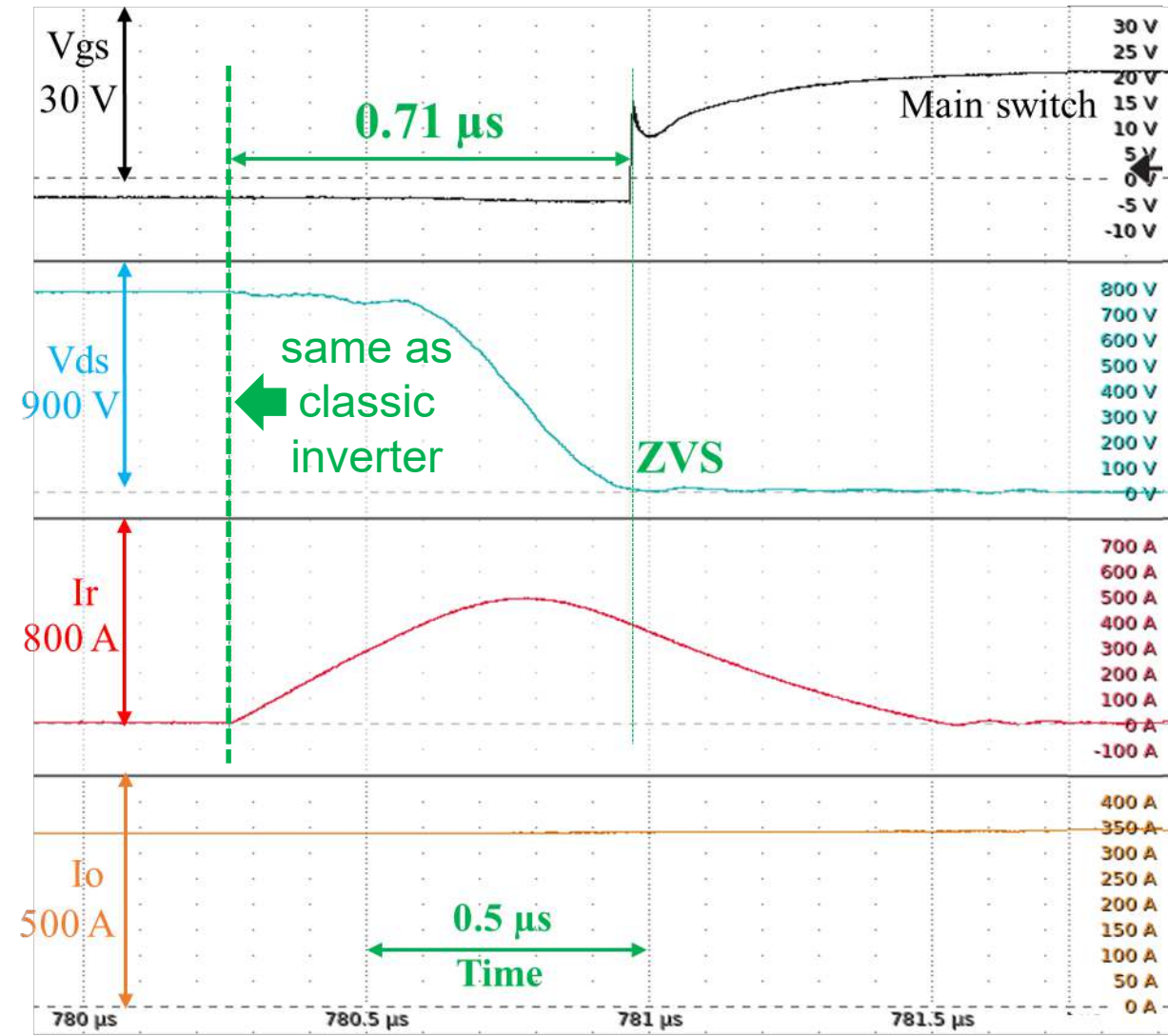


Reference: D. Wang and W. Yu, "Soft-Switching dv/dt Filter with Ultra High Power Density and 50% Power Loss Savings for 150 kW SiC Motor Drives," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), 2022, pp. 1-8

□ Adaptive time = $0.35\ \mu\text{s}$ at $I_o = 0\ \text{A}$, $V_{dc} = 800\ \text{V}$

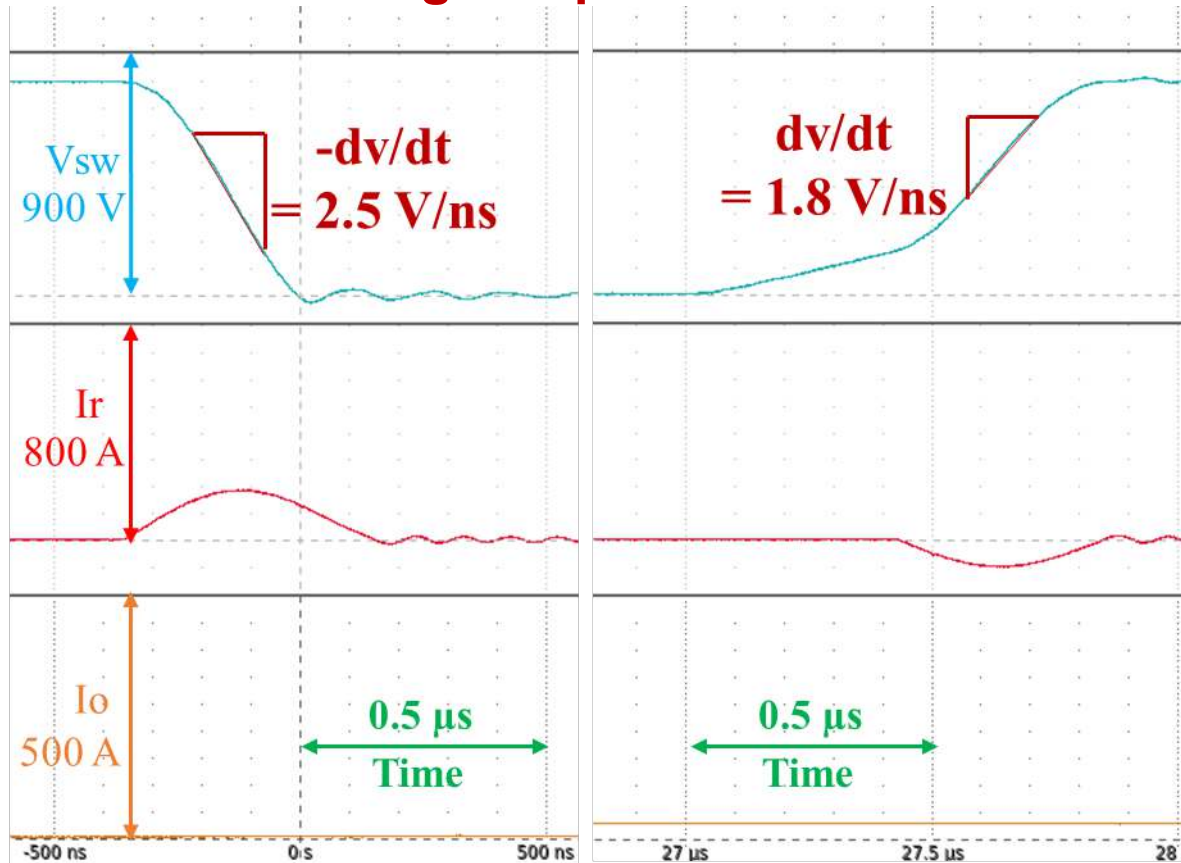


□ Adaptive time = $0.71\ \mu\text{s}$ at $I_o = 350\ \text{A}$, $V_{dc} = 800\ \text{V}$

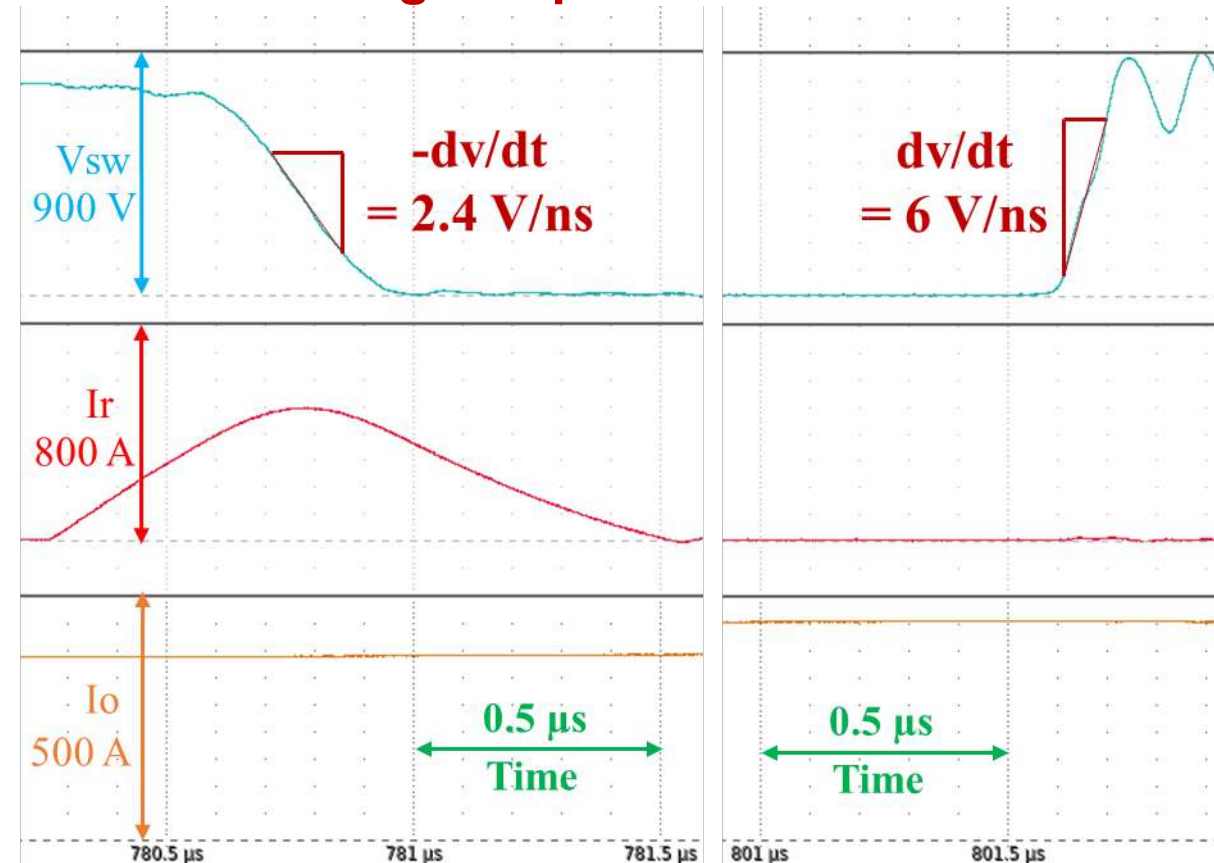


- ❑ Voltage slope dv/dt is verified below 6 V/ns at falling and rising edges with more than full range of load current variations (0 - 350 A)

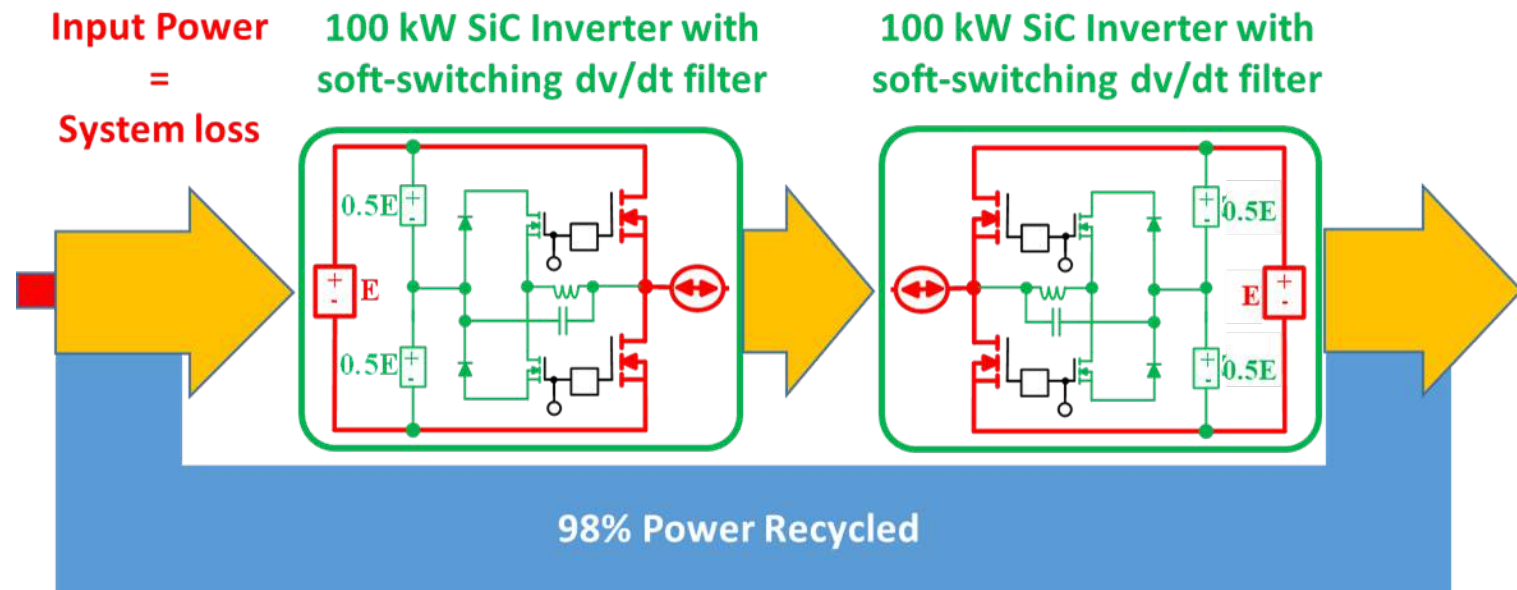
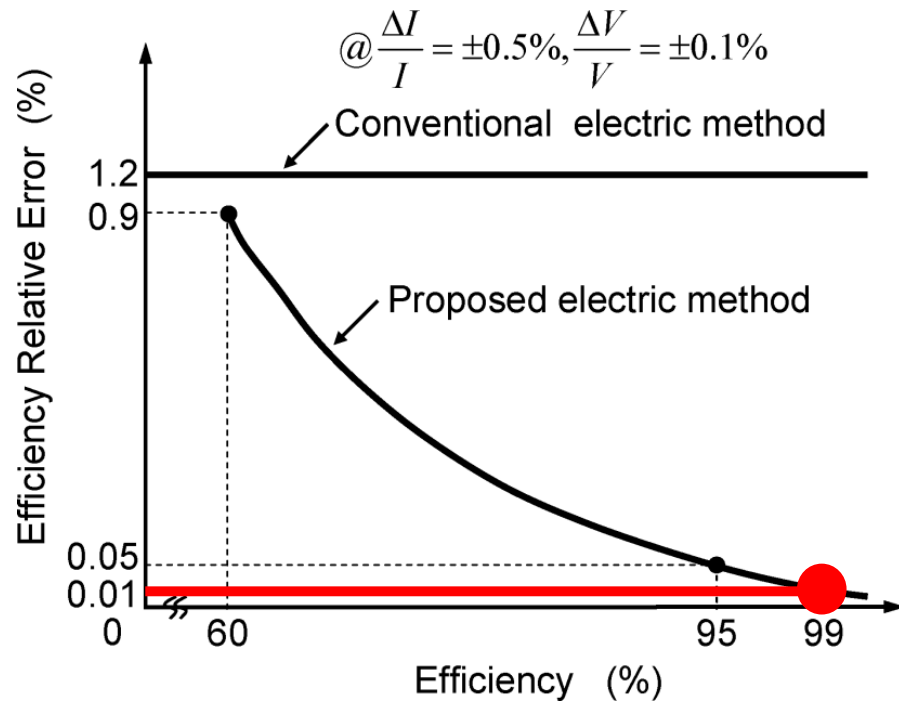
- **Voltage slope at zero load**



- **Voltage slope at 2X rated load**



- Based on the reference below, with the use of back-to-back regenerative measurement for high-efficiency inverter, the relative **efficiency error will stay below $\pm 0.01\%$** .
- Inverter efficiency measurement accuracy is expected to improve by a factor of **50**.



Reference: W. Yu, H. Qian and J. -S. Lai, "Design of High-Efficiency Bidirectional DC-DC Converter and High-Precision Efficiency Measurement," in IEEE Transactions on Power Electronics, vol. 25, no. 3, pp. 650-658, March 2010

- ❑ The proposed SiC inverter using parallel-connected dv/dt filter is a viable solution with significantly better performance than the state-of-art SiC inverters using series-connected dv/dt filter
 - ✓ **10 times of dv/dt filter volume reduction**
 - ✓ More than **50% savings** of SiC inverter total power loss
- ❑ A matrix coreless inductor is proposed, simulated and tested with near field leakage flux cancellation
 - ✓ **2 times of improvement** of energy density compared to the state-of-art coreless inductors
 - ✓ Quality factor (**Q**) is up to **124 at 1 MHz** frequency
- ❑ Single-phase inverter integrated with soft-switching dv/dt filter is fabricated and tested
 - ✓ Voltage slope is verified **below 6 kV/μs** with the **simple adaptive gating** for more than full range of load current variation (0 - 350 A)
- ❑ Inverter efficiency measurement accuracy is expected to improve by a **factor of 50**.
 - ✓ Based on back-to-back regenerative measurement method, the relative efficiency error will stay **below ± 0.01%** for the SiC inverter with the soft-switching dv/dt filter.