Development of Bi-Directional FETs, Modules and Circuits for Solar Converter Applications

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• Magnetics: Isaac Wong, Sagar Rastogi

Post Doc: • PV Converter Applications: Suyash Shah

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Complementary Activities

**APEC’23 Tutorial:** “Design & Integration of Solid-State Circuit Protection” (Monday AM, 20 March)

**Including the Lower Power Worlds**

- Starting DARPA 6mo./$680K Ph-0 project:
  DARPA’s: Next-Generation Microelectronics Manufacturing initiative
  “Requirements for a 3DHI Power Microsystem (3DHIP) and Manufacturing Center”

- Co-Chair: IEEE Heterogeneous Integration Roadmap
  Chap 10, “Integrated Power Electronics” – 4 PARTS
  Synergy with PELS ITRW roadmap

- Chair IEEE-EPS: “Power & Energy” Technical Committee
  Co-Sponsor 3D-PEIM
**Project Goals**

Cyclo-Converter based 1-Ø and 3-Ø Grid Connected PV Inverter
Enabled by Monolithically Integrated SiC 4-QPS at 1200V, 10-25A,
Advanced Packaging, Topologies & Advanced Magnetics

Elimination of DC electrolytic capacitors. Only filter capacitors are film with low VA rating and low ESR
All switches can be SiC 4-QPS – hence standardized modules

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High-frequency link 1-Ø converter using 4-QPS enabled cyclo-converter

High-frequency link 3-Ø using 4-QPS enabled cyclo-converter.
Project Objectives

Develop BiDirectional FET (BiDFET) dies rated at
• 1200V/10A
• 1200V/25A

Develop packaging for die and converter testing and development for
• single-dies
• two parallel-dies per switch
• verification of EMMs function

Develop and demo a PV-to-1Ø AC Grid Connected Converter Hardware Prototype at 1.5 kW [2.1kW]
• Gate driver design and operation for BiDFET (i.e. 4-QPS) –
  • High frequency (100kHz), short circuit protection, with diagnostics and prognostics
  • Control of grid connected converter system (with low inertia), grid support functions

Design, develop and test transformer and inductor magnetics for
1.5kW and 15kW PV system
Monolithic Bi-Directional FET (BiDFET) Development
# SiC Monolithic Bi-Directional FET – BiDFET

Comparison of fabricated 1.2 kV 20 A BiDFET with previous bidirectional switch implementations

<table>
<thead>
<tr>
<th>Switch Configuration</th>
<th>Description</th>
<th>Number of Components</th>
<th>On-State Voltage Drop (V)</th>
<th>Switching Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode Bridge + Asymmetric IGBT</td>
<td>5</td>
<td>8.6 [2 diodes + 1 IGBT]</td>
<td>High</td>
<td></td>
</tr>
<tr>
<td>Asymmetric IGBTs + Freewheeling diodes</td>
<td>4</td>
<td>5.8 [1 diode + 1 IGBT]</td>
<td>High</td>
<td></td>
</tr>
<tr>
<td>Back-to-back symmetric IGBTs</td>
<td>2</td>
<td>2.2 [1 symmetric IGBT]</td>
<td>Very High</td>
<td></td>
</tr>
<tr>
<td>SiC Power MOSFETs + JBS diodes</td>
<td>4</td>
<td>3.1 [1 diode + 1 MOSFET]</td>
<td>Low</td>
<td></td>
</tr>
<tr>
<td>Back-to-back SiC Power MOSFETs + antiparallel and series JBS diodes</td>
<td>6</td>
<td>3.1 [1 diode + 1 MOSFET]</td>
<td>Low</td>
<td></td>
</tr>
<tr>
<td>Four-terminal SiC Monolithic BiFET</td>
<td>1</td>
<td>1.0 [1 BiFET]</td>
<td>Low</td>
<td></td>
</tr>
</tbody>
</table>
BiDFET Gen-1 Chip Design

- JBSFET Cells in Entire Active Area
- Cell Pitch = 6.1 mm
- Gate Oxide Thickness = 55 nm
- Channel Type = Accumulation
- Channel Length = 0.5 mm
- Contact Anneal Temperature = 900 °C
- Specific On-Resistance = 11.25 mW-cm²
- Each JBSFET Active Area = 0.45 cm²
- Expected JBSFET Resistance = 25 mW
- Expected BiDFET On-Resistance = 50 mW

Objective: Demonstrate First Monolithic 1.2 kV BiDirectional Switch

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**BiDFET Gen-1: Single Chip**

**Internal JBSFET cross-section**

- Source
- Gate Poly-Si
- Drain
- 10 μm N-DRIFT
- 8 × 10^{18} cm^{-3}
- N+ SUBSTRATE
- 350 μm, 0.02 0.3 cm
- W_{oxi}/2 = 6.1 μm
- W_{ox2}/2 = 1.5 μm

**Fabricated BiDFET die**

- 10.4 mm
- 11 mm
- 40 nm

**Custom-designed 4-terminal package for the BiDFET**

- Module Area = 3.22 cm²

- Blocking Voltage > 1400 V
- On-Resistance = 50 mΩ
- First Pass Success
- Used to demo 1-ph 2.3 kW converter
- C_{iss} = 11,000 pF
- C_{oss} = 500 pF at 1000 V
- C_{rss} = 50 pF at 1000 V
1.2 kV BiDFET: DPT Performance

**Test Conditions:** $V_{\text{DC}}=800 \text{ V}$, $R_{\text{Gate}}=10\Omega$

**HS Switch:** 1.2 kV BiDFET ($V_{G_{1T1}} = -5$, $V_{G_{1T1}} = 20 \text{ V}$)

**LS Switch:** 1.2 kV BiDFET ($V_{G_{1T1}} = -5/20 \text{ V}$, $V_{G_{2T2}} = 20 \text{ V}$)

- Switching losses increase by 1.71x when $I_{\text{ON}}$ rises from 10 to 20 A.
- A current overshoot during turn-on is due to output capacitance of HS switch.
- Reduced output capacitance of HS-Sw reduces switching loss $T_c$.
- Switching losses decrease by 17% as $T_c$ increases from 25 °C to 140 °C.

**Graphs:**

- **Switching Voltage ($V_{T2-T1}$)**:
  - $I_{T2T1}=8-20 \text{ A}$, $T_c=25^\circ \text{C}$

- **Current ($I_{T2T1}$)**:
  - $I_{T2T1}=8-20 \text{ A}$, $T_c=25^\circ \text{C}$

- **Gate Voltage ($V_{G1-T1}$)**:
  - $V_{G1-T1}=-5/20 \text{ V}$, $V_{G2T2}=20 \text{ V}$

- **Switching Losses ($E_{\text{SW,T}}$, $E_{\text{ON}}$, $E_{\text{OFF}}$)**:
  - $T_c=25-150^\circ \text{C}$

**Table:**

<table>
<thead>
<tr>
<th>$I_{\text{ON}}$ (A)</th>
<th>$E_{\text{ON}}$ ((\mu)J)</th>
<th>$E_{\text{OFF}}$ ((\mu)J)</th>
<th>$E_{\text{SW,T}}$ ((\mu)J)</th>
<th>$E_{\text{SW,T}}$ Norm.</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>559</td>
<td>271</td>
<td>830</td>
<td>0.9</td>
</tr>
<tr>
<td>10</td>
<td>620</td>
<td>298</td>
<td>918</td>
<td>1.0</td>
</tr>
<tr>
<td>12</td>
<td>688</td>
<td>360</td>
<td>1048</td>
<td>1.14</td>
</tr>
<tr>
<td>15</td>
<td>792</td>
<td>438</td>
<td>1230</td>
<td>1.34</td>
</tr>
<tr>
<td>18</td>
<td>889</td>
<td>553</td>
<td>1442</td>
<td>1.57</td>
</tr>
<tr>
<td>20</td>
<td>939</td>
<td>633</td>
<td>1572</td>
<td>1.71</td>
</tr>
</tbody>
</table>

**Diagrams:**

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- **Jayant Baliga <bjbaliga@ncsu.edu>**
- **Douglas Hopkins <dchopkins@ncsu.edu>**

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**SLIDE 9**

**SOLAR ENERGY TECHNOLOGIES OFFICE**

**U.S. Department Of Energy**

**FREEDM SYSTEMS CENTER**
BiDFET Gen-1: Parallel Chips

Objective: Demonstrate Reduced On-Resistance BiDFET by Paralleling Two Chips for 3-ph Converter Application

- Blocking Voltage > 1400 V
- On-Resistance = 25 mΩ
- Symmetric in 1st & 3rd Quadrant

Module Area = 27 cm²

Blocking Characteristics

Output Characteristics
BiDFET Gen-1: Parallel Chips

Objective: Demonstrate Reduced On-Resistance BiDFET by Paralleling Two Chips for 3-ph Converter Application

- Same transconductance in 1\textsuperscript{st} and 3\textsuperscript{rd} Quadrant
- Capacitances:
  - $C_{iss} = 15,100 \text{ pF}$
  - $C_{oss} = 1050 \text{ pF at 1000 V}$
  - $C_{rss} = 70 \text{ pF at 1000 V}$

  Capacitances are ~2x of a single BiDFET

- Turn-on and Turn-off like a single Gen-1 BiDFET chip
- Switching Losses (800 V, 20 A):
  - $E_{ON} = 1350 \text{ mJ}$
  - $E_{OFF} = 460 \text{ mJ}$
  - $E_{TOTAL} = 1810 \text{ mJ}$

Two Paralleled Gen-1 BiDFETs can handle 20 A.
Objective: Demonstrate Reduced On-Resistance BiDFET with Single Chip for 3φ Converter Application

Module with Single Gen-2 BiDFETs

Area = 13.7 cm²

Module with Two Gen-1 BiDFETs in Parallel

Area = 27.4 cm²

<table>
<thead>
<tr>
<th>Parameter, Units</th>
<th>Gen 1 (2 Chips)</th>
<th>Gen 2 (1 Chip)</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Area, cm²</td>
<td>2.28</td>
<td>1.14</td>
<td>2x</td>
</tr>
<tr>
<td>$R_{DS,ON}$, mΩ</td>
<td>25</td>
<td>27</td>
<td>-</td>
</tr>
<tr>
<td>$g_M$, S</td>
<td>15</td>
<td>15</td>
<td>-</td>
</tr>
<tr>
<td>$C_{ISS}$, pF</td>
<td>15100</td>
<td>11730</td>
<td>1.3x</td>
</tr>
<tr>
<td>$C_{OSS}$, pF</td>
<td>1050</td>
<td>600</td>
<td>1.75x</td>
</tr>
<tr>
<td>$C_{RSS}$, pF</td>
<td>70</td>
<td>70</td>
<td>-</td>
</tr>
<tr>
<td>$E_{ON}$, µJ</td>
<td>1350</td>
<td>1120</td>
<td>1.2x</td>
</tr>
<tr>
<td>$E_{OFF}$, µJ</td>
<td>460</td>
<td>250</td>
<td>1.8x</td>
</tr>
<tr>
<td>$E_{TOTAL}$, µJ</td>
<td>1810</td>
<td>1370</td>
<td>1.3x</td>
</tr>
</tbody>
</table>
Converter Demonstration

Hardware of the DC/AC DAB converter

2.1 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiFETs
**PV 1φ Grid Connected Cycloconv. Prototype at 2.3kW, 120/240/277V**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>120 V system</th>
<th>277 V / 240 V system</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>1kW</td>
<td>2.3kW / 2.1kW</td>
</tr>
<tr>
<td>High frequency inductance (referred to grid-side)</td>
<td>100 uH</td>
<td>30 uH</td>
</tr>
<tr>
<td>Turns-ratio</td>
<td>1:2.7</td>
<td>1:1.3</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>50 kHz</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Grid side filter capacitance</td>
<td>4 uF</td>
<td>4 uF</td>
</tr>
<tr>
<td>Grid side inductance</td>
<td>37 uH</td>
<td>37 uH</td>
</tr>
<tr>
<td>High-frequency transformer current (referred to grid-side)</td>
<td>10.1 Arms</td>
<td>11.6 Arms / 10.6 Arms</td>
</tr>
<tr>
<td>Grid-side capacitor current</td>
<td>4.6 Arms</td>
<td>6.4 Arms / 6.9 Arms</td>
</tr>
<tr>
<td>Grid-side inductor current</td>
<td>8.4 Arms</td>
<td>8.5 Arms</td>
</tr>
</tbody>
</table>
2.1kW, 1-ph Prototype Enabled by 1200V, 20A BiDFETs

- Full load operation at 400V in / 240V_{RMS} out, at 2.1 kW and Power factor: 0.9998
- THD in grid-side current: 4.8%

HF transformer voltages/current and grid side current at 100% load at 240 V AC voltage.
2.1kW, 1-ph Prototype Enabled by 1200V, 20A BiDFETs

Power factor and current THD distortion at 100% load, at 240 V AC voltage.

- Measured w/ Hioki Power Analyzer PW6001.
- Current sensors: 50 A, 2 MHz.
- Voltage potentiometers: 1000 V.
Efficiency can be improved by improving transformer design and reducing switching frequency for reduced turn-off losses.

Semiconductor efficiency estimated after segregating the transformer, inductor and filter losses.

$P_{o,100\%} = 2328 \text{ W}$
Custom Packaging of 4-QPS
Early Stage Discrete-Die Bidirectional Switch

- The challenge for the packaging with the new 4-QPS is to provide ultra-low electrical and thermal resistances in a very high-density package at low cost.
- “Early Stage” package used two conventional MOSFETs

Electrical testing results:
- Total package resistance added 15% of $R_{ds(on)}$ (=25 mΩ)
- Leakage drain current ($I_{dss}$) were 2 uA @ $V_{ds}$=1200V, under the typ. value of the datasheet
Discrete 1.2kV/10A Monolithic BiDFET Packages

Discrete 1.2kV/10A BiDFET packages:
- 4-terminal PKG
- 12-terminal PKG

Interconnection:
- Two 5-mil Al wires for G1, G2, KS1, KS2
- Twelve 5-mil Al wires for T1 and T2
ERCD vs DBC Performance

Thermal-mechanical reliability comparison:
Only “dual ERCD” and “ERCD/DBC” can pass the failure criteria for SAC305 and SiC device.

The “trigger” is Organic Dielectric with ≥8W/mK @ 120µm thick. This is better than 380µm (15mil) Al₂O₃ in thermal performance.

[Al₂O₃ Ribbon ceramic at 36W/mK @ 120µm thickness surpasses AlN]

(Simulated) Thermal Resist. junction-to-case

Max. Principal Stress_SiC Chip | Eq. Plastic Strain_SAC305 Solder
--- | ---
Dual DBC | SIC<br>SAC-305
Dual ERCD | SIC<br>SAC-305
ERCD/DBC | SIC<br>SAC-305
DBC/ERCD | SIC<br>SAC-305

Normalization

- Normalized to DBC

0.0964 °C/W<br>0.0927 °C/W<br>0.0962 °C/W<br>0.0928 °C/W

Dual DBC<br>Dual ERCD<br>ERCD/DBC<br>DBC/ERCD
Short-circuit Ruggedness Improvement

To increase short circuit capability, a low voltage Si enhancement mode MOSFET (EMM) connected with the BiDFET source. Due to the lower saturation current of the EMM compared with the BiDFET, the peak short-circuit current can be reduced in the latter under fault conditions, consequently increasing the $t_{SC}$ (duration under short circuit condition). The gate bias of the EMM can be varied to obtain the desired saturation current [1].

An integrated EMM 1.2kV/10A BiDFET module was devised to improve BiDFET short circuit capability.

Two paralleled EMMs were used to reduce series resistance.

To achieve ultra-low resistance, two rows of 8-mil heavy Al wires were applied to each JBSFET.
Assessment of Continuous Current Capability

<table>
<thead>
<tr>
<th>Component</th>
<th>Material</th>
<th>Max. operating temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heat slug</td>
<td>Cu</td>
<td>&gt;300</td>
</tr>
<tr>
<td>Conductor Layer</td>
<td>Cu</td>
<td>&gt;300</td>
</tr>
<tr>
<td>Pin</td>
<td>Cu</td>
<td>&gt;300</td>
</tr>
<tr>
<td>Wire</td>
<td>Al</td>
<td>&gt;600</td>
</tr>
<tr>
<td>Encapsulant</td>
<td>Epoxy resin and hardener</td>
<td>&gt;190</td>
</tr>
<tr>
<td>Solder</td>
<td>Sn95Sb5</td>
<td>&gt;200</td>
</tr>
<tr>
<td>BiDFET</td>
<td>SiC</td>
<td>175</td>
</tr>
<tr>
<td>EMM</td>
<td>Si</td>
<td>175</td>
</tr>
<tr>
<td>Dielectric</td>
<td>ERCD</td>
<td>300</td>
</tr>
</tbody>
</table>

(a) Chip limitation: 19.5 A
(b) Package limitation: 119.1 A
For increased current rating of a half-bridge, TWO BiDFETs are connected in parallel per switch (SW) and TWO switches are connected in series for a half-bridge.

To minimize the parasitic resistance and inductance in the power loop, 20-mil stitched Al wires are bonded on each JBSFET. The SMD signal pins and THD power pins assist alignment for mounting module on PCB.
Single-Side Cooled (SSC) Parallel BiDFET Half-Bridge Module

Four side holes on the eIMS provide heat sink/cool plate mounting & provides the convenience for paralleling multiple modules or building a three-phase inverter.
Thermal Simulation for eIMS & Parallel 1.2kV/10A BiDFET

• To simplify the simulation, an equivalent heat convective coefficient, $h_{\text{eff}}$, was applied to the bottom of the eIMS. The $h_{\text{eff}}$, obtained by experiment, 750 W/m$^2$K.

• The max. current was deduced from the $R_{\text{ds-on}}$, $R_{\varphi jc}$, max. $T_j$, and $T_a$. In addition, max. power was deduced from $R_{\varphi jc}$, max. $T_j$, and $T_a$.

• Results show the max. current and max. power comparison of single- and parallel-die half-bridge modules at $h_{\text{eff}}$=750 W/m$^2$K and $T_a$=25°C.

Size: 35x82 mm

$I_{\text{max}}$ = 54.9 A
$P_{\text{max}}$ = 226.8 W

Size: 19x54 mm

$I_{\text{max}}$ = 25.4 A
$P_{\text{max}}$ = 97.4 W
Parasitic Extraction Analysis

- This study conducted parasitics extraction analysis, including the resistance and inductance under DC and 1 MHz matching BiDFET turn-on and turn-off speed.
- To consider that users may only connect one side of the signal pins which lead to a longer driving loop for one of the BiDFETs in a SW, this study extracted both near and far driving loop, as shown below.

<table>
<thead>
<tr>
<th></th>
<th>Power loop</th>
<th>Driving loop (near)</th>
<th>Driving loop (far)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Resistance (mΩ)</td>
<td>0.49</td>
<td>7.19</td>
<td>10.46</td>
</tr>
<tr>
<td>AC Resistance @ 1MHz (mΩ)</td>
<td>2.22</td>
<td>7.30</td>
<td>14.49</td>
</tr>
<tr>
<td>AC Inductance @ 1MHz (nH)</td>
<td>22.36</td>
<td>5.62</td>
<td>7.82</td>
</tr>
</tbody>
</table>
Single-Die, Three-Phase Module

- To increase power density and reduce inductance, SIX 1.2kV/50mΩ BiDFETs formed a 3Ø module.
- Temperature sense pins (T) were added.
- To minimize power loop R&L, multiple Al bond wires and jumpers were adopted.
- The SMD signal pins and THD power pins assist alignment for mounting the module on PCB.
Steady-State Thermal-Electric Simulation (High $T_{ambient}$)

$T_{j,max} = 150^\circ C$, $T_{ambient} = 70^\circ C,$

Selected design point $h_{eff} = 1250 \text{ W/m}^2\text{K}$ allows BiDFET to operate at 33A.
Parasitic Extraction Analysis

- Module design focuses on minimizing point-to-point inductance within its housing.
- Extracted are the DC resistance and AC inductance of the driving and power paths at 1 MHz, which is representative of the BiDFET turn-on and turn-off speed.

<table>
<thead>
<tr>
<th></th>
<th>Driving loop (near)</th>
<th>Power path_U</th>
<th>Power path_V</th>
<th>Power path_W</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Resistance (mΩ)</td>
<td>7.19</td>
<td>0.55</td>
<td>4.61</td>
<td>4.79</td>
</tr>
<tr>
<td>AC Inductance @ 1MHz (nH)</td>
<td>5.62</td>
<td>10.68</td>
<td>20.35</td>
<td>46.98</td>
</tr>
</tbody>
</table>
**Interstial (shielding) Layer Development in Ultra-Thin Dielectrics**

Parasitic capacitance

\[ C = \varepsilon_0 \times \varepsilon_r \times \frac{A}{D} \]

\[ \Delta I = C \times \frac{dv}{dt} \]  
Unwanted CM current

- \( \varepsilon_0 \): permittivity of vacuum (8.854 \times 10^{-12} \text{ F/m})
- \( \varepsilon_r \): relative dielectric constant of medium
- \( A \): overlapping area of conductors
- \( D \): insulator thickness

**Solutions Of Baseplate Current Reduction**

Select low \( \varepsilon_r \) material, increase \( D \), and decrease \( A \), add external filters, add Interstitial conductor layer

**Thin organic/ceramic dielectrics**

**Al/Cu baseplate**

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• Two power devices, a half-bridge gate driver and ten 0402 MLCC decoupling capacitors are mounted on the top conductor layer.

• In a multi-layer IMS, an interstitial conductor layer (or shielding layer) is laminated by 120-um ERCD dielectrics on the top and bottom.

• Shielding layer uses through-hole vias to the top conductor and covers the top conductor pads with a minimal area for minimal capacitance.
Since the dv/dt and ringing frequency of the SW voltage can be up to a couple of hundred MHz, the power inductor $L$ and the decoupling capacitors $C_{Decap}$ can be regarded as open and short, respectively.

**Simplification of the CM Noise Impedance Model**

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**Full CM Noise Model**

**Simplified CM Noise Model**
Verifying optimized z-height ratio of the thin dielectrics

It indicates that the best thickness ratio of $T_1$ to $T_2$ is one for suppressing $I_{GND}$ or CM noise. A parametric study was carried out for validating the best thickness ratio. The highest product of $C_3$ and $C_6$ occurs at Case 5 which holds the same $T_1$ and $T_2$.

<table>
<thead>
<tr>
<th>Case</th>
<th>T1 (um)</th>
<th>T2 (um)</th>
<th>C3 (pF)</th>
<th>C6 (pF)</th>
<th>C3×C6 (pF^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>40</td>
<td>200</td>
<td>10.1</td>
<td>17.1</td>
<td>173.4</td>
</tr>
<tr>
<td>2</td>
<td>60</td>
<td>180</td>
<td>11.3</td>
<td>11.4</td>
<td>128.4</td>
</tr>
<tr>
<td>3</td>
<td>80</td>
<td>160</td>
<td>12.7</td>
<td>8.6</td>
<td>108.4</td>
</tr>
<tr>
<td>4</td>
<td>100</td>
<td>140</td>
<td>14.5</td>
<td>6.8</td>
<td>99.1</td>
</tr>
<tr>
<td>5</td>
<td>120</td>
<td>120</td>
<td>16.9</td>
<td>5.7</td>
<td>96.3</td>
</tr>
<tr>
<td>6</td>
<td>140</td>
<td>100</td>
<td>20.3</td>
<td>4.9</td>
<td>99.1</td>
</tr>
<tr>
<td>7</td>
<td>160</td>
<td>80</td>
<td>25.4</td>
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