Development of Bi-Directional FETs, Modules and Circuits for Solar Converter Applications

Principal Investigators:

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Graduate Students:

- Device: Aditi Agarwal, Kijeong Han, Ajit Kanale
- Advanced Packaging: Tzu-Hsuan Cheng
- PV converter: Ramandeep Narwal
- Magnetics: Isaac Wong, Sagar Rastogi

Post Doc:

- PV Converter Applications: Suyash Shah

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Complementary Activities

APEC'23 Tutorial: "Design & Integration of Solid-State Circuit Protection" (Monday AM, 20 March)

Including the Lower Power Worlds

- Starting DARPA 6mo./$680K Ph-0 project:
  DARPA's: Next-Generation Microelectronics Manufacturing initiative
  "Requirements for a 3DHI Power Microsystem (3DHIP) and Manufacturing Center"
- Co-Chair: IEEE Heterogeneous Integration Roadmap
  Chap 10, *"Integrated Power Electronics"* – 4 PARTS
  Synergy with PELS ITRW roadmap
- Chair IEEE-EPS: *"Power & Energy" Technical Committee*
  Co-Sponsor 3D-PEIM

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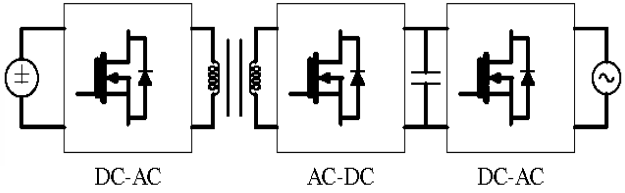
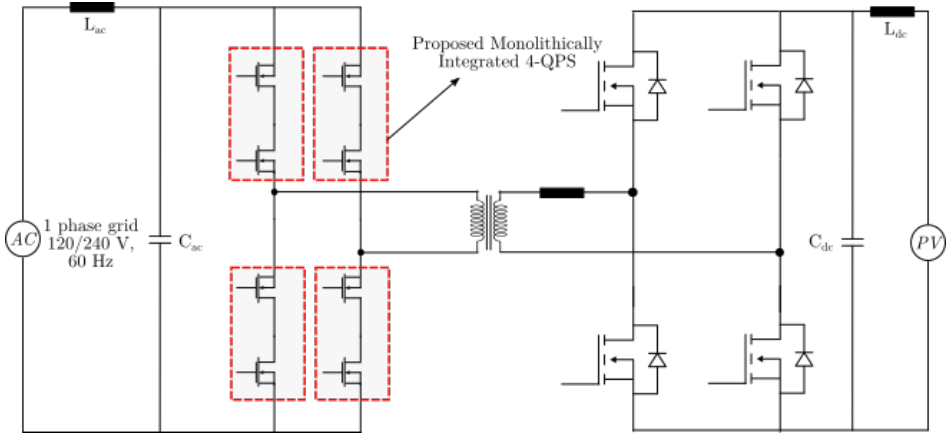
Project Goals

Cyclo-Converter based 1-Ø and 3-Ø Grid Connected PV Inverter Enabled by Monolithically Integrated SiC 4-QPS at 1200V, 10-25A, Advanced Packaging, Topologies & Advanced Magnetics

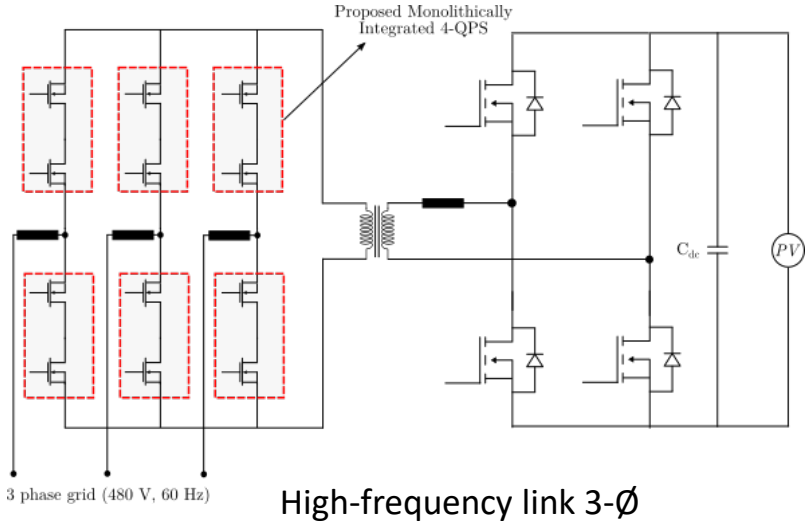
Conventional architecture for DC-AC conversion



Elimination of DC electrolytic capacitors. Only filter capacitors are film with low VA rating and low ESR
All switches can be SiC 4-QPS – <u>hence standardized modules</u>



High-frequency link **1-Ø** converter
using 4-QPS enabled cyclo-converter



High-frequency link 3-Ø
using 4-QPS enabled cyclo-converter.

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Project Objectives

Develop BiDirectional FET (BiDFET) dies rated at
- 1200V/10A
- 1200V/25A

Develop packaging for die and converter testing and development for
- single-dies
- two parallel-dies per switch
- verification of EMMs function

Develop and demo a PV-to-1Ø AC Grid Connected Converter Hardware Prototype at 1.5 kW [*2.1kW*]
- Gate driver design and operation for BiDFET (i.e. 4-QPS) –
  - High frequency (100kHz), short circuit protection, with diagnostics and prognostics
- Control of grid connected converter system (with low inertia), grid support functions

Design, develop and test transformer and inductor magnetics for 1.5kW and 15kW PV system

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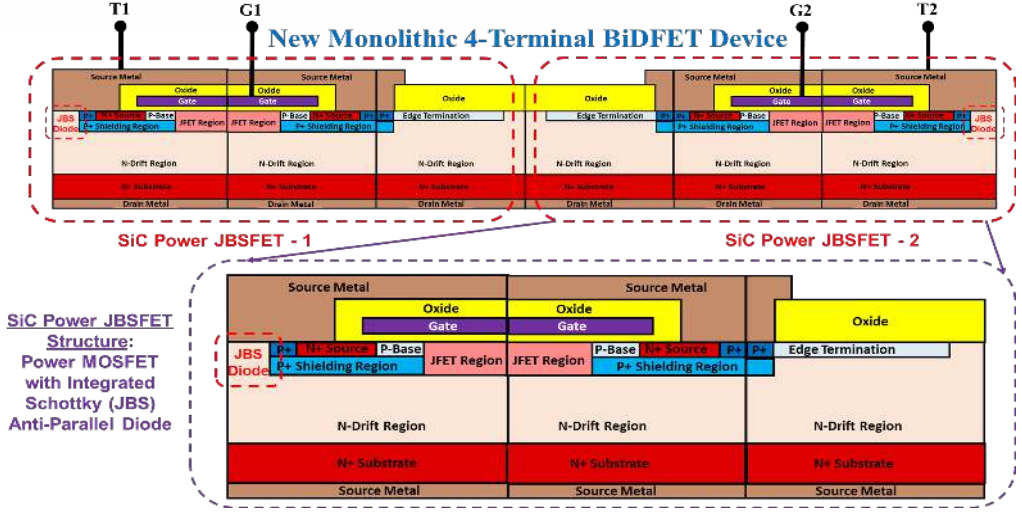
Monolithic Bi-Directional FET (BiDFET) Development



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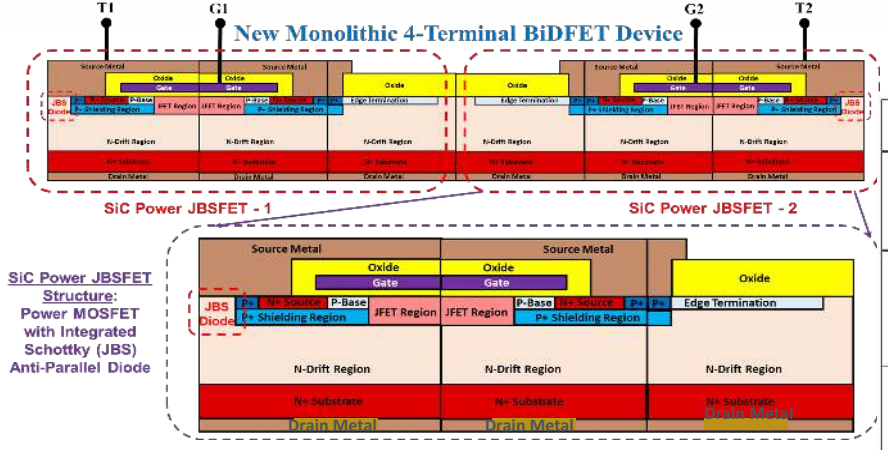
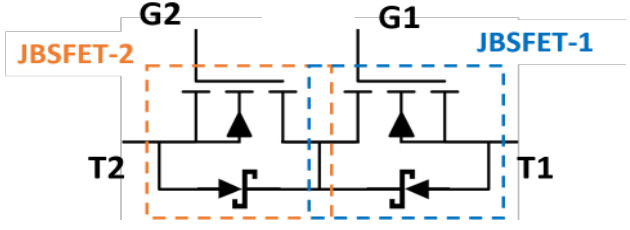
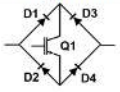
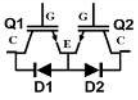
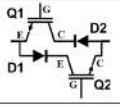
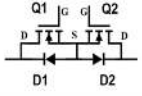
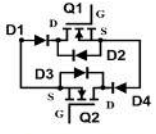
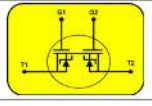
SiC Monolithic Bi-Directional FET – BiDFET





Comparison of fabricated 1.2 kV 20 A BiDFET with previous bidirectional switch implementations

Switch Configuration	Description	Number of components	On-State Voltage Drop (V)	Switching Loss
	Diode Bridge + Asymmetric IGBT Neft & Schauder, IEEE Trans. Ind. Appl., vol. 28, pp. 546-551, 1992	5	8.6 [2 diodes + 1 IGBT]	High
	Asymmetric IGBTs + Freewheeling diodes Moghe et al., ECCE, pp. 3848-3855, 2012	4	5.8 [1 diode + 1 IGBT]	High
	Back-to-back symmetric IGBTs Takei et al., ISPSD, pp. 413-416, 2001	2	2.2 [1 symmetric IGBT]	Very High
	SiC Power MOSFETs + JBS diodes Safari et al., IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2584-2596, 2014	4	3.1 [1 diode + 1 MOSFET]	Low
	Back-to-back SiC Power MOSFETs + antiparallel and series JBS diodes Ahmed et al., IEEE Trans. Power Electron., vol. 32, pp. 1232-1244, 2017	6	3.1 [1 diode + 1 MOSFET]	Low
	Four-terminal SiC Monolithic BiDFET	1	1.0 [1 BiDFET]	Low

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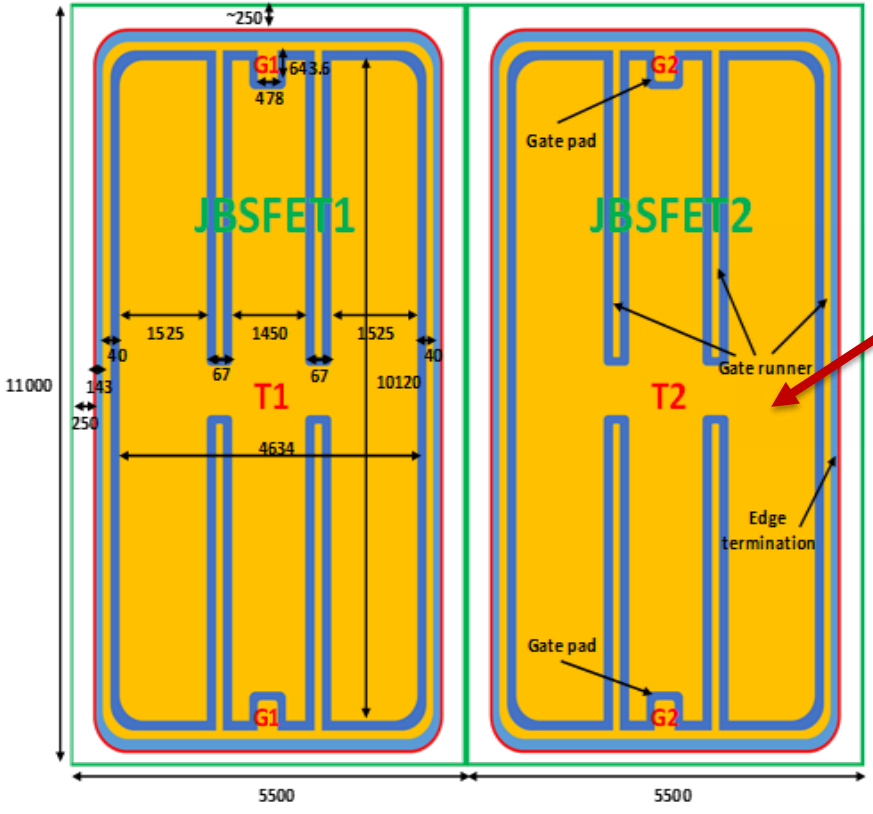
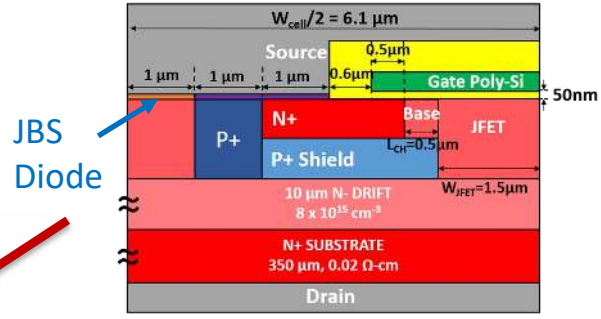
BiDFET Gen-1 Chip Design

Objective: Demonstrate First Monolithic 1.2 kV BiDirectional Switch





- JBSFET Cells in Entire Active Area
- Cell Pitch = 6.1 mm
- Gate Oxide Thickness = 55 nm
- Channel Type = Accumulation
- Channel Length = 0.5 mm
- Contact Anneal Temperature = 900 °C
- Specific On-Resistance = 11.25 mW-cm^2
- Each JBSFET Active Area = 0.45 cm^2
- Expected JBSFET Resistance = 25 mW
- Expected BiDFET On-Resistance = 50 mW

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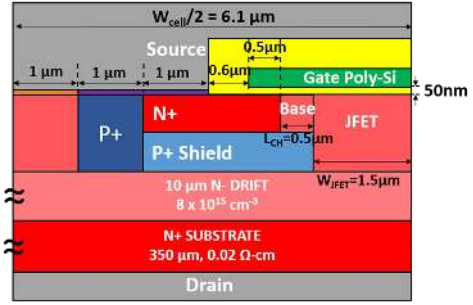
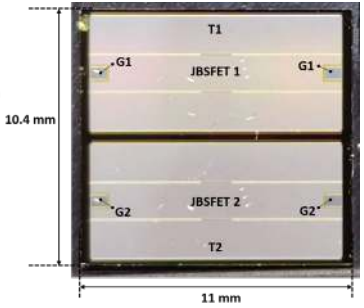
BiDFET Gen-1: Single Chip

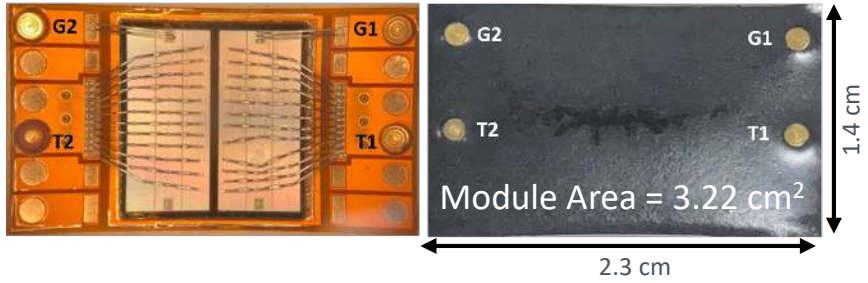
Internal JBSFET cross-section



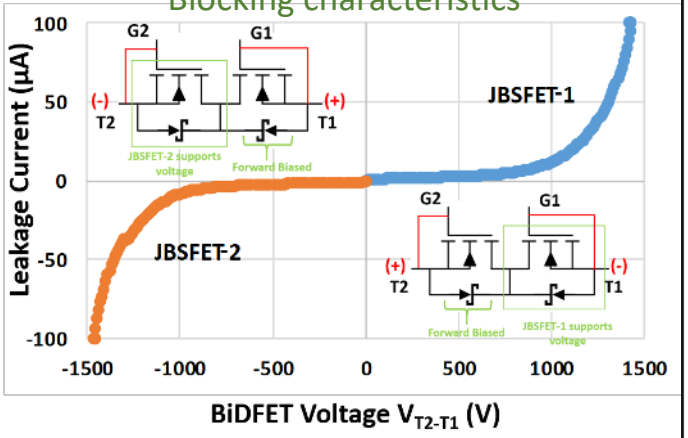
Fabricated BiDFET die

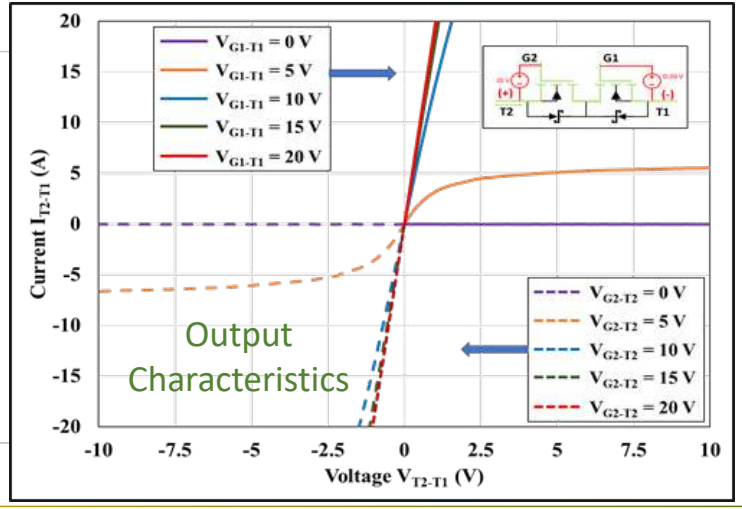


Custom-designed 4-terminal package for the BiDFET



Blocking characteristics





- Blocking Voltage>1400 V
- On-Resistance = 50 mΩ
- First Pass Success
- Used to demo 1-ph 2.3 kW converter
- C_{iss} = 11,000 pF
- C_{oss} = 500 pF at 1000 V
- C_{rss} = 50 pF at 1000 V

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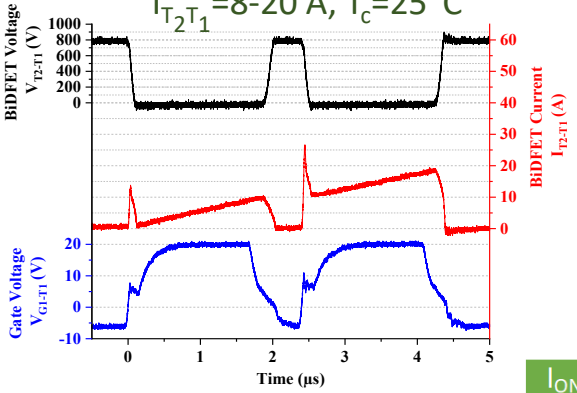
1.2 kV BiDFET: DPT Performance

Test Conditions: V_{DC}=800 V, R_{Gate}=10Ω

LS Switch: 1.2 kV BiDFET ($V_{G_1T_1}$ = -5/20 V, $V_{G_2T_2}$ = 20 V)

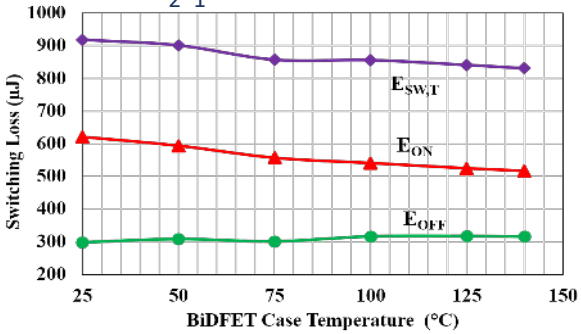
HS Switch: 1.2 kV BiDFET ($V_{G_1T_1}$ = -5 V, $V_{G_1T_1}$ = 20 V)

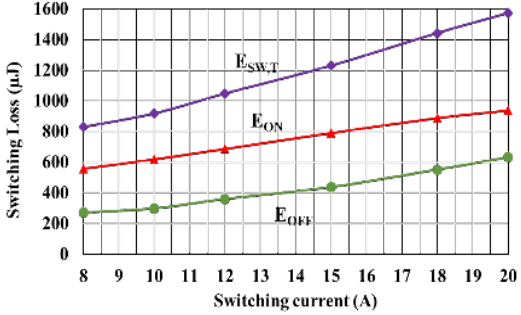
$I_{T_2T_1}$=8-20 A, T_c=25°C



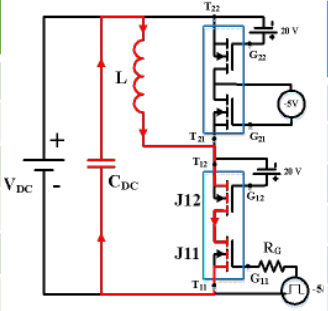
- Switching losses increase by 1.71x when I_{ON} rises from 10 to 20 A.
- A current overshoot during turn-on is due to output capacitance of HS switch.
- Reduced output capacitance of HS-Sw reduces switching loss T_C.
- Switching losses decrease by 17% as TC increases from 25 °C to 140 °C.

$I_{T_2T_1}$=10 A, T_c=25-150°C





I_{ON} (A)	E_{ON} (µJ)	E_{OFF} (µJ)	$E_{SW,T}$ (µJ)	$E_{SW,T}$ Norm.
8	559	271	830	0.9
10	620	298	918	1.0
12	688	360	1048	1.14
15	792	438	1230	1.34
18	889	553	1442	1.57
20	939	633	1572	1.71



T_C (°C)	E_{ON} (µJ)	E_{OFF} (µJ)	$E_{SW,T}$ (µJ)	$E_{SW,T}$ Norm.
25	620	298	918	1
50	593	308	901	0.96
75	556	301	857	0.9
100	540	316	856	0.87
125	524	317	841	0.85
140	516	315	831	0.83

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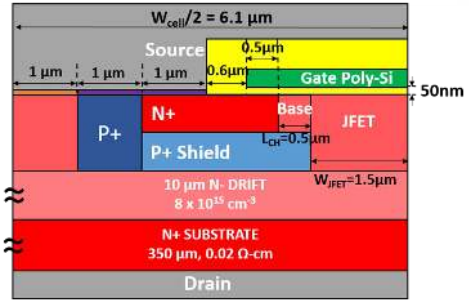
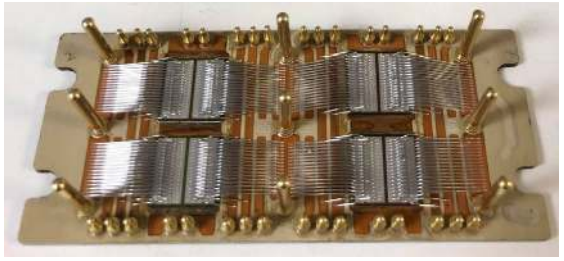
BiDFET Gen-1: Parallel Chips

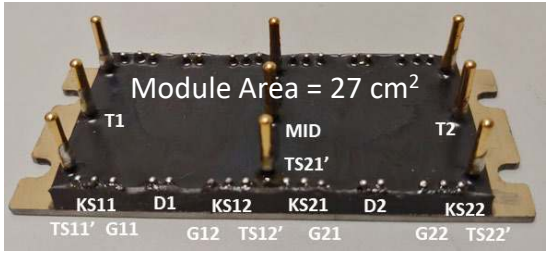
Objective: Demonstrate Reduced On-Resistance BiDFET by Paralleling Two Chips for 3-ph Converter Application

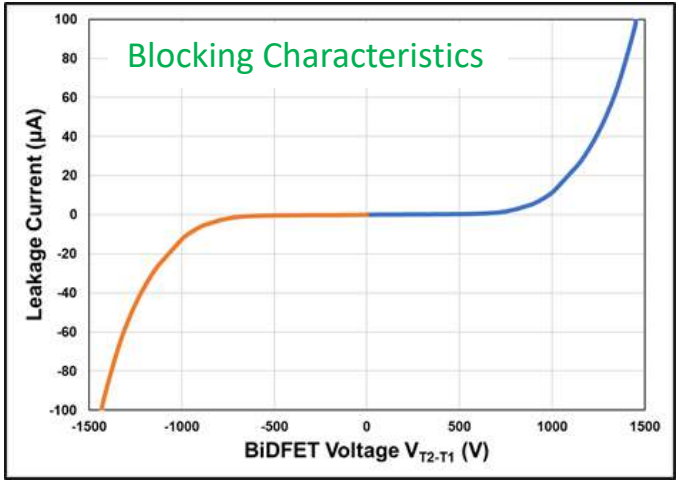
Internal JBSFET cross-section

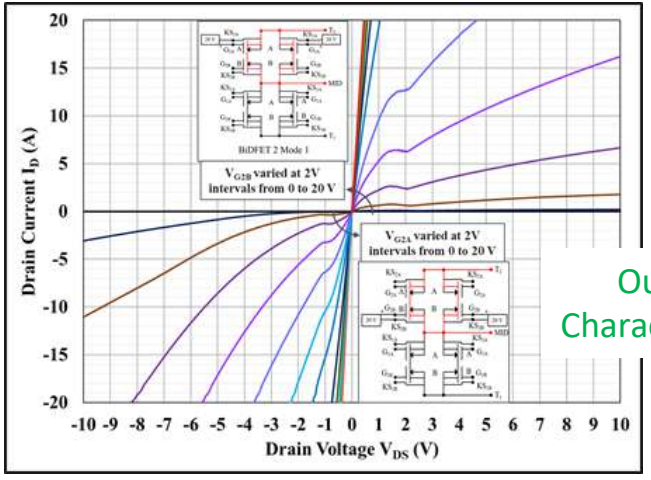


Custom-designed Half-Bridge Module with Paralleled BiDFET chips









Output Characteristics

- Blocking Voltage > 1400 V
- On-Resistance = 25 mΩ
- Symmetric in 1st & 3rd Quadrant

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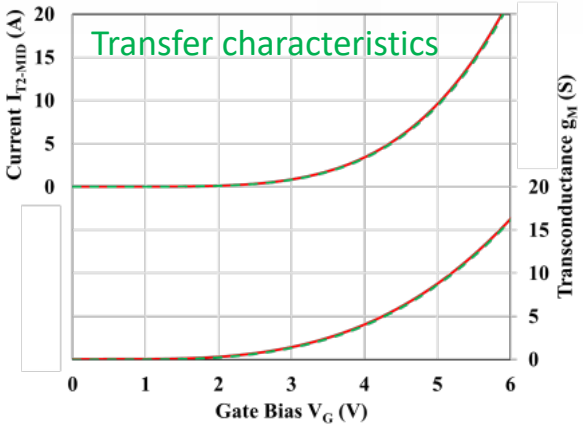
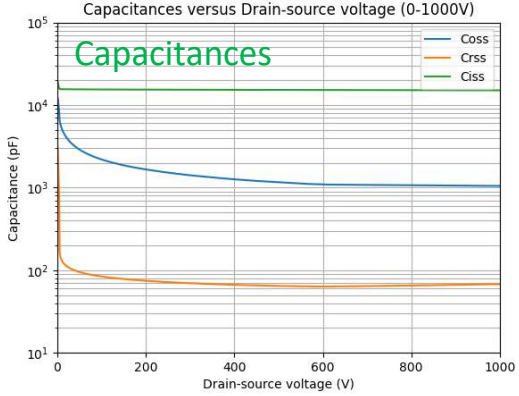
BiDFET Gen-1: Parallel Chips

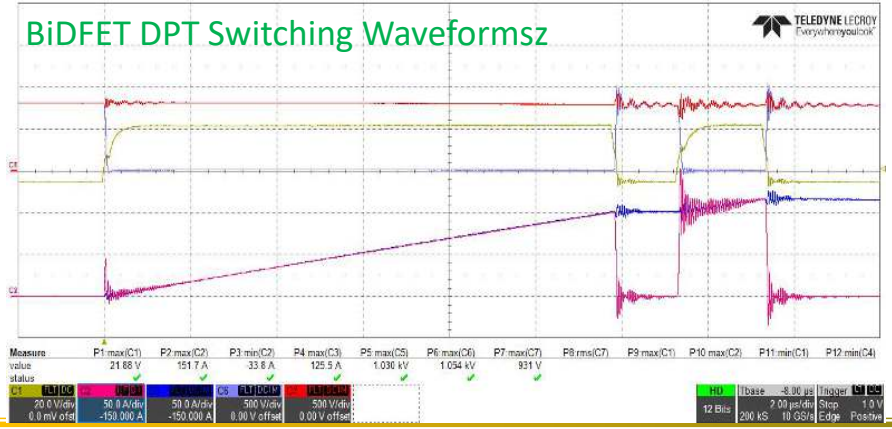
Objective: Demonstrate Reduced On-Resistance BiDFET by Paralleling Two Chips for 3-ph Converter Application





- Same transconductance in 1st and 3rd Quadrant
- Capacitances:
  - C_{iss} = 15,100 pF
  - C_{oss} = 1050 pF at 1000 V
  - C_{rss} = 70 pF at 1000 V

Capacitances are ~ 2x of a single BiDFET



- Turn-on and Turn-off like a single Gen-1 BiDFET chip
- Switching Losses (800 V, 20 A):
  - E_{ON} = 1350 mJ
  - E_{OFF} = 460 mJ
  - E_{TOTAL} = 1810 mJ

Two Paralleled Gen-1 BiDFETs can handle 20 A.

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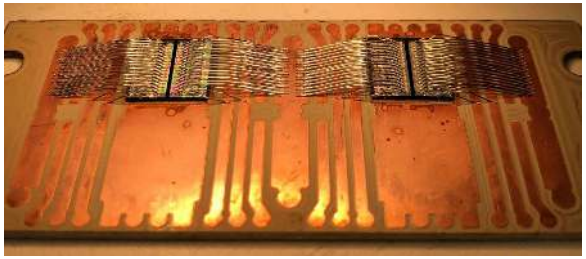
SiC BiDFET BP-2 Single Gen-2 Chip vs BP-1 Two Gen-1 Chips in Parallel

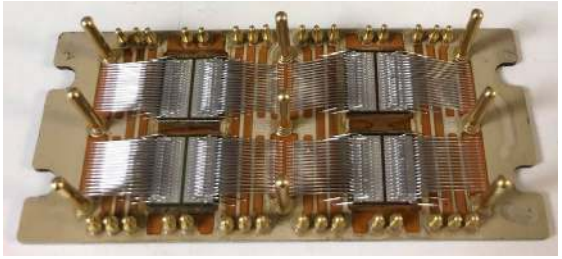
Objective: Demonstrate Reduced On-Resistance BiDFET with Single Chip for 3ϕ Converter Application

Module with Single Gen-2 BiDFETs



Area = 13.7 cm^2

Module with Two Gen-1 BiDFETs in Parallel



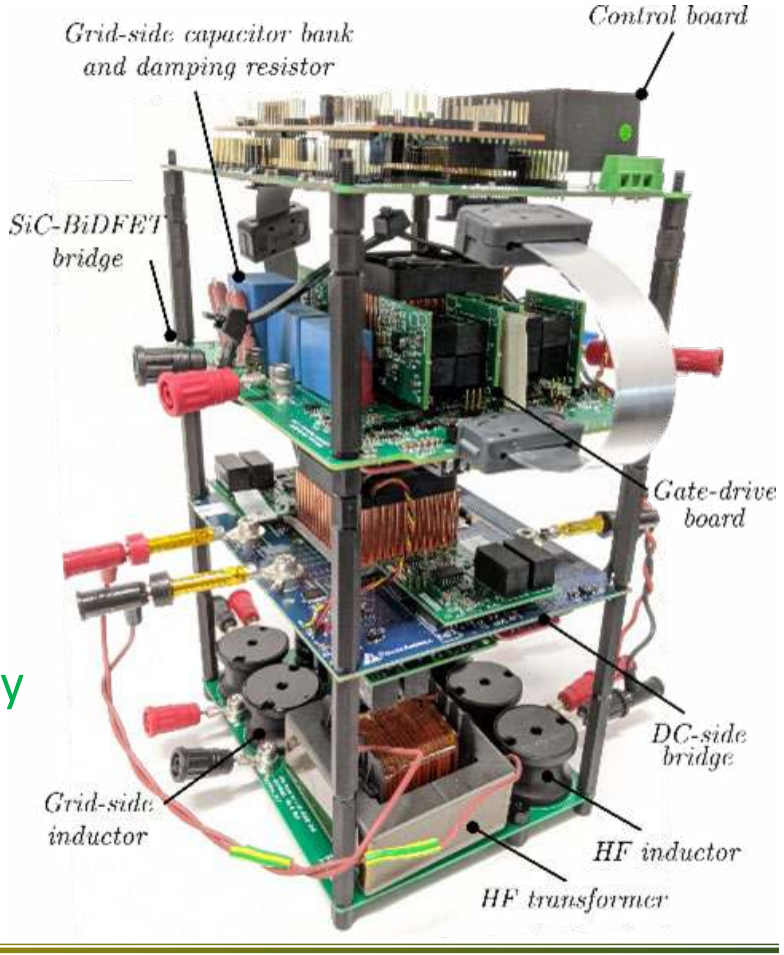
Area = 27.4 cm^2

Parameter, Units	Gen 1 (2 Chips)	Gen 2 (1 Chip)	Improvement
Chip Area, cm^2	2.28	1.14	2x
$R_{DS,ON}$, mΩ	25	27	-
g_M, S	15	15	-
C_{ISS}, pF	15100	11730	1.3x
C_{OSS}, pF	1050	600	1.75x
C_{RSS}, pF	70	70	-
E_{ON}, µJ	1350	1120	1.2x
E_{OFF}, µJ	460	250	1.8x
E_{TOTAL}, µJ	1810	1370	1.3x

Converter Demonstration

Hardware of the DC/AC DAB converter

2.1 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFETs



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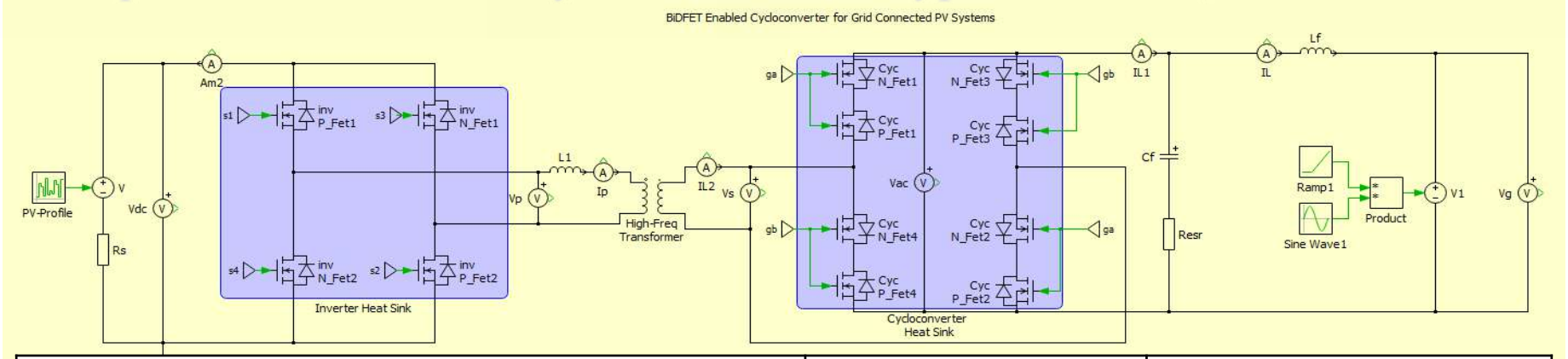
PV 1ϕ Grid Connected Cycloconv. Prototype at 2.3kW, 120/240/277V



Parameter	120 V system	277 V/ 240 V system
Power	1kW	2.3kW / 2.1kW
High frequency inductance (referred to grid-side)	100 uH	30 uH
Turns-ratio	1:2.7	1:1.3
Switching frequency	50 kHz	50 kHz
Grid side filter capacitance	4 uF	4 uF
Grid side inductance	37 uH	37 uH
High-frequency transformer current (referred to grid-side)	10.1 Arms	11.6 Arms / 10.6 Arms
Grid-side capacitor current	4.6 Arms	6.4 Arms /6.9 Arms
Grid-side inductor current	8.4 Arms	8.5 Arms

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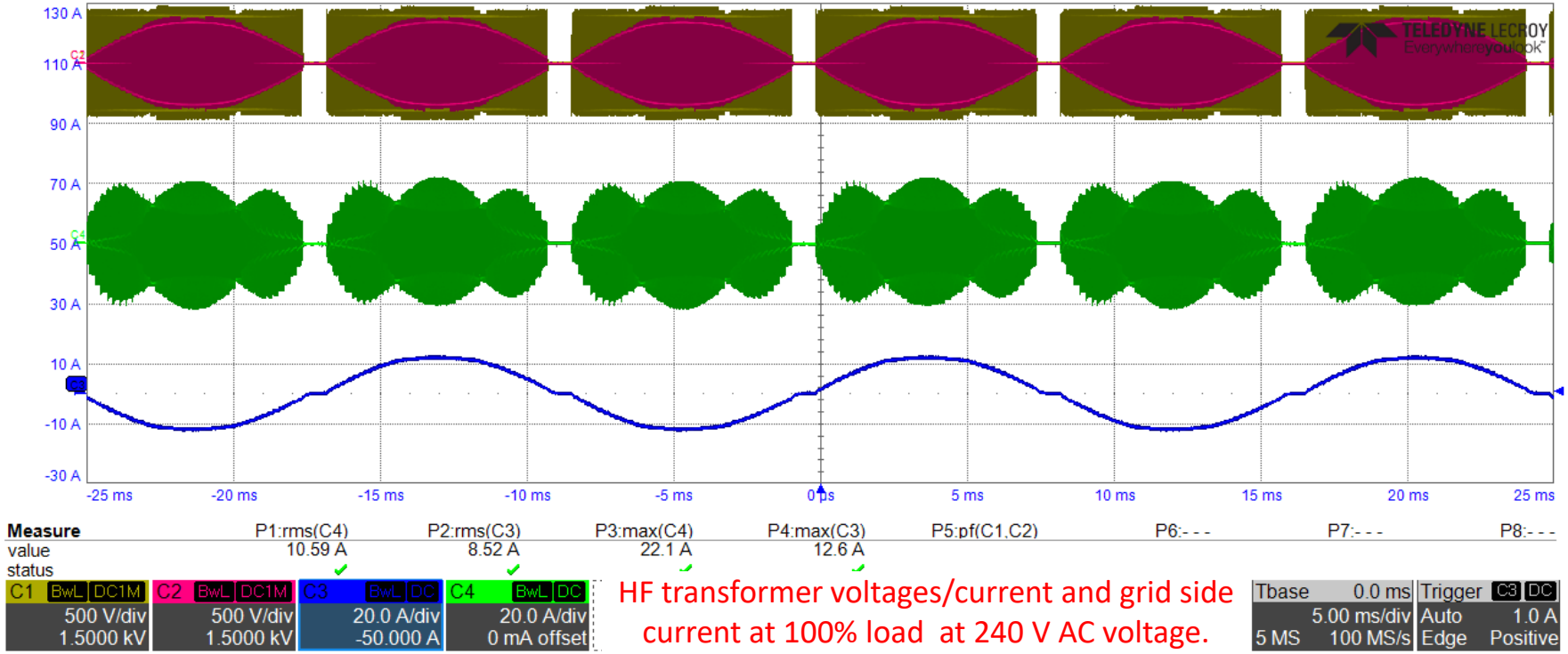
2.1kW, 1-ph Prototype Enabled by 1200V, 20A BiDFETs

- Full load operation at 400V in / 240V_{RMS} out, at 2.1 kW and Power factor: 0.9998
- THD in grid-side current: 4.8%



HF transformer voltages/current and grid side current at 100% load at 240 V AC voltage.

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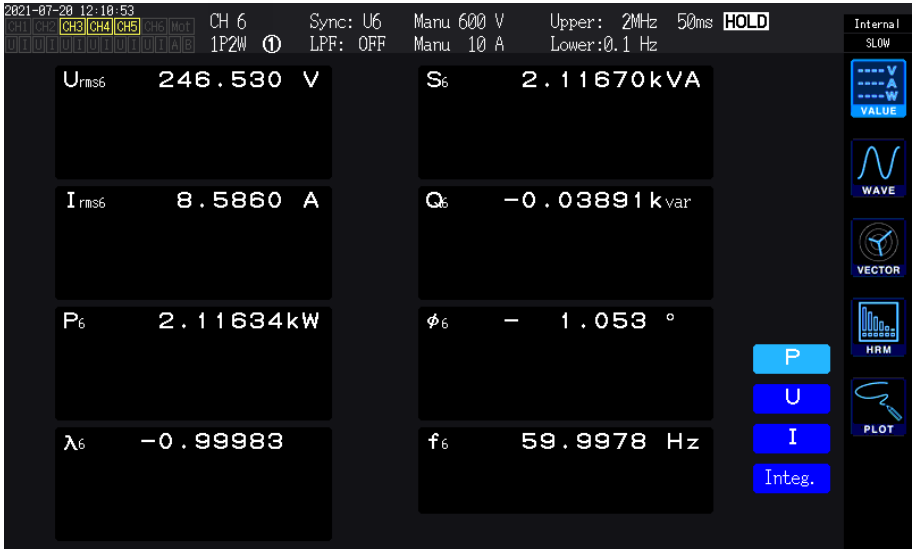
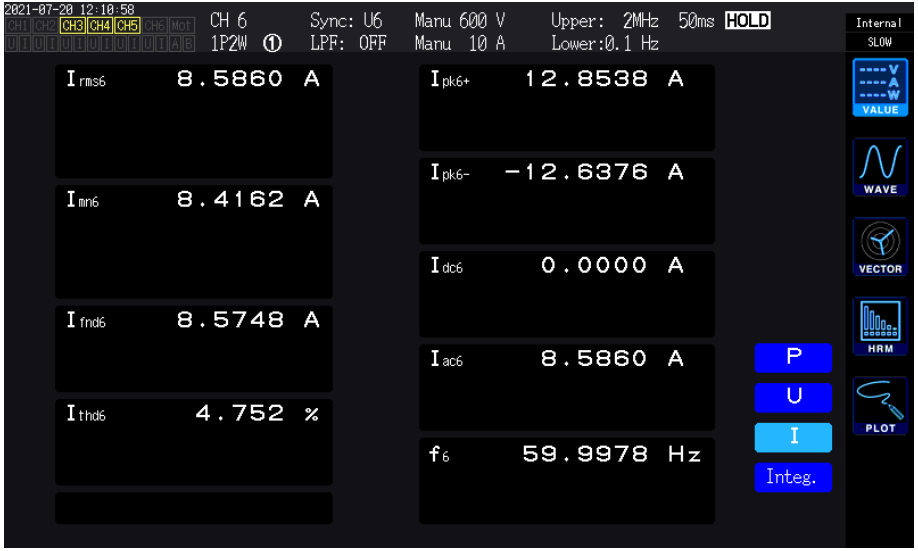
2.1kW, 1-ph Prototype Enabled by 1200V, 20A BiDFETs



Power factor and current THD distortion at 100% load, at 240 V AC voltage.



- Measured w/ Hioki Power Analyzer PW6001.
- Current sensors: 50 A, 2 MHz.
- Voltage potentiometers: 1000 V.

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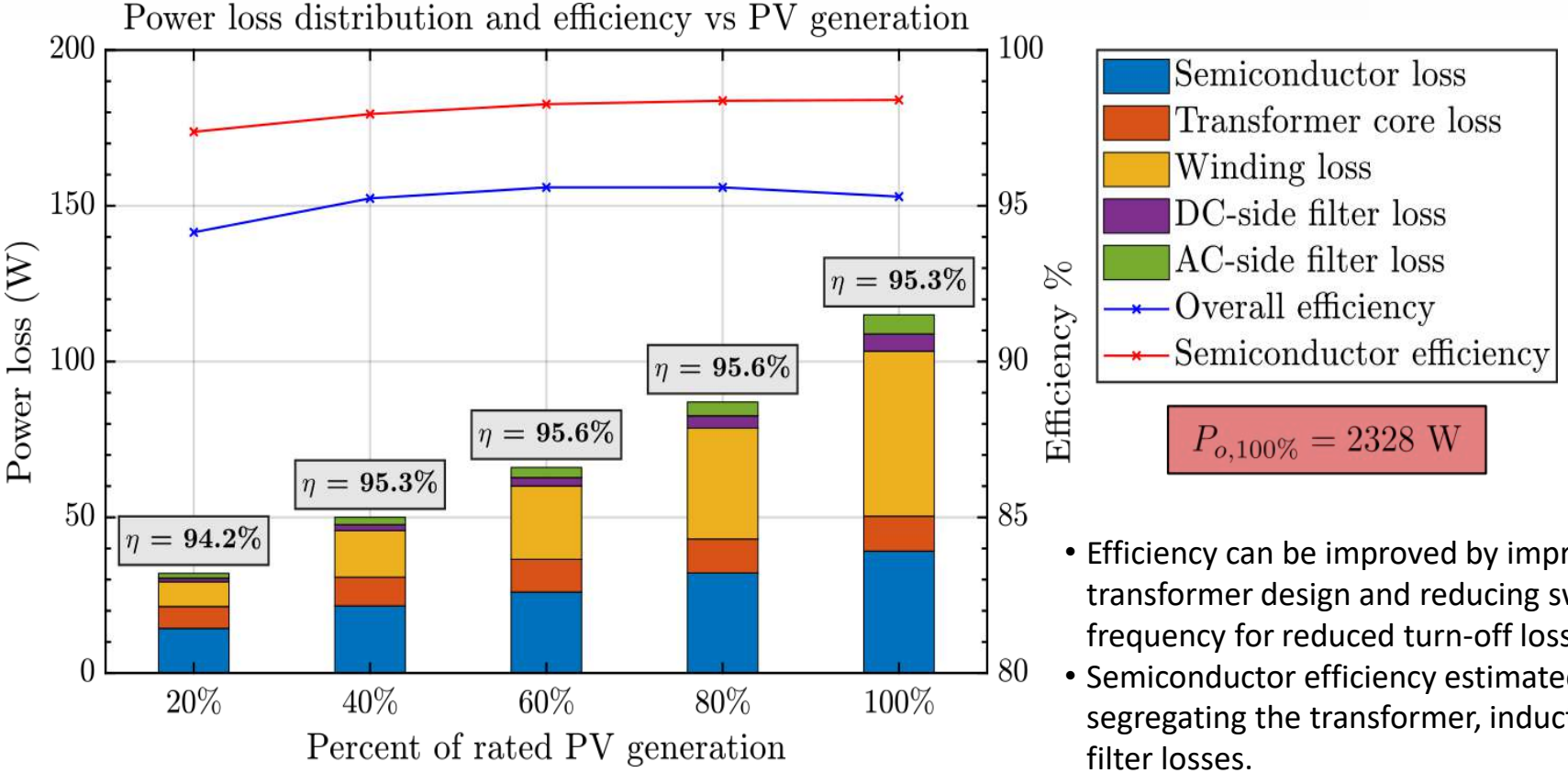
2.1kW, 1ph Grid Connected Converter with 1.2kV/20A BiDFETs



- Efficiency can be improved by improving transformer design and reducing switching frequency for reduced turn-off losses.
- Semiconductor efficiency estimated after segregating the transformer, inductor and filter losses.

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Custom Packaging of 4-QPS

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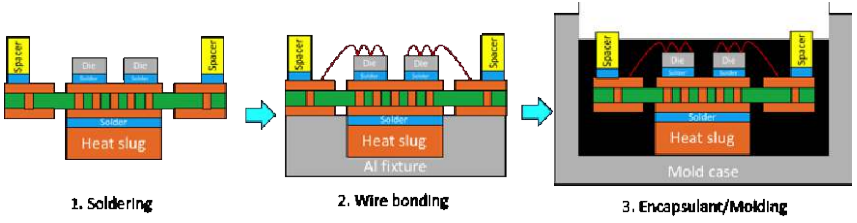
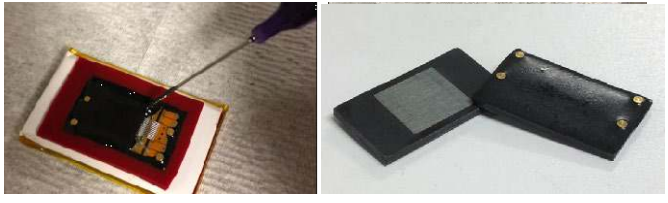
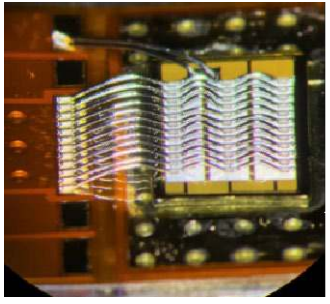
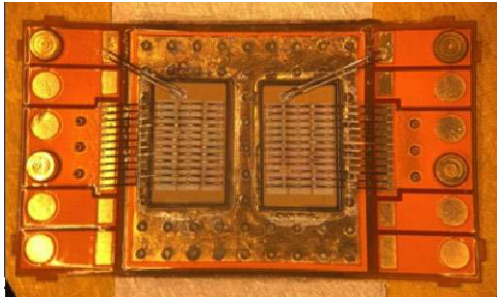
Early Stage Discrete-Die Bidirectional Switch

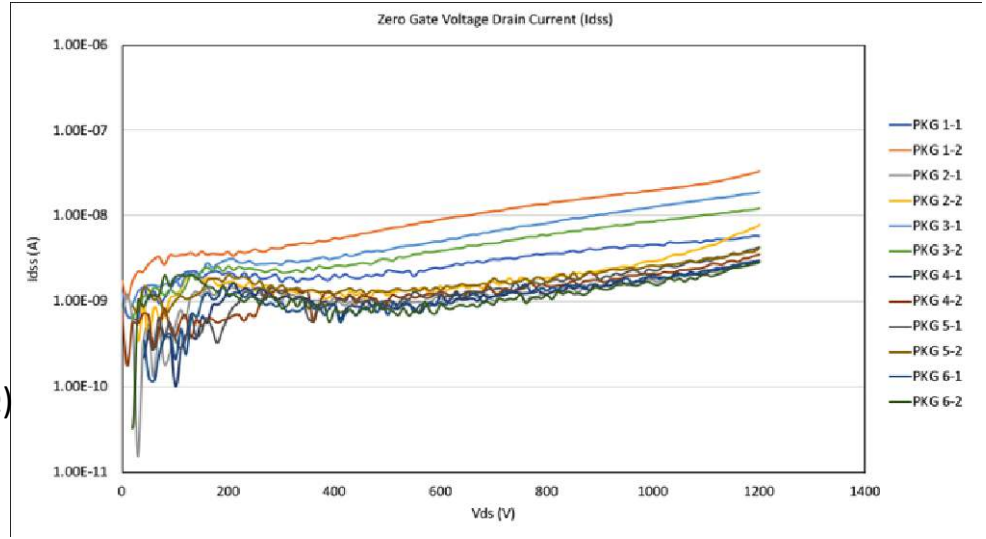
- The challenge for the packaging with the new 4-QPS is to provide *ultra-low electrical and thermal resistances in a very high-density package at low cost.*
- "Early Stage" package used two conventional MOSFETs











Electrical testing results:

- Total package resistance added 15% of R_{dson} (=25 mΩ)
- Leakage drain current (I_{dss}) were *2 uA @ V_{ds}=1200V,* under the typ. value of the datasheet

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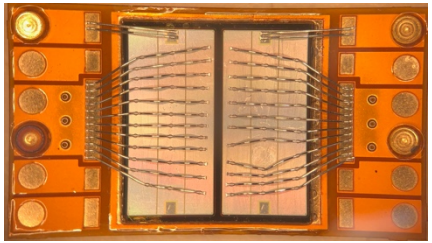
Discrete 1.2kV/10A Monolithic BiDFET Packages

Discrete 1.2kV/10A BiDFET packages:

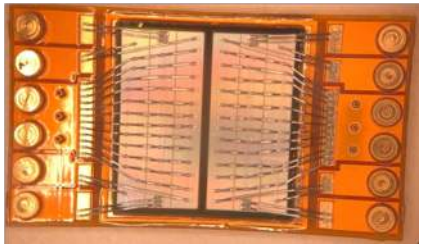
- 4-terminal PKG
- 12-terminal PKG

Interconnection:

- Two 5-mil Al wires for G1, G2, KS1, KS2
- Twelve 5-mil Al wires for T1 and T2



4-terminal PKG



12-terminal PKG

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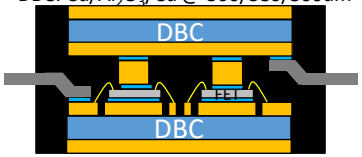
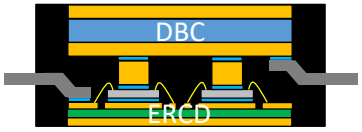
ERCD vs DBC Performance

Thermal-mechanical reliability comparison: Only ”dual ERCD” and “ERCD/DBC” can pass the failure criteria for SAC305 and SiC device.

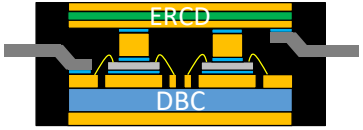
DBC: Cu/Al_2O_3/Cu @ 300/380/300um



Dual DBC

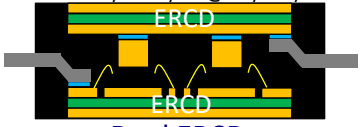


Top/Bottom: DBC/ERCD



Top/Bottom: ERCD/DBC

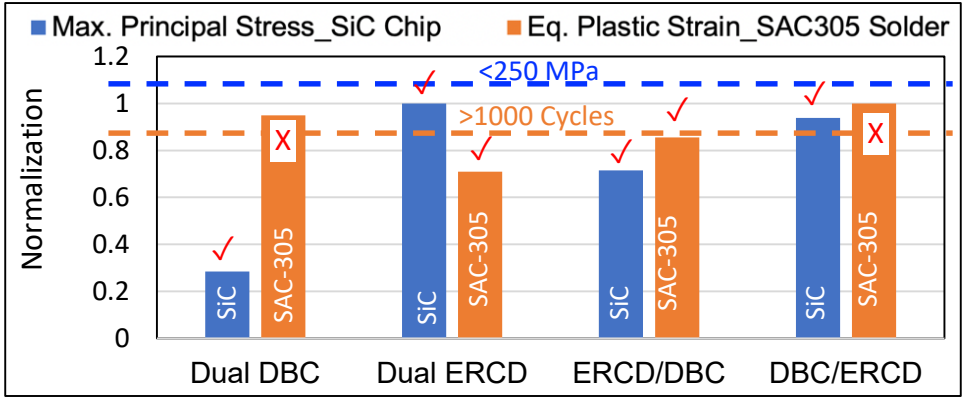
ERCD: Cu/ERCD/Cu @ 70/120/70



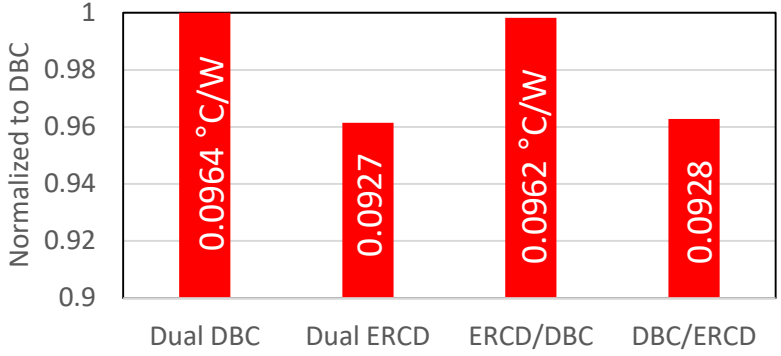
Dual ERCD

The “trigger” is Organic Dielectric with ≥8W/mK @ 120µm thick. This is better than 380µm (15mil) Al_2O_3 in thermal performance.

[Al_2O_3 Ribbon ceramic at 36W/mK @ 120µm thickness surpasses AlN]



(Simulated) Thermal Resist. junction-to-case



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Short-circuit Ruggedness Improvement

To increase short circuit capability, a low voltage Si enhancement mode MOSFET (EMM) connected with the BiDFET source. Due to the lower saturation current of the EMM compared with the BiDFET, the peak short-circuit current can be reduced in the latter under fault conditions, consequently increasing the t_{SC} (duration under short circuit condition). The gate bias of the EMM can be varied to obtain the desired saturation current [1].

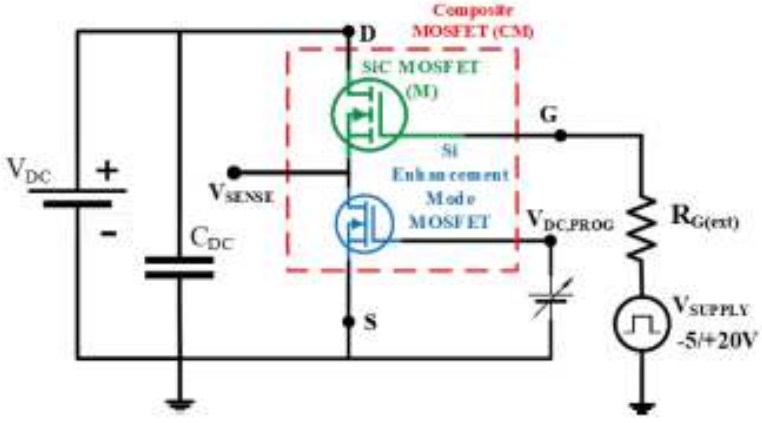

Fig. 2. Schematic for the short-circuit characterization test for the BaSIC(EMM) topology for a 1.2-kV SiC power MOSFET.

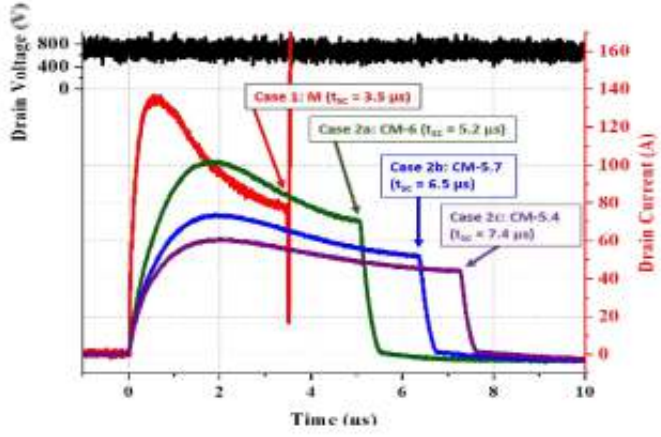

Fig. 4. Measured short-circuit test waveforms for the standalone SiC power MOSFET and BaSIC(EMM) topology.

[1] "A New User-Configurable Method to Improve Short-Circuit Ruggedness of 1.2-kV SiC Power MOSFETs," Ajit Kanale, and B. Jayant Baliga, IEEE Trans. on Power Elect., Vol. 36, No. 2, February 2021. DOI: 10.1109/TPEL.2020.3010154.

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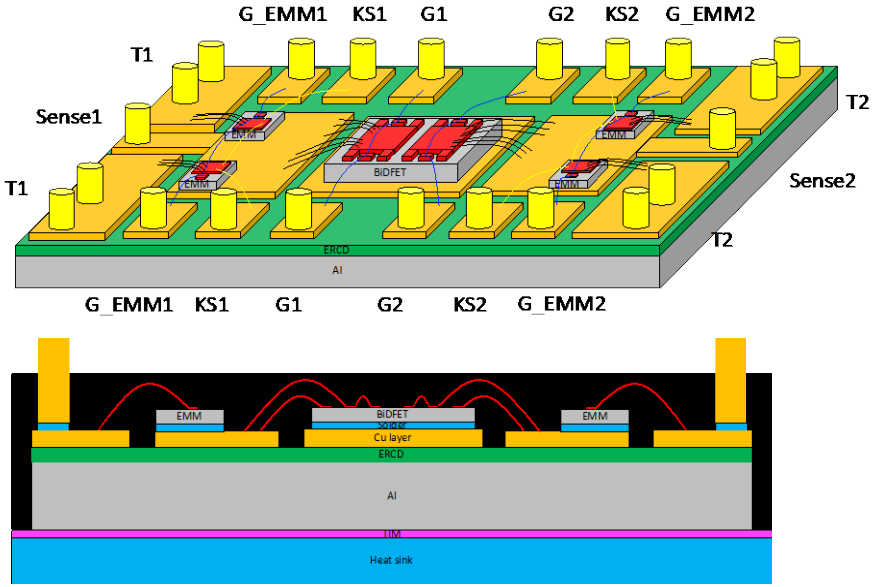
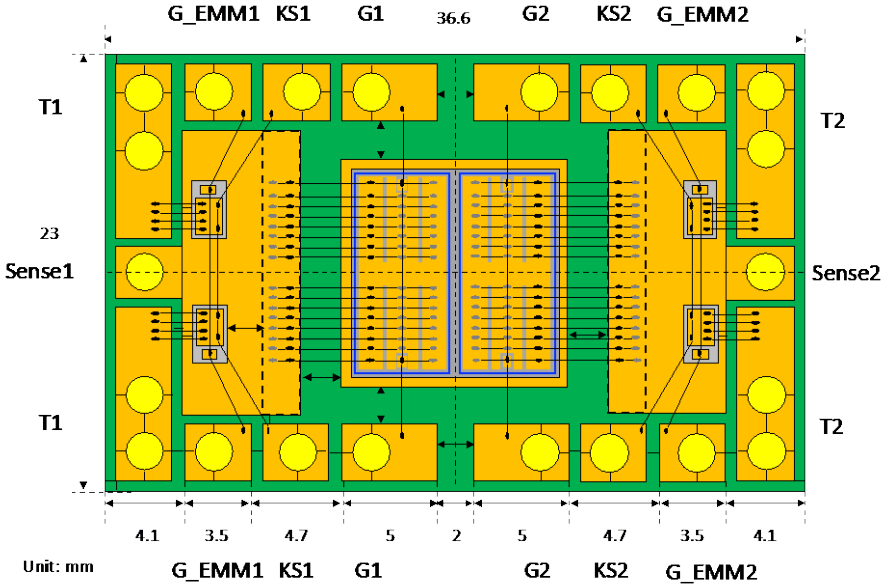
Package-Integrated BaSIC Topology for BiDFETs & Intro eIMS-Al

- An integrated EMM 1.2kV/10A BiDFET module was devised to improve BiDFET short circuit capability.
- Two paralleled EMMs were used to reduce series resistance.
- To achieve ultra-low resistance, two rows of 8-mil heavy Al wires were applied to each JBSFET.

Applying the BaSIC Topology to thee BiDFET





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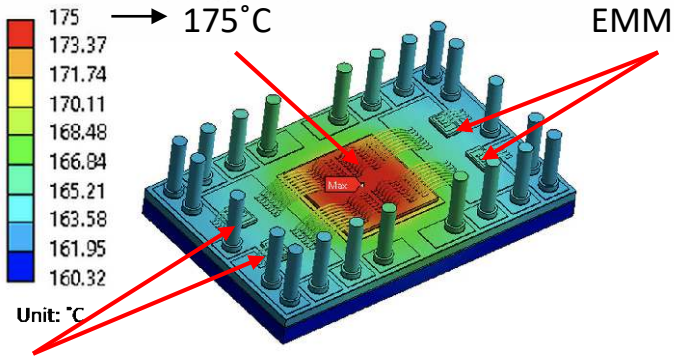
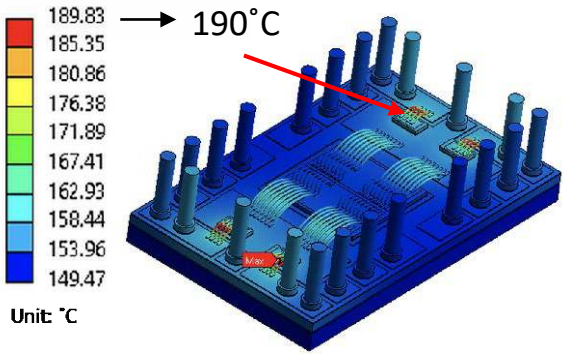
Assessment of Continuous Current Capability



(a) Chip limitation: 19.5 A



(b) Package limitation: 119.1 A

Component	Material	Max. operating temperature (˚C)
Heat slug	Cu	>300
Conductor Layer		
Pin		
Wire	Al	>600
Encapsulant	Epoxy resin and hardener	>190
Solder	Sn95Sb5	>200
BiDFET	SiC	175
EMM	Si	175
Dielectric	ERCD	300

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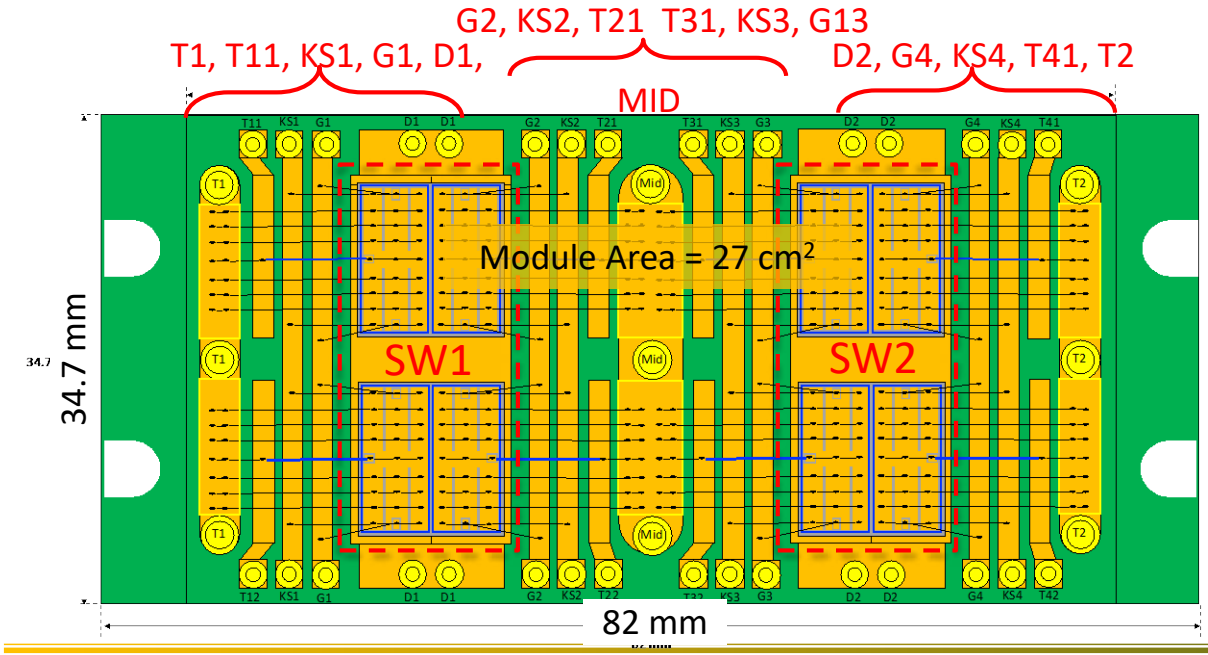
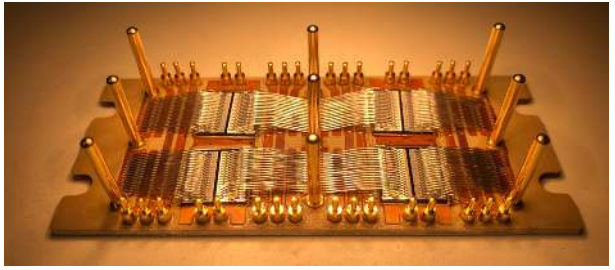
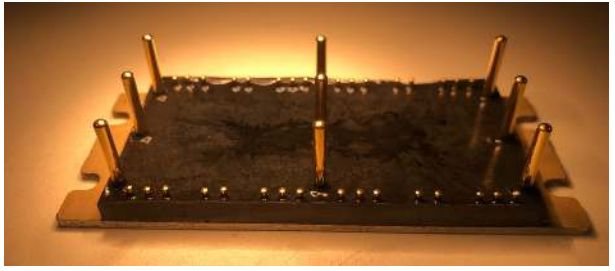
Single-Side Cooled (SSC) Parallel-BiDFET Half-Bridge Module

- For increased current rating of a half-bridge, TWO BiDFETs are connected in parallel per switch (SW) and TWO switches are connected in series for a half-bridge.
- To minimize the parasitic resistance and inductance in the power loop, 20-mil stitched Al wires are bonded on each JBSFET. The SMD signal pins and THD power pins assist alignment for mounting module on PCB.







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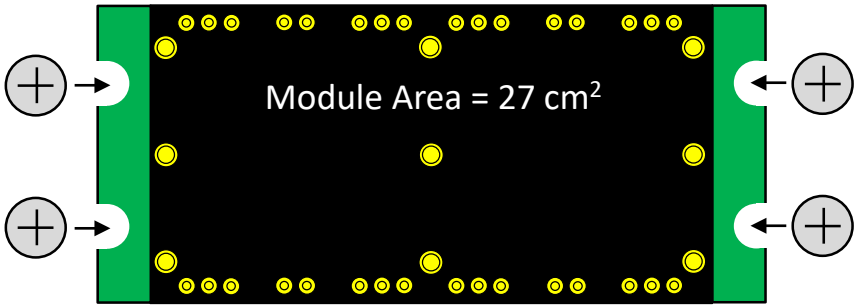
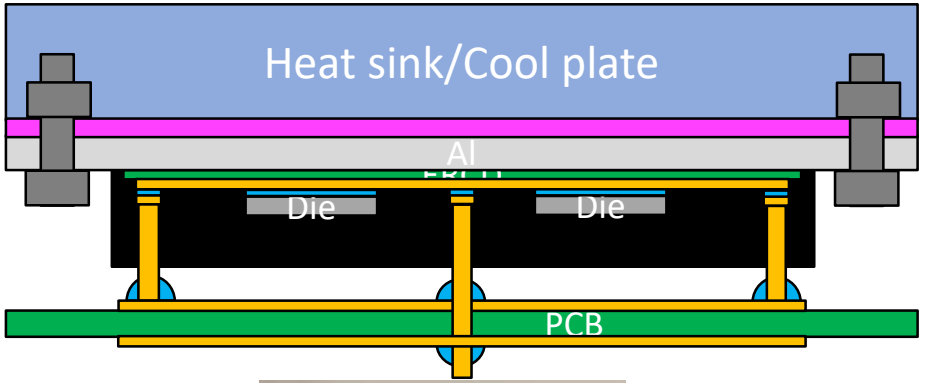
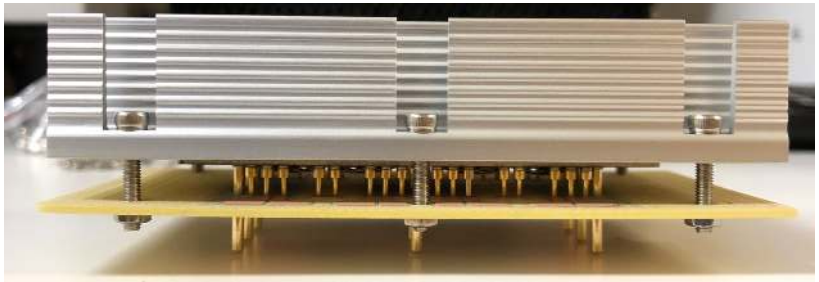
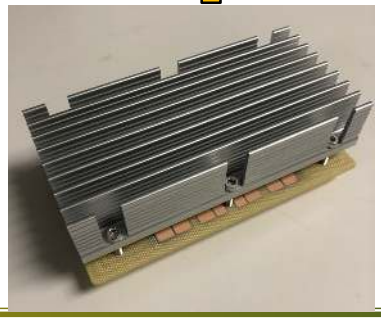
Single-Side Cooled (SSC) Parallel BiDFET Half-Bridge Module

Four side holes on the eIMS provide heat sink/cool plate mounting & provides the convenience for paralleling multiple modules or building a three-phase inverter.









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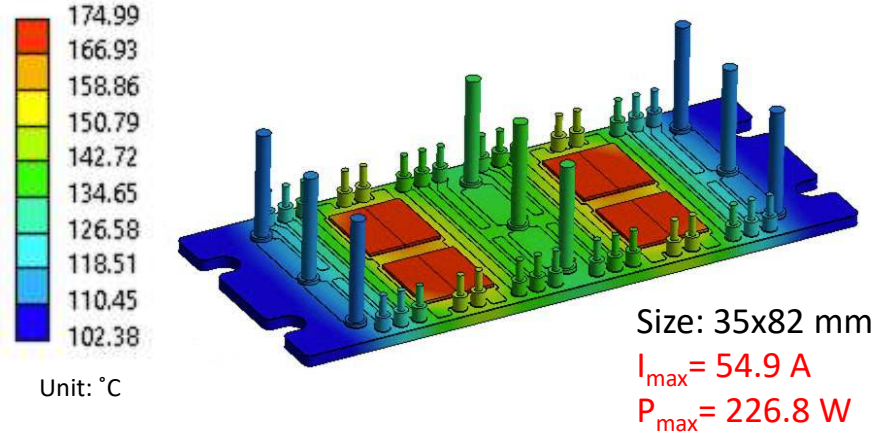
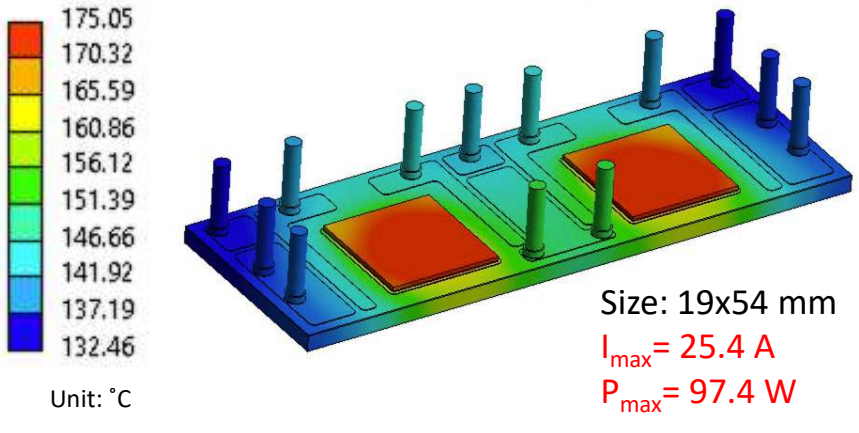
Thermal Simulation for eIMS & Parallel 1.2kV/10A BiDFET

- To simplify the simulation, an equivalent heat convective coefficient, *h_eff*, was applied to the bottom of the eIMS. The *h_eff*, obtained by experiment, 750 W/m^{2}K.
- The max. current was deduced from the $R_{ds\text{-}on}$, $R_{\theta\text{-}jc}$, max. T_j, and T_a. In addition, max. power was deduced from $R_{\theta\text{-}jc}$, max. T_j, and T_a.
- Results show the max. current and max. power comparison of single- and parallel-die half-bridge modules at *h_eff=750 W/m^{2}K* and T_a=25˚C.





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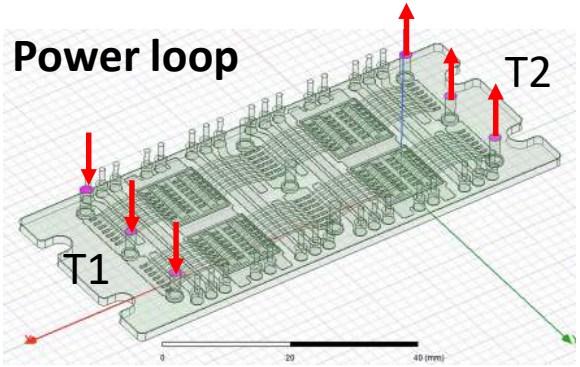
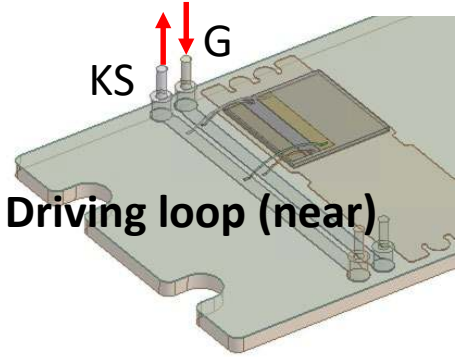
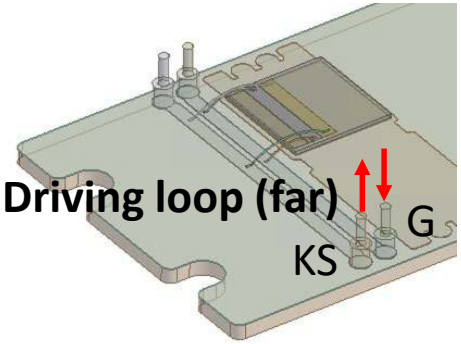
Parasitic Extraction Analysis

- This study conducted parasitics extraction analysis, including the resistance and inductance under DC and 1 MHz matching BiDFET turn-on and turn-off speed.
- To consider that users may only connect one side of the signal pins which lead to a longer driving loop for one of the BiDFETs in a SW, this study extracted both near and far driving loop, as shown below.







	Power loop	Driving loop (near)	Driving loop (far)
DC Resistance (mΩ)	0.49	7.19	10.46
AC Resistance @ 1MHz (mΩ)	2.22	7.30	14.49
AC Inductance @ 1MHz (nH)	22.36	5.62	7.82

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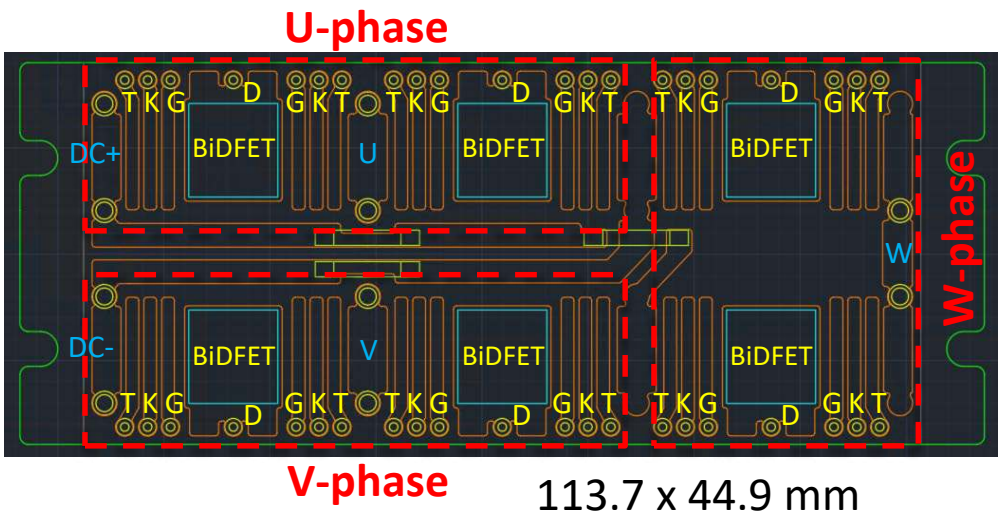
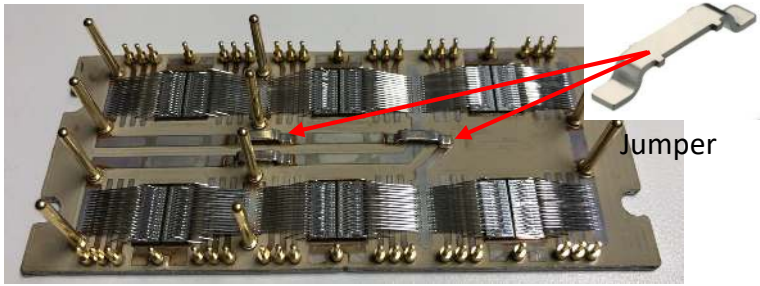
Single-Die, Three-Phase Module

- To increase power density and reduce inductance, SIX 1.2kV/50mΩ BiDFETs formed a 3Ø module.
- Temperature sense pins (T) were added.
- To minimize power loop R&L, multiple Al bond wires and jumpers were adopted.
- The SMD signal pins and THD power pins assist alignment for mounting the module on PCB.



113.7 x 44.9 mm



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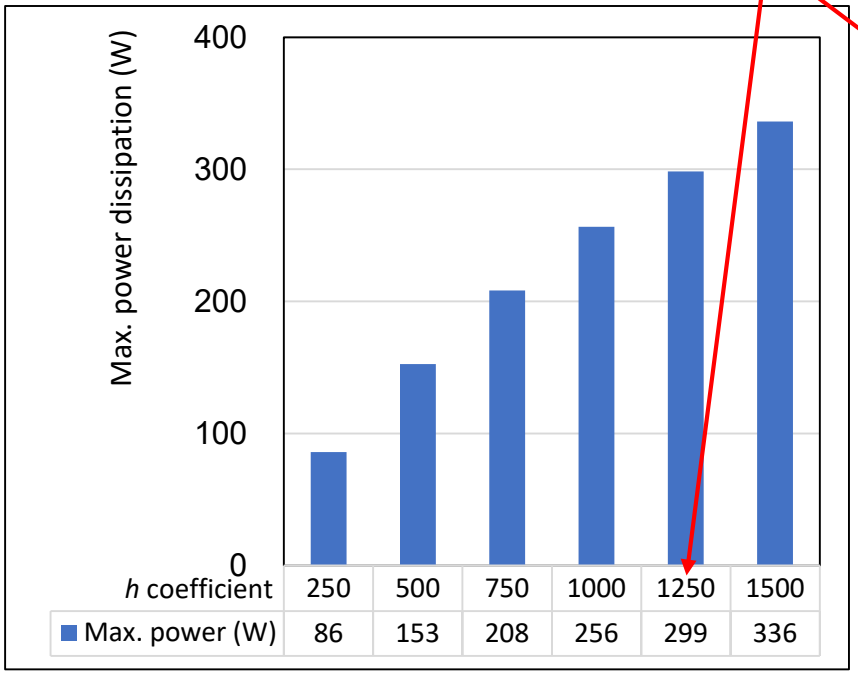
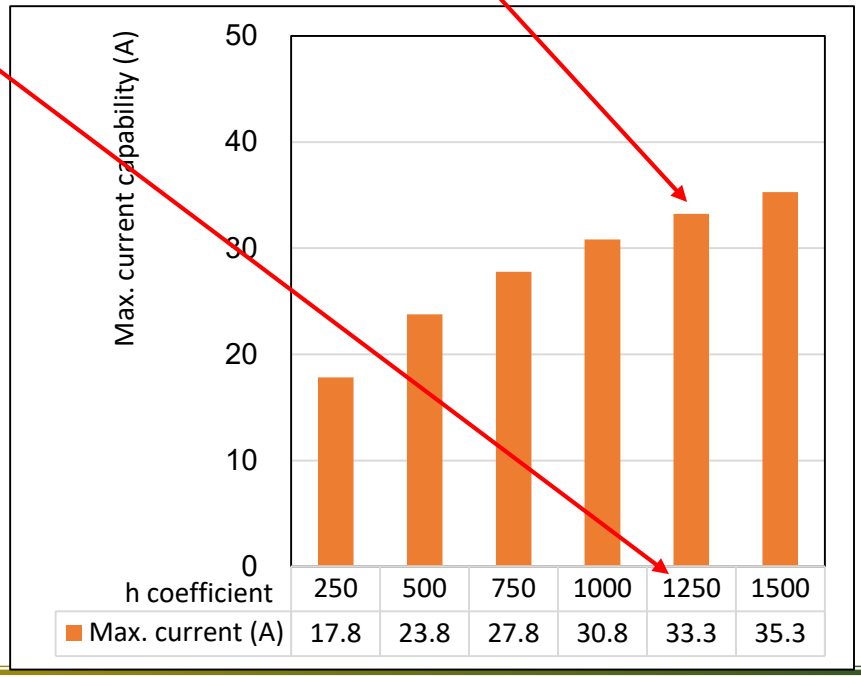
Steady-State Thermal-Electric Simulation (High $T_{ambient}$)

$T_{j,max}$ = 150°C, $T_{ambient}$ = 70°C,
Selected design point h_{eff} = 1250 W/m²K allows BiDFET to operate at 33A





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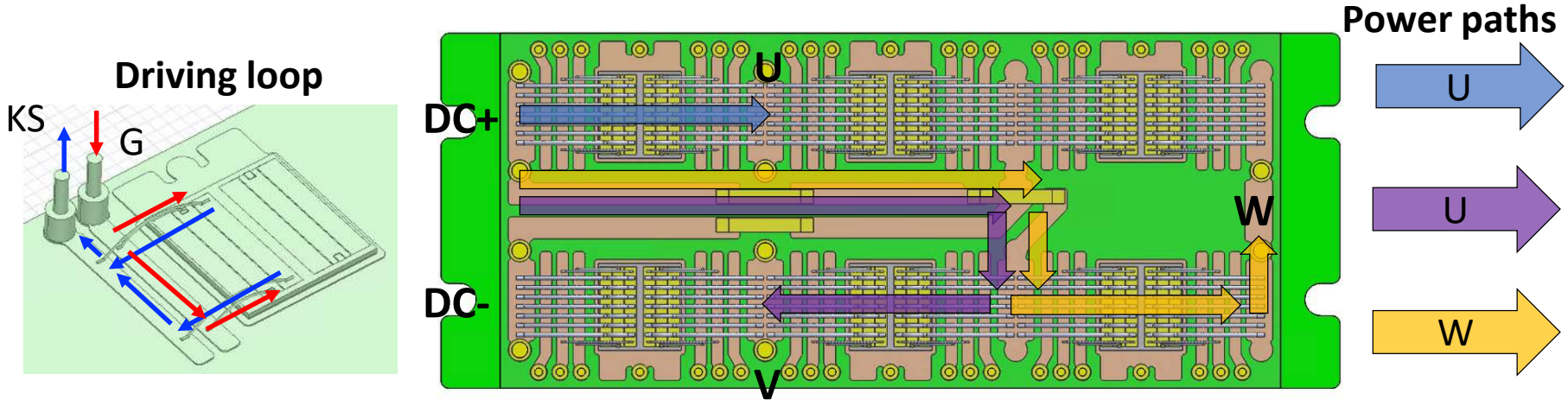
Parasitic Extraction Analysis

- Module design focuses on minimizing point-to-point inductance within its housing.
- Extracted are the DC resistance and AC inductance of the driving and power paths at 1 MHz, which is representative of the BiDFET turn-on and turn-off speed.



	Driving loop (near)	Power path_U	Power path_V	Power path_W
DC Resistance (mΩ)	7.19	0.55	4.61	4.79
AC Inductance @ 1MHz (nH)	5.62	10.68	20.35	46.98

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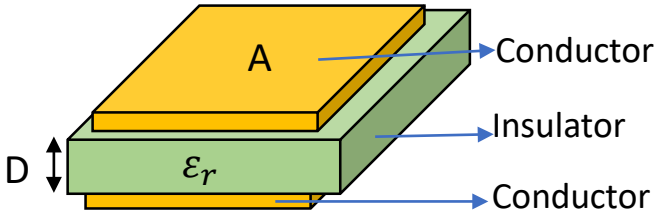
Interstitial (shielding) Layer Development in Ultra-Thin Dielectrics

Parasitic capacitance

$$C = \varepsilon_0 \times \varepsilon_r \times \frac{A}{D}$$

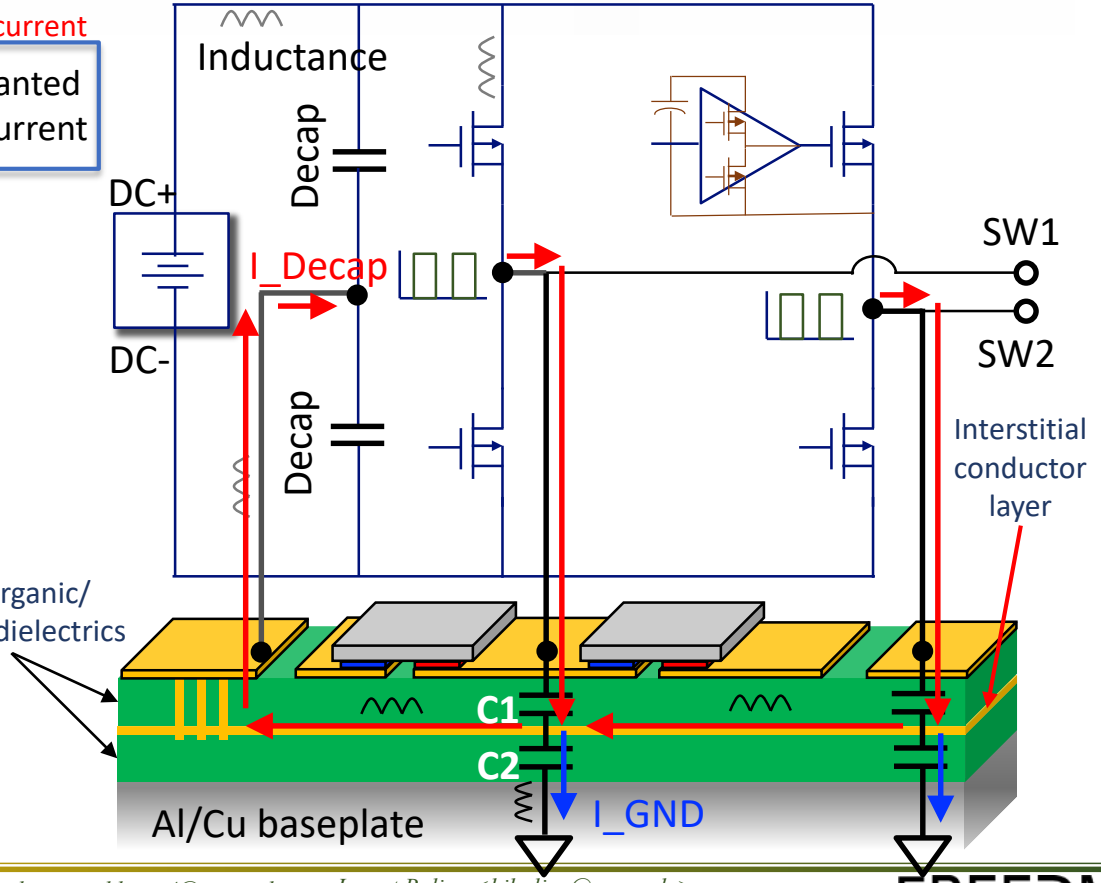
CM: Common-Mode current

$$\Delta I = C \times \frac{dv}{dt}$$ Unwanted CM current



ε_0 : permittivity of vacuum (8.854×10^{-12} F/m)
ε_r : relative dielectric constant of medium
A: overlapping area of conductors
D: insulator thickness

Solutions Of Baseplate Current Reduction
Select low ε_r material, increase D, and decrease A, add external filters, add Interstitial conductor layer



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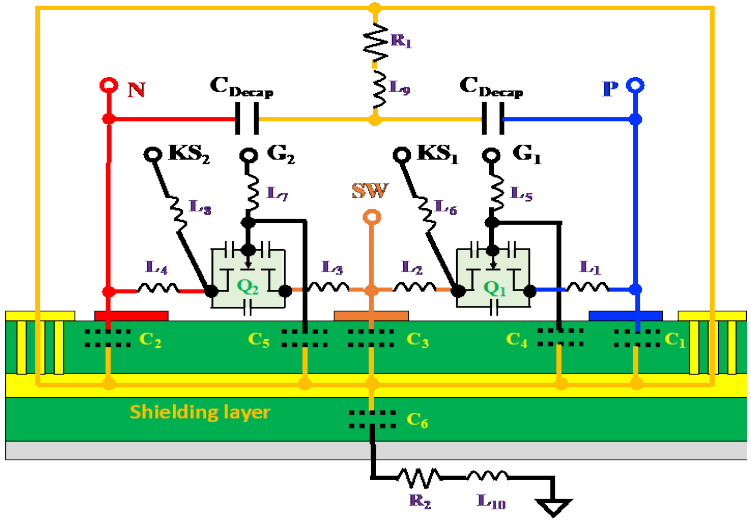
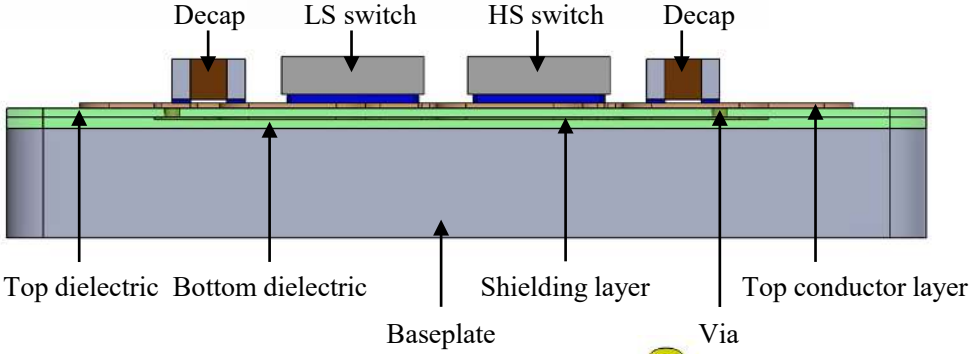
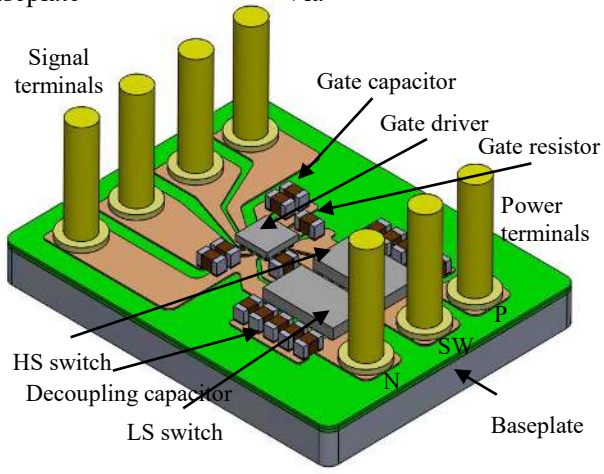
Implementation of a Shielding Layer (On-Going Research)







- Two power devices, a half-bridge gate driver and ten 0402 MLCC decoupling capacitors are mounted on the top conductor layer.
- In a multi-layer IMS, an interstitial conductor layer (or shielding layer) is laminated by 120-um ERCD dielectrics on the top and bottom.
- Shielding layer uses through-hole vias to the top conductor and covers the top conductor pads with a minimal area for minimal capacitance.

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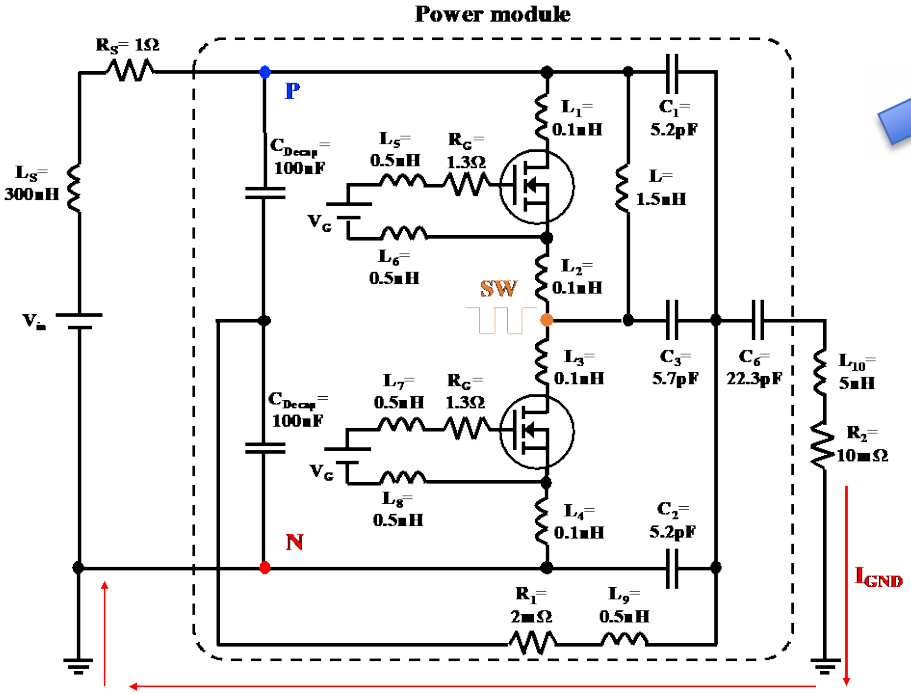
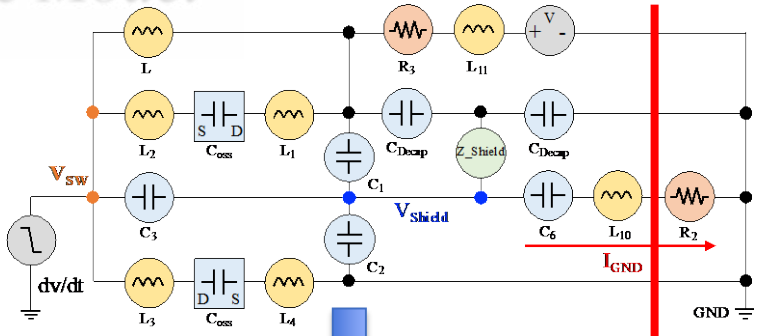
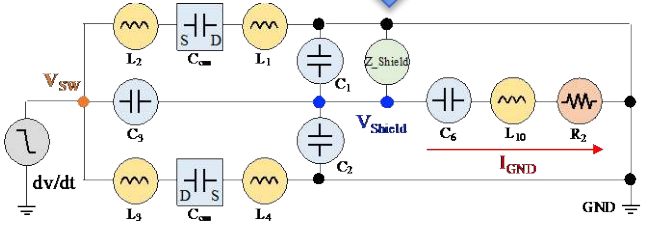
Simplification of the CM Noise Impedance Model

Since the dv/dt and ringing frequency of the SW voltage can be up to a couple of hundred MHz, the power inductor L and the decoupling capacitors C_{Decap} can be regarded as open and short, respectively.

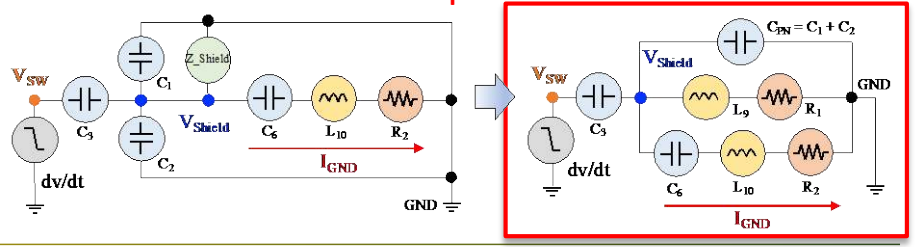


Full CM Noise Model





Simplified CM Noise Model



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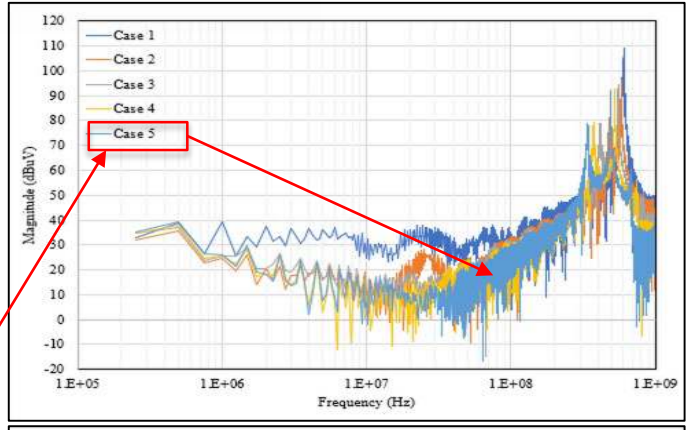
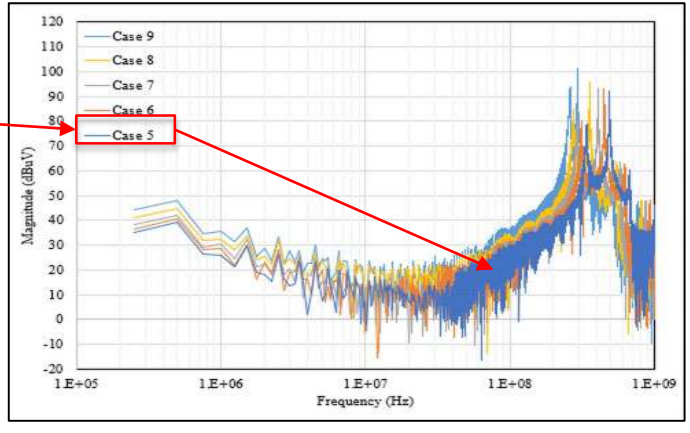
Verifying optimized z-height ratio of the thin dielectrics

It indicates that the best thickness ratio of T_1 to T_2 is one for suppressing I_{GND} or CM noise. A parametric study was carried out for validating the best thickness ratio. The highest product of C_3 and C_6 occurs at *Case 5* which holds the same T_1 and T_2.

Case	T1 (um)	T2 (um)	C3 (pF)	C6 (pF)	C3×C6 (pF^2)
1	40	200	10.1	17.1	173.4
2	60	180	11.3	11.4	128.4
3	80	160	12.7	8.6	108.4
4	100	140	14.5	6.8	99.1
5	120	120	16.9	5.7	96.3
6	140	100	20.3	4.9	99.1
7	160	80	25.4	4.3	108.4
8	180	60	33.8	3.8	128.4
9	200	40	50.7	3.4	173.4





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THANK YOU

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Publications

- A. Kanale, T-H. Cheng, S. S. Shah, K. Han, A. Agarwal, B. J. Baliga, D. Hopkins and S. Bhattacharya, “Switching Characteristics of a 1.2 kV, 50 mΩ SiC Monolithic Bidirectional Field Effect Transistor (BiDFET) with Integrated JBS Diodes”, lecture presentation at the APEC 2021 Virtual Conference.
- Suyash Sushilkumar Shah, Ramandeep Narwal, Subhashish Bhattacharya, Ajit Kanale, Tzu-Hsuan Cheng, Utkarsh Mehrotra, Aditi Agarwal, B. Jayant Baliga and Douglas C. Hopkins, “Optimized AC/DC Dual Active Bridge Converter using Monolithic SiC Bidirectional FET (BiDFET) for Solar PV Applications”, accepted for lecture presentation at the ECCE 2021 Conference.
- Ajit Kanale, Tzu-Hsuan Cheng, Aditi Agarwal, Suyash Sushilkumar Shah, B. Jayant Baliga, Subhashish Bhattacharya and Douglas C. Hopkins, “Comparison of the Capacitance and Switching Losses of 1.2 kV Common-Source and Common-Drain Bidirectional Switch Topologies”, to be presented at WiPDA 2021.