

Modular Solid-State Transformers Using 3.3kV SiC Devices

Professor: Dr. Wensong Yu, wyu2@ncsu.edu Ph.D. Students: Pranit Pawar, Tohfa Haque, Md Tanvir Ahammed North Carolina State University April 02, 2024

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Technical Approach Modular Universal SST: Single-stage AC-AC SST or DC-DC SST

- Power semiconductors: 3.3 kV SiC MOSFET
- Advanced duo-loop digital control
- Ultra-high efficiency (99%) and high frequency (>50 kHz) isolation
- Soft-switching operation with source voltage and load current adaptability

Objectives

- To achieve 99% efficiency with single-stage AC-AC SST at rated (2400Vac-480Vac) voltage and DC-DC SST at rated 4200Vdc-400Vdc
- To explore the feasibility and scalability for such technology at 66 kVac and 10 MVA levels





Building Blocks to be connected in series or parallel





Electrical Design Progress

Why High-Voltage SiC with Soft-Switching ?

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3300V SiC FET Is Very Reliable

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3300V SiC FET Operating at 210 kHz

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□ Validated high frequency (210 kHz) operating of 3.3 kV SiC MOSFETs with cost-effective discrete TO247 package 210 kHz / 4.76 µs Transformer 6 kV current at HV-side 23 A (10 A/div C4) 2 kV Transformer 1 kV voltage at 4000 V HV-side (1 kV/div)

Time (1 µs/div)

2 µs

3 115

-1 µs

-3 15

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FREENS SIMULATION OF MODULATOR with Two-Input Variables: SYSTEMS CENTER Independent Period and Phase

0.8

Structure of independent period and phase modulation







Modulator dynamic response to period and phase step changes

Ts Step change of period input

12	_	 	
10			
10			
Q			
0			
6			
0			

Phase Step change of phase input

0 1			
0.4			
0.2			
0			

G1 Dynamic response of modulator output G1



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Simulation of Converter (Power Stage + Modulator)





Converter dynamic response to 2-input step changes



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Looking Inside: Local Power Supply with 200-2100V Input SYSTEMS CENTER

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4.2kV

Local Power Supply (no need of external PSU – "self powered") (0.5*2.1) kV Min working iso DC-link midpoint as reference halves the isolation requirement DC+ 2.1kV DC-2.1kV 25L Flyback Fiber Optic TxRx 3.3kV SiC half-bridge Gate Drv 1 PWM___/ 和L SK1 Gate Drv 2 SW Confidential FLT SK2 Local isolated gate driver local isolated power supply Low Voltage PGND High Voltage and local heatsinks 100kV (0.5*2.1) kV **Optical iso from Fiber** Min working iso

Fiber Optic for bidirectional communication (provides control-to-power 100 kV isolation) **NC STATE**

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Hardware of Local Power Supply (200-2100V Input)

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FREE Testing of Local Power Supply (200-2100V Input)

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File Edit Utility Help			
Waveform View	VDC:1kV Load: 8	30% (9.6W, 150hm)	Add New
			80 mV 60 mV
VOUT-GNDFB			40 mV Measure Sear
	Manual International Account of the	the second s	Table Pic
	d pr		-40 mV
Output voltage 20//17/01/			-60 mV -80 mV Meas 1
0,5 40 µs	80 µs 120 µs 160 µs	Observation:	320 µs Mean µ': -4.471 mV
		too much DCIVI, room for Inductor (Doumization 2.5 kV Meas 2 Peak-to-Peak
SW-DC- 500V/dlv			2 kV µ': 56.18 mV 1.5 kV
Mann www.	mil Manual Man	m/ www.m/ www.m/w	Maximum Maximum
C2		····U·································	0V Meas 5
			-1 kV . µ' 59.66 V
			• Meas 6 120 V Maximum
00)////			100 V µ° 714.0 mA an V Meas 7
SR FET 20V/dIV	h h	ь ь ь	60 ν Mean μ°: 4.991 mA
LAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA	AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA	AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA	AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
			-20 V
			-40 V
			1.2 A
200mA/div			Am 0001 Am 008
Ipri			600 mA
ipit ipit	A TABLE A A A A		200 mA
- ana and a same the same same	man and a second and a second		1919-200 mA
s a s la s as s la So	tar, no failure observed du	e to proposed design	-400 mA
Ch 1 Ch 2 Ch 3 Ch 4 20 mV/div 500 V/div 20 V/div 200 mA/div	Achieved 50% of intended	operating voltage	Trigger Acquisition Stoppe
50 Ω 1 MΩ 1 MΩ 1 MΩ 200 MHz ^B 350 MHz 350 MHz 120 MHz ^B	Further testing und	Ier way SR: 3.125 GS RL: 1.25 Mpt	/s 320 ps/pt Sample: 12 bits 19 Feb 20 s ♥ 10% 44 Acgs 12:55:47



Mechanical Design Progress: From Single Block To System Level

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Cost-Effective 3D Packaging of Single Block with Discrete 3300V SiC Devices



□ Low cost discrete 3300V SiC MOSFETs with sealed air cooling

□ High performance Aluminum Nitride (AIN) thermal interface

- Very high voltage isolation
- Very low thermal resistance

Optimized rubber buffer assembly

□ Minimum commutation loop inductance



Reference: Wensong Yu, Dakai Wang, and Srdjan Lukic, "High Voltage Isolation Using Discrete Non-Isolated Devices And Electrically Isolating, Thermally Conductive Substrate" U.S. Patent Application #: US20220385081A1.

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3D Packaging of Single Building Block



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Modular SST 3D Conceptual Design: From Single Block To System Level

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• Flexible interconnect enables efficient usage of available space

- Electric terminals connected in parallel or in series along XYZ
- Cooling channels connected in parallel (Preferred) or in series
- Fiber optics connected in parallel or in chain structure





□ Major Accomplishments

- Fiber controlled 3.3kV SiC MOSFETs with self-power enables modular SST with scalability up to 66 kVac
- Modulation method with 2-independent-input was simulated for proposed AC-AC SST and DC-DC SST
- Discrete 3.3kV SiC MOSFETs with the patented structure simplifies the SST building block design
- Sealed cooling channels are pre-defined to ensure cooling performance and contamination free

Given Future Work

- To finalize conceptual 3D design
- Hardware and software development of modular DC-DC or AC-AC SST
- Possible innovative design of the transformers with ultra-high partial discharge inception voltage

Any Comments, Suggestions, or Questions?

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