Power Conversion Systems enabled by SiC-based Monolithic Bidirectional FET (BiDFET)

Subhashish Bhattacharya

Prof. Jay Baliga – SiC BiDFET device
Prof. Doug Hopkins – Advanced packaging of SiC BiDFET device

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Four Quadrant Switch (FQS): The Ideal Power Device (The Holy Grail)

**Ideal Device Characteristics:**
- Large Forward & Reverse Blocking Capability
- Bi-directional current flow
- Zero On-State Voltage Drop
- Fast Switching Capability
- Gate Voltage Controlled Output Characteristics
- Excellent Safe-Operating-Area

**ASD needs Energy Storage Element:**
- DC link capacitor as energy storage element
- Bulky
- Expensive
- Poor Reliability
- Degraded performance under high temperature
- Single point failure

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Four Quadrant Switch (FQS) Enabled Direct AC-AC Matrix or Cyclo Converter

- Direct AC-AC Matrix or Cyclo Converter creates a variable output voltage with unrestricted frequency using an array of fully controlled four-quadrant bidirectional switches.
- Does not need large energy storage element and DC-Link.
- “Unfortunately, there were no such devices available” and “Consequently, multiple discrete devices had to be used to construct suitable switch cell” [P.W. Wheeler, et al, “Matrix Converters: A Technology Review”, IEEE Trans. Industrial Electronics, vol. 49, no. 2, pp. 276–288, April 2002.]
- CSI have traditionally used Thyristor family reverse voltage blocking (RB) switches [e.g. Thyristors, SGTO Thyristors, Symmetric IGCTs] – however, Thyristor family RB switches typically have low switching frequency.
- WBG based SiC MOSFET with series connected SiC JBS [Junction Barrier Schottky] diode provides a RB switch with increased switching frequency for CSI – however, will have higher conduction voltage drop compared to single MOSFETs or IGBTs.
- SiC BiDFET as a monolithic devices offers advantage of lower conduction voltage drop and higher switching frequency for CSI and Direct AC-AC Matrix or Cyclo Converter based power conversion systems.

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**Fig. 1.** Simplified circuit of a 3 × 3 matrix converter.

CSI with Bi-Directional [RB] Switches
Monolithic SiC-based Bidirectional FET (BiDFET) Switch: 1200V, 20A DIE

Monolithic BiDFET Cross-section

4-terminal Monolithic BiDFET Circuit Schematic

Fabricated BiDFET Die:

Custom-Made 4-Terminal Package for the BiDFET:

Comparison of Fabricated 1.2 kV 20 A BiDFET with Previous Bidirectional Switch Implementations:

<table>
<thead>
<tr>
<th>Switch Configuration</th>
<th>Description</th>
<th>Number of Components</th>
<th>On-State Voltage Drop (V)</th>
<th>Switching Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode Bridge + Asymmetric IGBT</td>
<td>5</td>
<td>8.6 [2 diodes + 1 IGBT]</td>
<td>High</td>
<td></td>
</tr>
<tr>
<td>Asymmetric IGBTs + Free-wheeling diodes</td>
<td>4</td>
<td>5.8 [1 diode + 1 IGBT]</td>
<td>High</td>
<td></td>
</tr>
<tr>
<td>Back-to-back symmetric IGBTs</td>
<td>2</td>
<td>2.2 [1 symmetric IGBT]</td>
<td>Very High</td>
<td></td>
</tr>
<tr>
<td>SiC Power MOSFETs + JBS diodes</td>
<td>4</td>
<td>3.1 [1 diode + 1 MOSFET]</td>
<td>Low</td>
<td></td>
</tr>
<tr>
<td>Back-to-back SiC Power MOSFETs + antiparallel and series JBS diodes</td>
<td>6</td>
<td>3.1 [1 diode + 1 MOSFET]</td>
<td>Low</td>
<td></td>
</tr>
<tr>
<td>Four-terminal SiC Monolithic BiDFET</td>
<td>1</td>
<td>1.0 [1 BiDFET]</td>
<td>Low</td>
<td></td>
</tr>
</tbody>
</table>
Gen-1 SiC BiDFET: Chip Design

Objective 1:
- Rated Blocking Voltage = 1.2 kV
- Breakdown Voltage > 1.4 kV
- Use Hybrid JTE Edge Termination BV > 1.6 kV

Objective 2:
- On-Resistance of BiDFET = 50 mΩ
- Each JBSFET On-Resistance = 25 mΩ
- Use JBSFET Active Area = 0.45 cm²

Objective 3:
- Low Internal Gate Resistance < 1 Ω
- Use Gate Runners

Objective 4:
- Improved Packaging and Board Interconnect
- Use Two Gate Bonding Pads per JBSFET
SiC BiDFET Gen-1: Single Chip

Internal JBSFET cross-section

- Fabricated BiDFET die

- Custom-designed 4-terminal package for the BiDFET

Module Area = 3.22 cm²

- BiDFET blocking characteristics
  - Blocking Voltage > 1400 V
  - On-Resistance = 50 mΩ
  - First Pass Success
  - Used to demonstrate 1f 2.3 kW converter
  - Ciss = 11,000 pF
  - Coss = 500 pF at 1000 V
  - Crss = 50 pF at 1000 V
SiC BiDFET Gen-1: Parallel Chips

Objective: Demonstrate Reduced On-Resistance BiDFET by Paralleling Two Chips for 3φ Converter Application

- Turn-on and Turn-off like a single Gen-1 BiDFET chip
- Switching Losses (800 V, 20 A):
  - $E_{\text{ON}} = 1350 \, \mu \text{J}$
  - $E_{\text{OFF}} = 460 \, \mu \text{J}$
  - $E_{\text{TOTAL}} = 1810 \, \mu \text{J}$
Gen-2 BiDFET: Achieve 2x Lower $R_{on}$

**Objective:**
- Rated Blocking Voltage = 1.2 kV
- Breakdown Voltage > 1.4 kV
- Device On-Resistance = 25 mΩ

**Conventional Doubling Die Size Approach:**
- Very Low Yield
- Die Size exceeds X-Fab Maximum Reticle Size
- Impossible

**Parallel Gen-1 Dies:**
- Achieved in Modules

**New Design and Process Strategy Created:**
- Separate JBS Diode from MOSFET Cells
- Reduces Cell Pitch to 2.8 μm from 6.1 μm
- Reduces Specific On-Resistance to 5.3 mΩ-cm²
- Ascribe 10 % Active Area to JBS Diode
- $R_{on}$ = 26 mΩ achievable

**Additional Objective:**
- Add Integrated Temperature Sensor
- Use Poly-Silicon Gate Electrode Resistance
- No additional processing required
SiC BiDFET Gen-2 Single Chip

Objective: Demonstrate Reduced On-Resistance BiDFET with Single Chip for 3ф Converter Application

- Turn-on and Turn-off like a single Gen-1 BiDFET chip
- Switching Losses (800 V, 20 A):
  - $E_{\text{ON}} = 1120 \, \mu\text{J}$
  - $E_{\text{OFF}} = 250 \, \mu\text{J}$
  - $E_{\text{TOTAL}} = 1370 \, \mu\text{J}$

Single Gen-2 BiDFET chip can handle 20 A ($V_{\text{ON}} = 0.5 \, \text{V}$).
SiC BiDFET Single Gen-2 Chip vs BP-1 Two Gen-1 Chips in Parallel

**Objective:** Demonstrate Reduced On-Resistance BiDFET with Single Chip for 3φ Converter Application

<table>
<thead>
<tr>
<th>Parameter, Units</th>
<th>Gen 1 (2 Chips)</th>
<th>Gen 2 (1 Chip)</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Area, cm²</td>
<td>2.28</td>
<td>1.14</td>
<td>2x</td>
</tr>
<tr>
<td>$R_{DS,ON}$, mΩ</td>
<td>25</td>
<td>27</td>
<td>-</td>
</tr>
<tr>
<td>$g_M$, S</td>
<td>15</td>
<td>15</td>
<td>-</td>
</tr>
<tr>
<td>$C_{ISS}$, pF</td>
<td>15100</td>
<td>11730</td>
<td>1.3x</td>
</tr>
<tr>
<td>$C_{OSS}$, pF</td>
<td>1050</td>
<td>600</td>
<td>1.75x</td>
</tr>
<tr>
<td>$C_{RSS}$, pF</td>
<td>70</td>
<td>70</td>
<td>-</td>
</tr>
<tr>
<td>$E_{ON}$, µJ</td>
<td>1350</td>
<td>1120</td>
<td>1.2x</td>
</tr>
<tr>
<td>$E_{OFF}$, µJ</td>
<td>460</td>
<td>250</td>
<td>1.8x</td>
</tr>
<tr>
<td>$E_{TOTAL}$, µJ</td>
<td>1810</td>
<td>1370</td>
<td>1.3x</td>
</tr>
</tbody>
</table>
BiDFET characterization

DPT results of BiDFET module with two Gen-1 dies in parallel at 800V, 100A.

Timescale: 2us/div

Timescale: 100ns/div

Toff = 130ns

Turn-OFF transition

Timescale: 100ns/div

Ton = 160ns

Turn-ON transition

Channel 1: Gate-source voltage (20 V/div)
Channel 2: DUT current (50 A/div)
Channel 3: Inductor current (50 A/div)
Channel 6: DUT voltage (500 V/div)
Channel 7: DC bus voltage (500 V/div)
BiDFET characterization

DPT results of BiDFET module with Gen-2 dies at 800V, 20A.

Channel 1: Gate-source voltage (10 V/div)
Channel 2: DUT current (20 A/div)
Channel 3: Inductor current (20 A/div)
Channel 5: Freewheeling device voltage (500 V/div)
Channel 6: DUT voltage (500 V/div)
Channel 7: DC bus voltage (500 V/div)
Dynamic characterization of BiDFET modules at 400V and 800V operation.
2.3 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFET

Hardware prototype of the AC/DC DAB converter for 400 V DC input and 120V/240V/277V AC output.

- Full load operation at 400 V input, 277 V RMS AC output at 2.3 kW power.
- Total harmonic distortion in grid-side current: 4.7%
- Power factor: 0.9998
2.1 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFET

- Full load operation at 400V input, 240V RMS output at 2.1 kW
- Total harmonic distortion in grid-side current: 4.8%
- Power factor: 0.9998

Hardware prototype of the AC/DC DAB converter
2.1 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFET

Power factor and current total harmonic distortion at 100% load at 240 V AC voltage.

- Measurement using Hioki Power Analyzer PW6001.
- Current sensors: 50 A, 2 MHz.
- Voltage potentiometers: 1000 V.
2.1 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFET

Hardware prototype of the AC/DC DAB converter

Overall efficiency, semiconductor efficiency and estimated loss distribution at different rates of PV generation.

- Semiconductor efficiency indicates losses in the semiconductors estimated after segregating the transformer, inductor and filter losses.
- Efficiency can be improved by improving transformer design and reducing switching frequency for reduced turn-off losses.
The designed Half-Bridge Module contains two BiDFETs in Parallel per switch to enhance current and power handling capability.

The package is designed symmetrically to allow for easy installation in the converter.
SiC Bi-Directional FET (BiDFET) packaging: 1200V, 50A half-bridge module

Half-bridge module experimental thermal characterization testbench.

### Experimental thermal characterization testdata.

<table>
<thead>
<tr>
<th>I (A)</th>
<th>V1 (V)</th>
<th>V2 (V)</th>
<th>Ron_1 (mΩ)</th>
<th>Ron_2 (mΩ)</th>
<th>P1 (W)</th>
<th>P2 (W)</th>
<th>P_total (W)</th>
<th>Tc (˚C)</th>
<th>Tj_1 (˚C)</th>
<th>Tj_2 (˚C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>0.49</td>
<td>0.49</td>
<td>22.2</td>
<td>22.3</td>
<td>10.8</td>
<td>10.8</td>
<td>21.6</td>
<td>31.5</td>
<td>37.9</td>
<td>39.2</td>
</tr>
<tr>
<td>27</td>
<td>0.61</td>
<td>0.61</td>
<td>22.5</td>
<td>22.7</td>
<td>16.4</td>
<td>16.5</td>
<td>32.9</td>
<td>35.5</td>
<td>42.1</td>
<td>44.3</td>
</tr>
<tr>
<td>30</td>
<td>0.69</td>
<td>0.69</td>
<td>22.8</td>
<td>23.1</td>
<td>20.6</td>
<td>20.8</td>
<td>41.3</td>
<td>39</td>
<td>46.7</td>
<td>50.0</td>
</tr>
<tr>
<td>33</td>
<td>0.77</td>
<td>0.78</td>
<td>23.1</td>
<td>23.5</td>
<td>25.4</td>
<td>25.7</td>
<td>51.1</td>
<td>43</td>
<td>51.1</td>
<td>55.7</td>
</tr>
<tr>
<td>36</td>
<td>0.85</td>
<td>0.86</td>
<td>23.5</td>
<td>23.9</td>
<td>30.5</td>
<td>31.0</td>
<td>61.5</td>
<td>48</td>
<td>56.5</td>
<td>62.2</td>
</tr>
<tr>
<td>39</td>
<td>0.93</td>
<td>0.95</td>
<td>23.9</td>
<td>24.4</td>
<td>36.2</td>
<td>37.0</td>
<td>73.1</td>
<td>52.5</td>
<td>61.7</td>
<td>68.6</td>
</tr>
<tr>
<td>42</td>
<td>1.03</td>
<td>1.06</td>
<td>24.6</td>
<td>25.3</td>
<td>43.2</td>
<td>44.5</td>
<td>87.7</td>
<td>60</td>
<td>71.3</td>
<td>80.4</td>
</tr>
<tr>
<td>45</td>
<td>1.15</td>
<td>1.19</td>
<td>25.6</td>
<td>26.4</td>
<td>51.8</td>
<td>53.6</td>
<td>105.3</td>
<td>68</td>
<td>83.0</td>
<td>93.7</td>
</tr>
<tr>
<td>48</td>
<td>1.27</td>
<td>1.32</td>
<td>26.5</td>
<td>27.6</td>
<td>60.8</td>
<td>63.2</td>
<td>126.1</td>
<td>75</td>
<td>94.5</td>
<td>106.2</td>
</tr>
<tr>
<td>50</td>
<td>1.38</td>
<td>1.45</td>
<td>27.6</td>
<td>29.0</td>
<td>68.6</td>
<td>72.1</td>
<td>140.7</td>
<td>82</td>
<td>106.2</td>
<td>120.7</td>
</tr>
</tbody>
</table>

**Ron vs temperature**

**Power loss vs temperature**

- **SW1**: $y = 0.0004x^2 + 0.0382x + 20.362$  \[R^2 = 0.9995\]
- **SW2**: $y = 0.0004x^2 + 0.0255x + 20.736$  \[R^2 = 0.9991\]

- **Tj_1**: $y = 0.6868x + 21.329$  \[R^2 = 0.9956\]
- **Tj_2**: $y = 0.5773x + 22.414$  \[R^2 = 0.9935\]
- **Tc**: $y = 0.433x + 21.329$  \[R^2 = 0.9991\]
Gen-2 BiDFET: Chip Design

**Objective:** Improved design with 2x lower specific on-resistance for the same die size.

- Gen-1 BiDFET, with on-resistance of 50 mΩ, has JBS diode integrated within MOSFET cells.
- Gen-2 BiDFET, with on-resistance of 26 mΩ, has JBS diode and MOSFET in separate parts of the JBSFET chip.
- Gen-2 BiDFET On-Resistance further reduction achieved by reducing gate oxide thickness from 55 to 27 nm and reducing channel length from 0.5 µm to 0.3 µm.
- Higher ohmic contact anneal temperature used to further reduce specific on-resistance.
- New BP-2 BiDFET Design has same active area and chip size as the BP-1 BiDFET.

- JBS Diode Active Area = 0.045 cm²
- MOSFET Active Area = 0.405 cm²
- MOSFET $R_{on,sp}$ = 5.3 mΩ-cm²
- MOSFET $R_{on}$ = 13 mΩ
- BP-2 BiDFET $R_{on}$ = 26 mΩ
- BP-2 BiDFET $I_{on}$ = 25 A
- BP-2 BiDFET $V_{on}$ = 0.65 V @ 25 A
Gen-2 BiDFET: Temperature Sensor

New feature created in Gen-2 BiDFET: On-Chip Temperature Sensing Capability

- Makes use of Silicided Polysilicon Gate Electrode Layer
- No additional processing steps required
- Silicided Polysilicon Sheet Resistance: 3 \( \Omega \)/square
- 100 \( \Omega \) Poly-Si resistor integrated on-chip to allow BiDFET device temperature monitoring
Temperature Sense Resistor: Uniformity

Sense Resistor Room Temperature Data

- Measured Temperature Sense Resistance @ RT = 90 Ω
- Matches design value of ~100 Ω
- Achieved project goal

<table>
<thead>
<tr>
<th>Wafer Position</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottom</td>
<td>90 Ω</td>
</tr>
<tr>
<td>Right</td>
<td>91 Ω</td>
</tr>
<tr>
<td>Middle</td>
<td>87 Ω</td>
</tr>
<tr>
<td>Top</td>
<td>92 Ω</td>
</tr>
</tbody>
</table>
The 1.2 kV BiDFET Switch: Switching Performance

Test Conditions: $V_{DC} = 800 \text{ V}$, $I_{T2-T1} = 8-20 \text{ A}$, Case Temperatures: 25 °C, Gate resistances = 10 Ω
LS Switch: 1.2 kV BiDFET ($V_{G1-T1} = -5/20 \text{ V}$, $V_{G2-T2} = 20 \text{ V}$), HS Switch: 1.2 kV BiDFET ($V_{G1-T1} = -5 \text{ V}$, $V_{G1-T1} = 20 \text{ V}$)

<table>
<thead>
<tr>
<th>$I_{ON}$ (A)</th>
<th>$E_{ON}$ (µJ)</th>
<th>$E_{OFF}$ (µJ)</th>
<th>$E_{SW,T}$ (µJ)</th>
<th>$E_{SW,T}$ Norm.</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>559</td>
<td>271</td>
<td>830</td>
<td>0.9</td>
</tr>
<tr>
<td>10</td>
<td>620</td>
<td>298</td>
<td>918</td>
<td>1.0</td>
</tr>
<tr>
<td>12</td>
<td>688</td>
<td>360</td>
<td>1048</td>
<td>1.14</td>
</tr>
<tr>
<td>15</td>
<td>792</td>
<td>438</td>
<td>1230</td>
<td>1.34</td>
</tr>
<tr>
<td>18</td>
<td>889</td>
<td>553</td>
<td>1442</td>
<td>1.57</td>
</tr>
<tr>
<td>20</td>
<td>939</td>
<td>633</td>
<td>1572</td>
<td>1.71</td>
</tr>
</tbody>
</table>

The BiDFET switching losses increase by a factor of 1.71x when $I_{ON}$ rises from 10 to 20 A.

The BiDFET exhibits a current overshoot during turn-on transitions due to output capacitance of HS switch.
**The 1.2 kV BiDFET Switch: Switching Performance**

**Test Conditions:**
- $V_{DC} = 800 \text{ V}$, $I_{T_1,T_2} = 10 \text{ A}$, Case Temperatures: 25°C, Gate resistances = 2-20 Ω
- LS Switch: 1.2 kV BiDFET ($V_{G_1T_1} = -5/20 \text{ V}$, $V_{G_2T_2} = 20 \text{ V}$), HS Switch: 1.2 kV BiDFET ($V_{G_1T_1} = -5 \text{ V}$, $V_{G_1T_1} = 20 \text{ V}$)

### Current Flow Schematics:

**With Low-side BiDFET G₁₁ On**

![Diagram of BiDFET with Low-side G₁₁ On]

**With Low-side BiDFET G₁₁ Off**

![Diagram of BiDFET with Low-side G₁₁ Off]

### switching Loss Table

<table>
<thead>
<tr>
<th>$R_G$ (Ω)</th>
<th>$E_{ON}$ (µJ)</th>
<th>$E_{OFF}$ (µJ)</th>
<th>$E_{SW,T}$ (µJ)</th>
<th>$E_{SW,T}$ Norm.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>313</td>
<td>252</td>
<td>565</td>
<td>0.62</td>
</tr>
<tr>
<td>5</td>
<td>456</td>
<td>259</td>
<td>715</td>
<td>0.78</td>
</tr>
<tr>
<td>10</td>
<td>620</td>
<td>298</td>
<td>918</td>
<td>1.00</td>
</tr>
<tr>
<td>20</td>
<td>964</td>
<td>566</td>
<td>1530</td>
<td>1.67</td>
</tr>
</tbody>
</table>

The BiDFET switching losses increase with gate resistance due to increased switching transition time.

Increased gate resistance reduces gate current leading to a slow transient (reduced dV/dt). The slow transients result in a reduced current overshoot at turn-on.
The 1.2 kV BiDFET Switch: Switching Performance – Loss vs Case Temperature

Test Conditions: \( V_{DC} = 800 \, \text{V}, I_{T_2T_1} = 10 \, \text{A}, \) Case Temperatures: 25-140 \( ^\circ \text{C} \), Gate resistances = 10 \( \Omega \)

LS Switch: 1.2 kV BiDFET (\( V_{G1T1} = -5/20 \, \text{V}, V_{G2T2} = 20 \, \text{V} \)), HS Switch: 1.2 kV BiDFET (\( V_{G1T1} = -5 \, \text{V}, V_{G1T1} = 20 \, \text{V} \))

Current Flow Schematics:
With Low-side BiDFET \( G_{II} \) On

![Current Flow Schematic with Low-side BiDFET \( G_{II} \) On](image)

With Low-side BiDFET \( G_{II} \) Off

![Current Flow Schematic with Low-side BiDFET \( G_{II} \) Off](image)

<table>
<thead>
<tr>
<th>( T_c ) (°C)</th>
<th>( E_{ON} ) (µJ)</th>
<th>( E_{OFF} ) (µJ)</th>
<th>( E_{SW,T} ) (µJ)</th>
<th>( E_{SW,T} ) Norm.</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>620</td>
<td>298</td>
<td>918</td>
<td>1</td>
</tr>
<tr>
<td>50</td>
<td>593</td>
<td>308</td>
<td>901</td>
<td>0.96</td>
</tr>
<tr>
<td>75</td>
<td>556</td>
<td>301</td>
<td>857</td>
<td>0.9</td>
</tr>
<tr>
<td>100</td>
<td>540</td>
<td>316</td>
<td>856</td>
<td>0.87</td>
</tr>
<tr>
<td>125</td>
<td>524</td>
<td>317</td>
<td>841</td>
<td>0.85</td>
</tr>
<tr>
<td>140</td>
<td>516</td>
<td>315</td>
<td>831</td>
<td>0.83</td>
</tr>
</tbody>
</table>

Reduced output capacitance of the high-side switch results in reduction of switching loss with case temperature.

The BiDFET switching losses decrease by 17% as case temperature increases from 25 \( ^\circ \text{C} \) to 140 \( ^\circ \text{C} \).

Peak currents at turn-on exhibit small reduction with increasing case temperature.
BiDFET blocking characteristics:

- In 1st quadrant: \( V_{G1-T1} = V_{G2-T2} = 0 \) V, \( V_{T2-T1} > 0 \) V, \( V_{T2-T1} \) supported by JBSFET-1.
- In 3rd quadrant: \( V_{G1-T1} = V_{G2-T2} = 0 \) V, \( V_{T2-T1} < 0 \) V, \( V_{T2-T1} \) supported by JBSFET-2.
- \( BV @ 100 \mu A > 1400 \) V in both 1st and 3rd quadrants.

BiDFET output characteristics:

- Conduction through series JBS diode.
- Knee Voltage = 1.2 V.
- Output characteristics in 1st quadrant for \( V_{G2-T2}=20 \) V.
- \( R_{on} @ I_{T2-T1}=10 \) A and \( V_{G1-T1}=20 \) V is 50 m\( \Omega \).
- Output characteristics in 3rd quadrant for \( V_{G1-T1}=20 \) V.
- \( R_{on} @ I_{T2-T1}=-10 \) A and \( V_{G2-T2}=20 \) V is 50 m\( \Omega \).

BiDFET transfer characteristics:

- Conduction through JBSFET-1 channel for both cases.
- \( V_{th} @ V_{T2-T1}=20 \) V, \( I_{T2-T1}=10 \) mA was 1.35 V.
- \( Gm @ V_{T2-T1}=20 \) V, \( I_{T2-T1}=20 \) A was 17 S.

- Conduction through JBSFET-1 & JBSFET-2 channels for \( V_{G2-T2}=20 \) V case.
- No conduction for \( V_{G2-T2}=0 \) V case, because 0.1 V on T2 is not enough to forward bias internal JBS diode of JBSFET-2.
- \( V_{th} @ V_{T2-T1}=0.1 \) V, \( I_{T2-T1}=10 \) mA was 1.73 V.
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